CMOS single-chip 8-bit MCU with 10-bit A/D converter

Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 4Kbytes Flash Code Memory
  - 256bytes IRAM
  - 128bytes Data EEPROM
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Reset
  - Internal 1MHz RC Oscillator (±1.0%, T_A= -10 ~ +40°C, User trim)
  - Watchdog Timer RC Oscillator (1kHz)
- **Peripheral Features**
  - 10-bit Analog to Digital Converter (9 inputs)
  - Line Interface (Two Rx and Five Tx modes)
  - 16-bit CRC/Checksum Generator
- **I/O and Packages**
  - Up to 14 Programmable I/O lines with 16 pin package.
  - 16 SOPN
  - Pb-free package
- **Operating Conditions**
  - 2.0V to 5.5V Wide Voltage Range
  - -40°C to 85°C Temperature Range
- **Application**
  - Smoke detector and Fire system

A96L302

Datasheet

V 1.1

13 December, 2022

Revision history

Version	Date	Revision list
1.0	2018.07.20	Published this book.
1.1	2022.12.13	Modify a font.

Version 1.1

Published by FAE team

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1 Overview

1.1 Description

The A96L302 is an advanced CMOS 8-bit microcontroller with 4Kbytes of FLASH memory. This is powerful microcontroller which provides low power consumption and cost effective solution to smoke detector applications. This provides the following features : 4Kbytes of FLASH memory, 256bytes of IRAM, 128bytes of Data EEPROM, general purpose I/O, basic interval timer, watchdog timer, 16-bit timer/counter, 16-bit PPG output, Line Interface, 10-bit A/D converter, Flash CRC/Checksum generator, on-chip POR, LVR, on-chip oscillator and clock circuitry. The A96L302 also supports power down modes to reduce power consumption.

Device Name	FLASH	IRAM	EEPROM	ADC	I/O PORT	Package
A96L302AEN	4Kbytes	256bytes	128bytes	9inputs	14	16 SOPN

Table 1.1 Ordering Information of A96L302

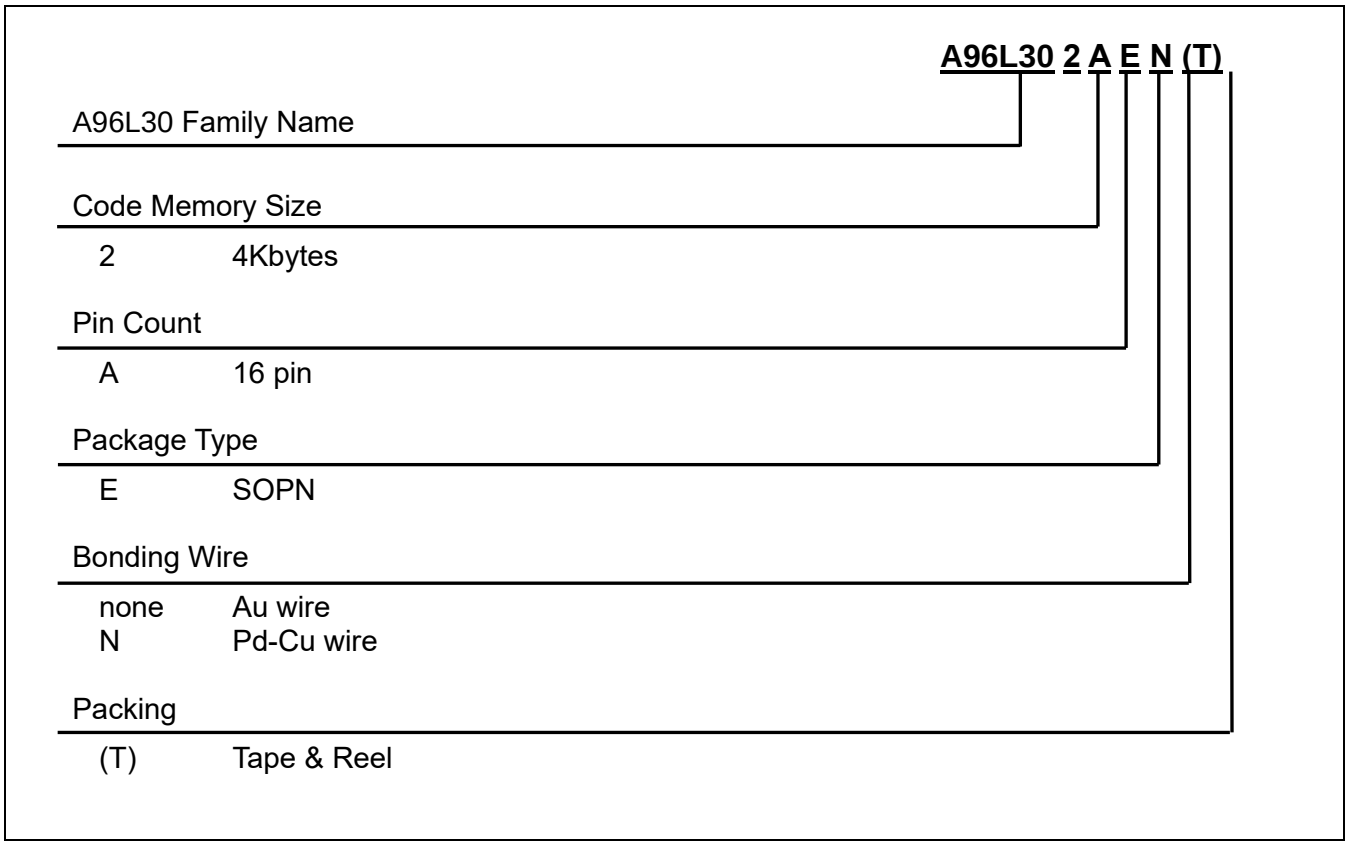


Figure 1.1 Device Nomenclature

1.2 Features

- **CPU**
  - 8-bit CISC core (M8051, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 4Kbytes Flash with self read/write capability
  - On Chip debug and In-System Programming(ISP)
  - Endurance : 10,000 cycles (Sector 0 ~ 119)
    100,000 cycles (Sector 120 ~ 127)
- **256bytes IRAM**
- **128bytes Data EEPROM**
  - Endurance : 100,000 cycles
- **General Purpose I/O (GPIO)**
  - Normal I/O : 14 Ports
    (P0[7:0], P1[5:0])
- **Timer/Counter**
  - Basic Interval Timer (BIT) 8-bit× 1-ch
  - Watch Dog Timer (WDT) 8-bit × 1-ch
    1kHz internal RC oscillator for WDT
  - 16-bit× 2-ch (T0/T1)
- **Programmable Pulse Generation**
  - Pulse generation (by T0/T1)
- **Line Interface**
  - Two Rx and Five Tx modes
- **10-bit A/D Converter**
  - 9 Input channels
- **16-Bit CRC/Checksum Generator**
  - Auto and User CRC/Checksum mode
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 3 level detect
    (1.60V/ 2.20V/ 2.70V)
- **Interrupt Sources**
  - External Interrupts
    (EINT0/1/2/3/10/11) (6)
  - Timer(0/1) (2)
  - WDT (1)
  - BIT (1)
  - Line Interface Rx/Tx (2)
  - ADC (1)
- **Internal RC Oscillator**
  - 1MHz ± 3.0% (TA = -40°C to +85°C)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 2.0V ~ 5.5V (@ 0.125 ~ 1.0MHz with IRC)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 2us (@1MHz IRC)
- **Operating Temperature**
  - –40 ~ +85℃
- **Package Type**
  - 16 SOPN
  - Pb-free package

1.3 Development tools

1.3.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of A96L302 is Mentor 8051. And, device ROM size is smaller than 64Kbytes. Developer can use all kinds of third party's standard 8051 compiler.

1.3.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two-wire interfacing between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32bit) operating system.

If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site(http://www.abov.co.kr).

Connection:

- DSCL (A96L302 P12 port)
- DSDA (A96L302 P13 port)

OCD connector diagram: Connect OCD with user system

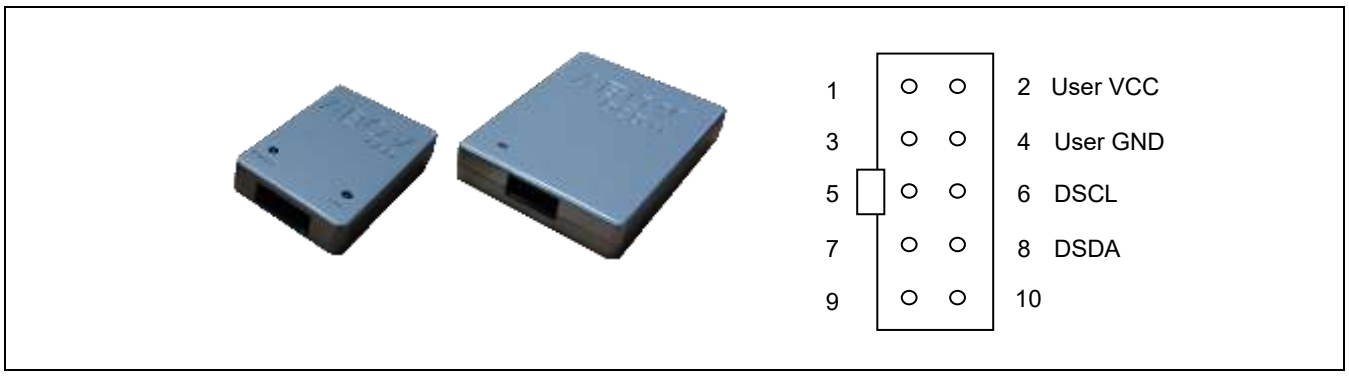


Figure 1.2 Debugger(OCD1/OCD2) and Pin description

1.3.3 Programmer

Single programmer :

E-PGM+ : It programs MCU device directly.

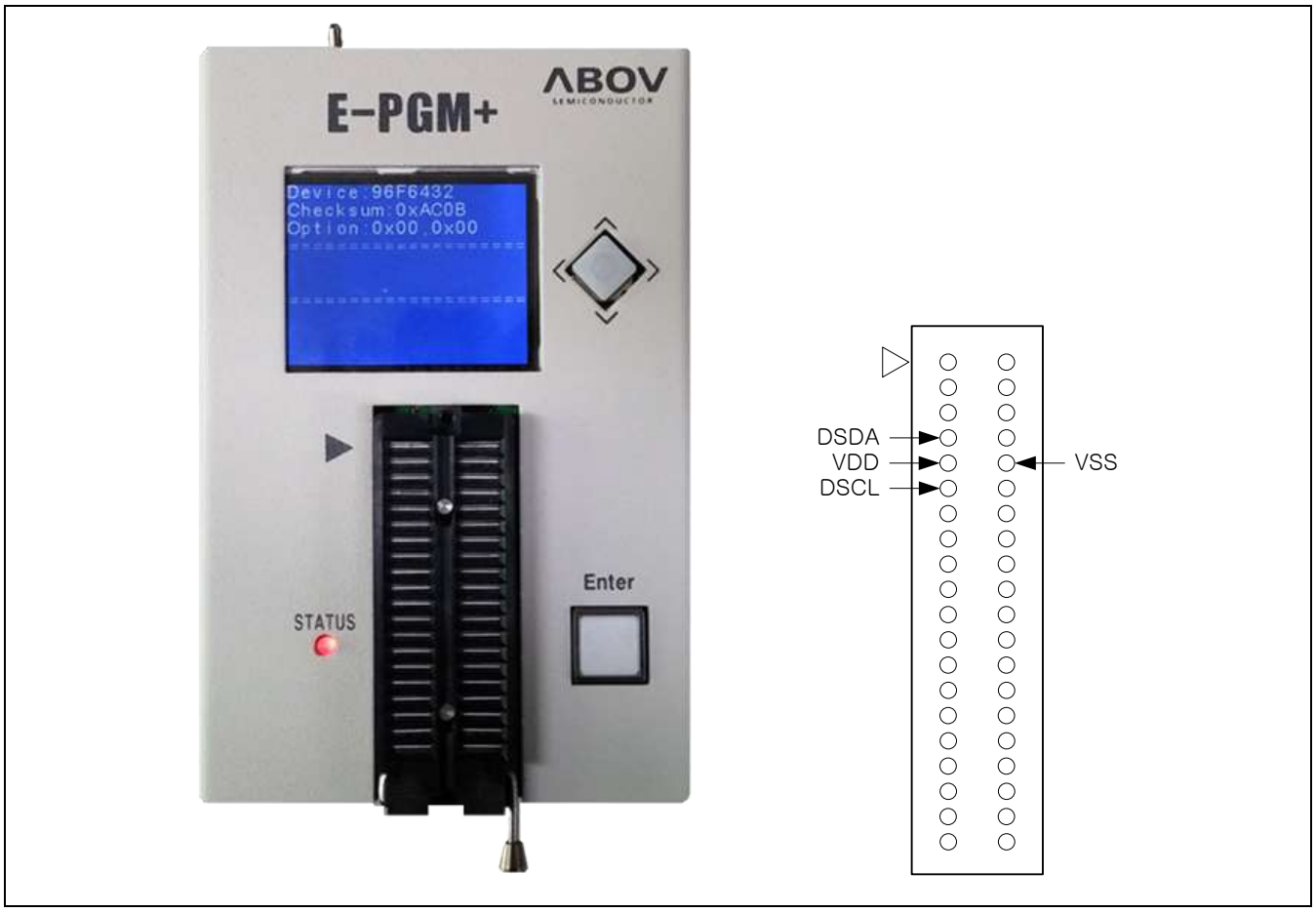


Figure 1.3 E-PGM+ (Single writer)

OCD emulator:

It can write code to MCU device too, because OCD debugger supports ISP (In System Programming).It does not require additional H/W, except developer's target system.

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

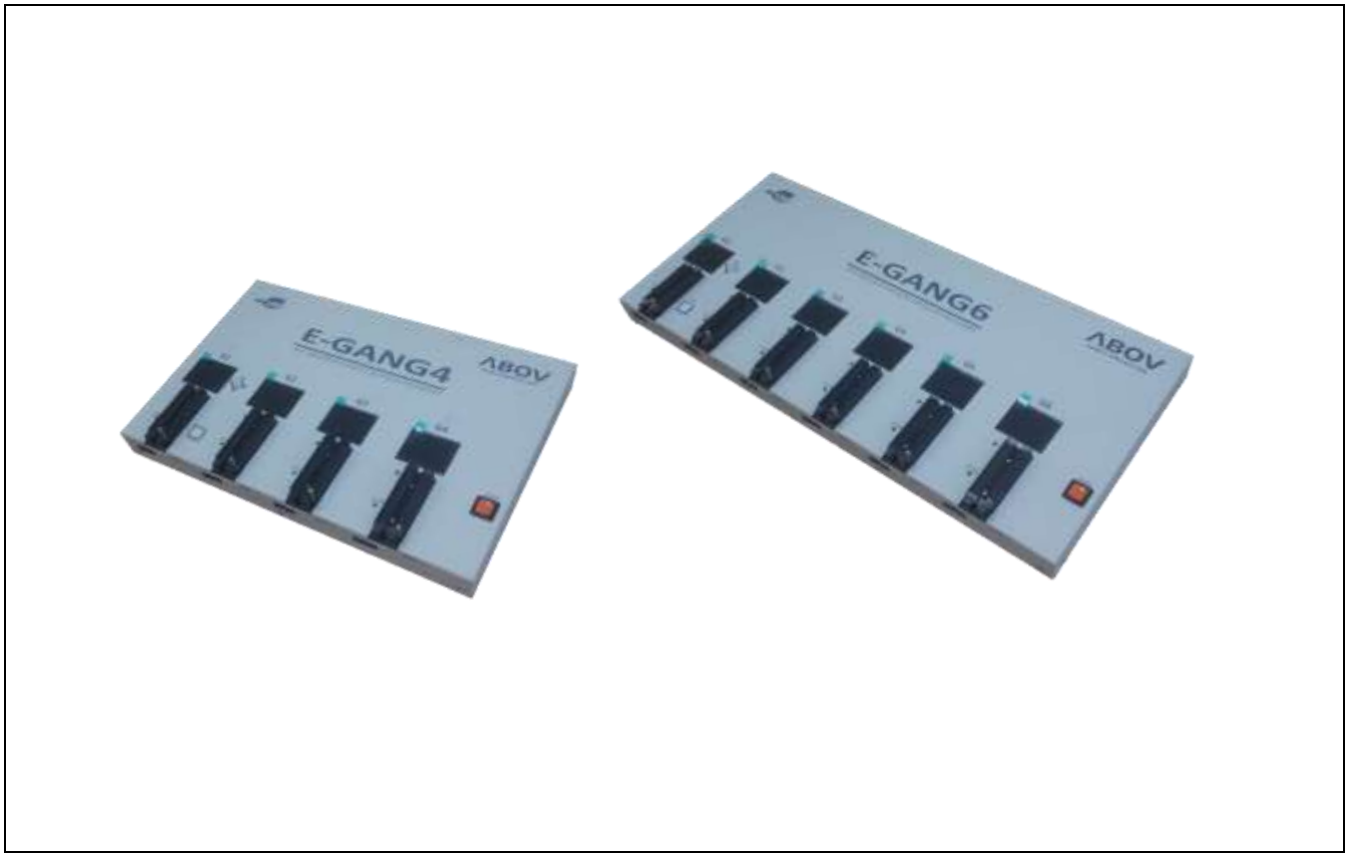


Figure 1.4 E-GANG4 and E-GANG6 (for Mass Production)

1.4 MTP programming

1.4.1 Overview

The program memory of A96L302 is MTP Type. This flash is accessed by serial data format. There are four pins(DSCL, DSDA, VDD, VSS) for programming/reading the flash.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P12	I	Serial clock pin. Input only pin.
DSDA	P13	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

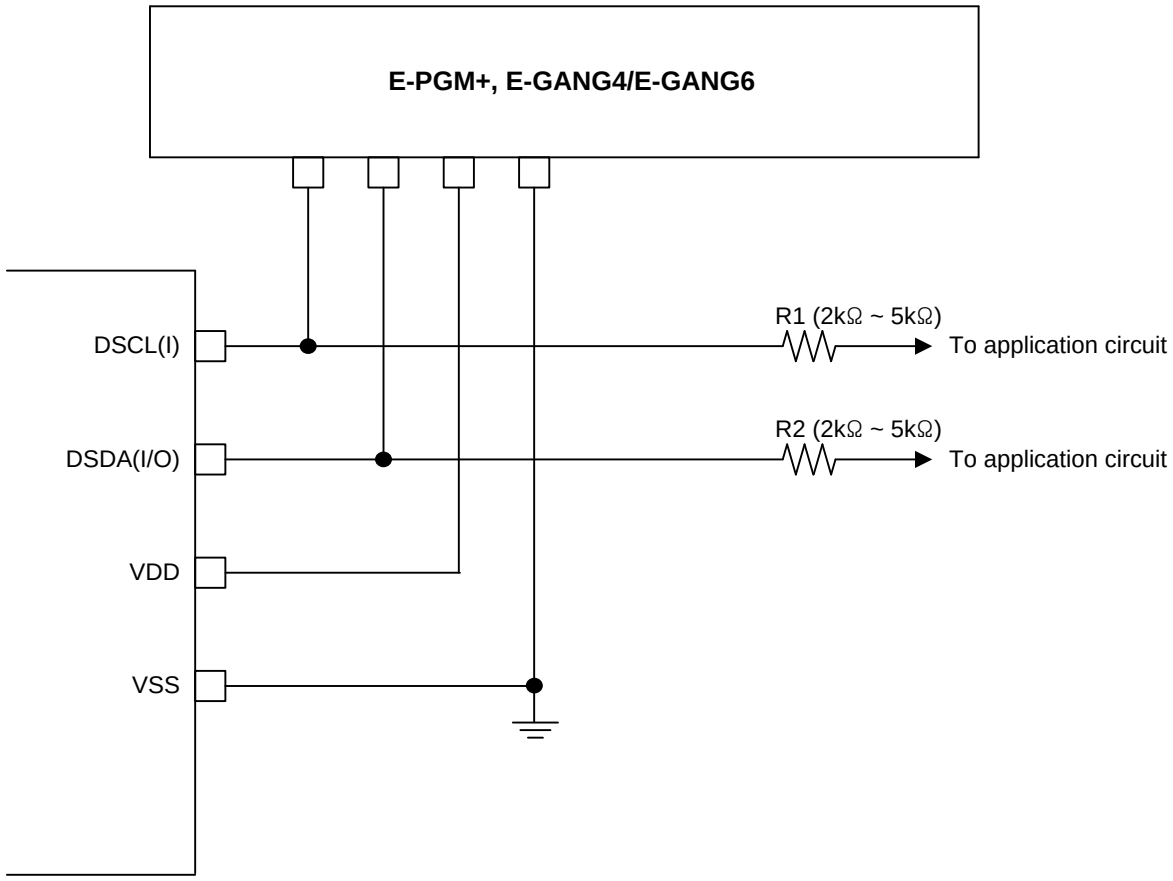
Table 1.2 Descriptions of pins which are used to programming/reading the Flash

1.4.2 On-Board programming

The A96L302 needs only four signal lines including VDD and VSS pins for programming FLASH with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

1.4.3 Circuit Design Guide

At the FLASH programming, the programming tool needs 4 signal lines that are DSCL, DSDA, VDD, and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming. Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTE)

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 1.5 PCB design guide for on board programming

2 Block diagram

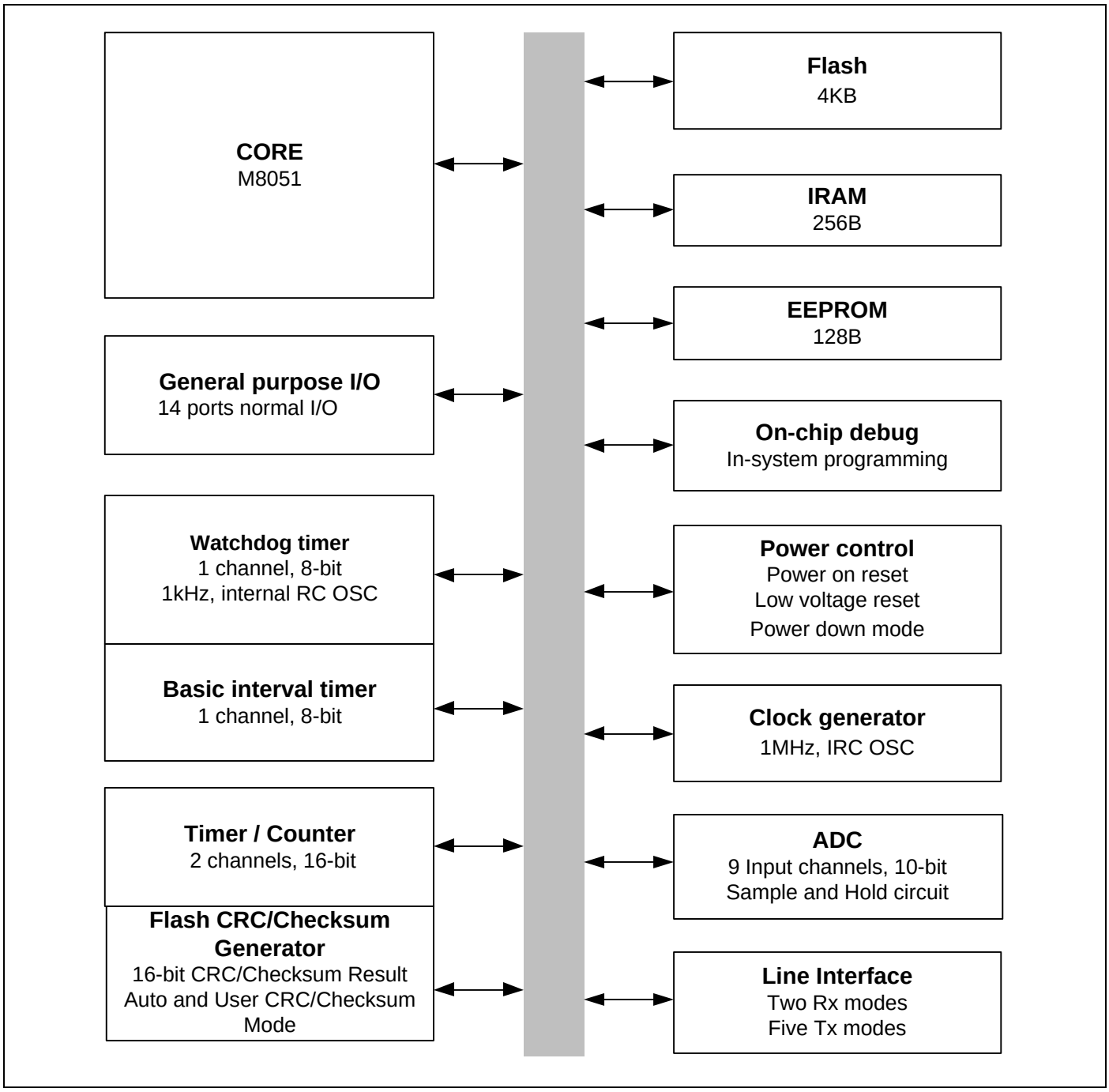
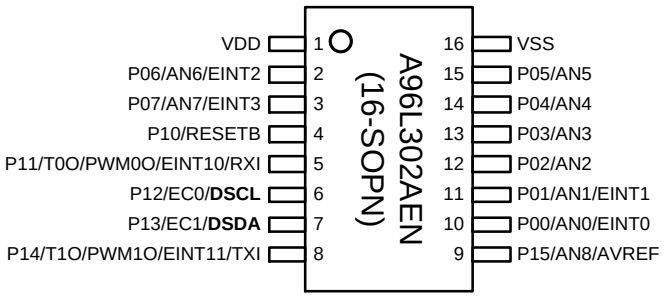


Figure 2.1 Block diagram of A96L302

3 Pin assignment



NOTE)

1. On On-Chip Debugging, ISP uses P1[2:3] pin as DSCL, DSDA.

Figure 3.1 A96L302AEN 16SOPN Pin Assignment

4 Package Diagram

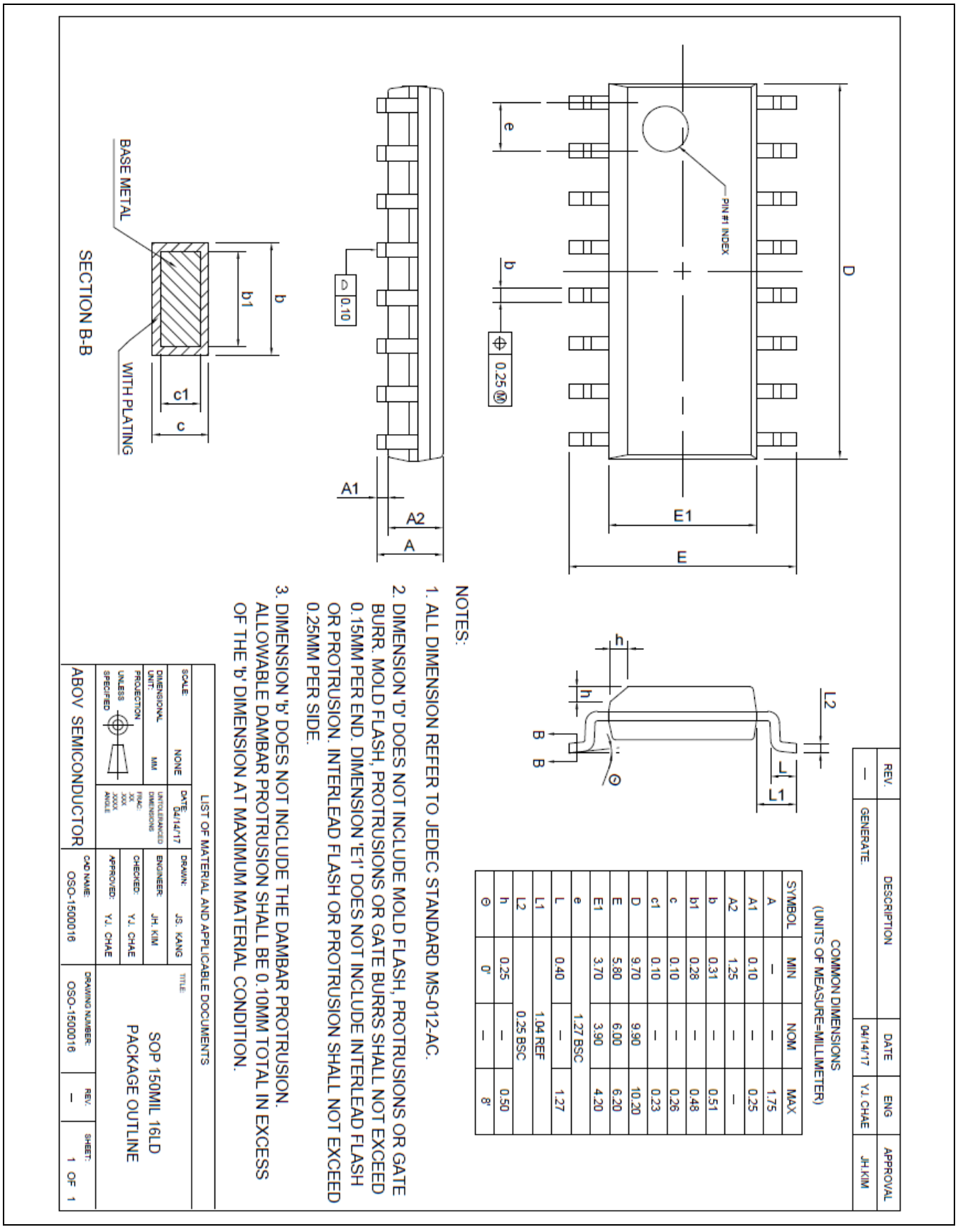


Figure 4.1 16-Pin SOPN Package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	The port 0 is a bit-programmable I/O port which can be configured as an input (P00/P01/P06/P07: Schmitt trigger input), a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	AN0/EINT0
P01				AN1/EINT1
P02				AN2
P03				AN3
P04				AN4
P05				AN5
P06				AN6/EINT2
P07				AN7/EINT3
P10	I/O	The port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	RESETB
P11				T0O/PWM0O/EINT10/RXI
P12				EC0/DSCL
P13				EC1/DSDA
P14				T1O/PWM1O/EINT11/TXI
P15				AN8/AVREF
EINT0	I/O	External interrupt inputs	Input	P00/AN0
EINT1				P01/AN1
EINT2				P06/AN6
EINT3				P07/AN7
EINT10	I/O	External interrupt input and Timer 0 capture input	Input	P11/T0O/PWM0O/RXI
EINT11	I/O	External interrupt input and Timer 1 capture input	Input	P14/T1O/PWM1O/TXI
T0O	I/O	Timer 0 interval output	Input	P11/PWM0O/EINT10/RXI
T1O	I/O	Timer 1 interval output	Input	P14/PWM1O/EINT11/TXI
PWM0O	I/O	Timer 0 pulse output	Input	P11/T0O/EINT10/RXI
PWM1O	I/O	Timer 1 pulse output	Input	P14/T1O/EINT11/TXI
EC0	I/O	Timer 0 event count input	Input	P12/DSCL
EC1	I/O	Timer 1 event count input	Input	P13/DSDA
RXI	I/O	Line interface receive input	Input	P11/T0O/PWM0O/EINT10
TXI	I/O	Line interface transmit output	Input	P14/T1O/PWM1O/EINT11
AN0	I/O	A/D converter analog input channels	Input	P00/EINT0
AN1				P01/EINT1
AN2				P02
AN3				P03
AN4				P04
AN5				P05
AN6				P06/EINT2
AN7				P07/EINT3
AN8				P15/AVREF
AVREF	I/O	A/D converter reference voltage	Input	AN8/P15

Table 5.1 Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P10
DSCL	I/O	On chip debugger clock input	Input	EC0/P12
DSDA	I/O	On chip debugger data input/output	Input	EC1/P13
VDD, VSS	–	Power input pins	–	–

Table 5.1 Normal Pin Description (Concluded)

NOTE)

1. The P10/RESETB pin is configured as one of the P10 and the RESETB pin by the “CONFIGURE OPTION”.
2. If the P13/DSDA and P12/DSCL pins are connected to an emulator during reset or power-on reset, the pins are automatically configured as the debugger pins.
3. The P13/DSDA and P12/DSCL pins are configured as inputs with an internal pull-up resistor only during the reset or power-on reset.

6 Port Structures

6.1 General Purpose I/O Port

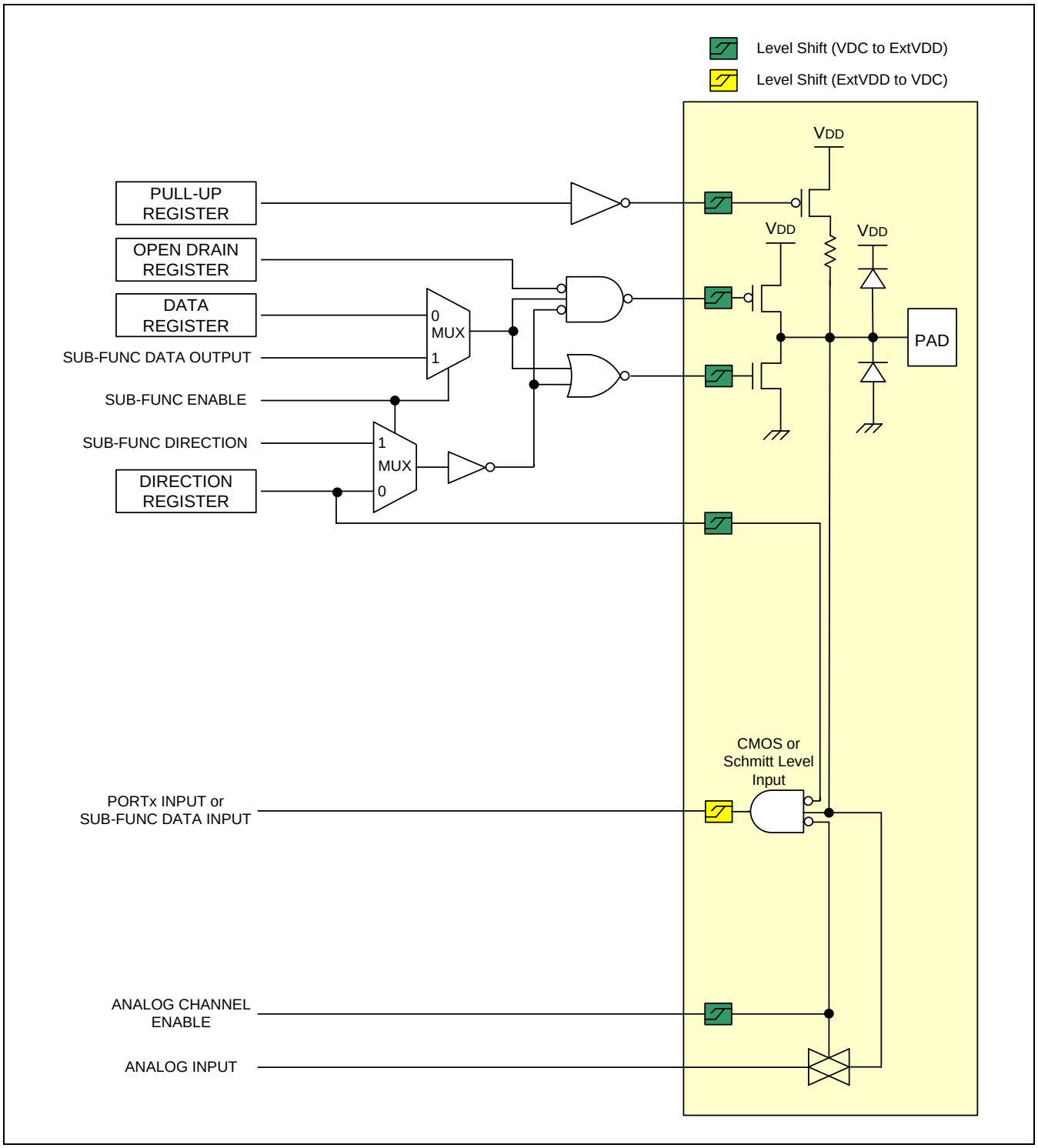


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

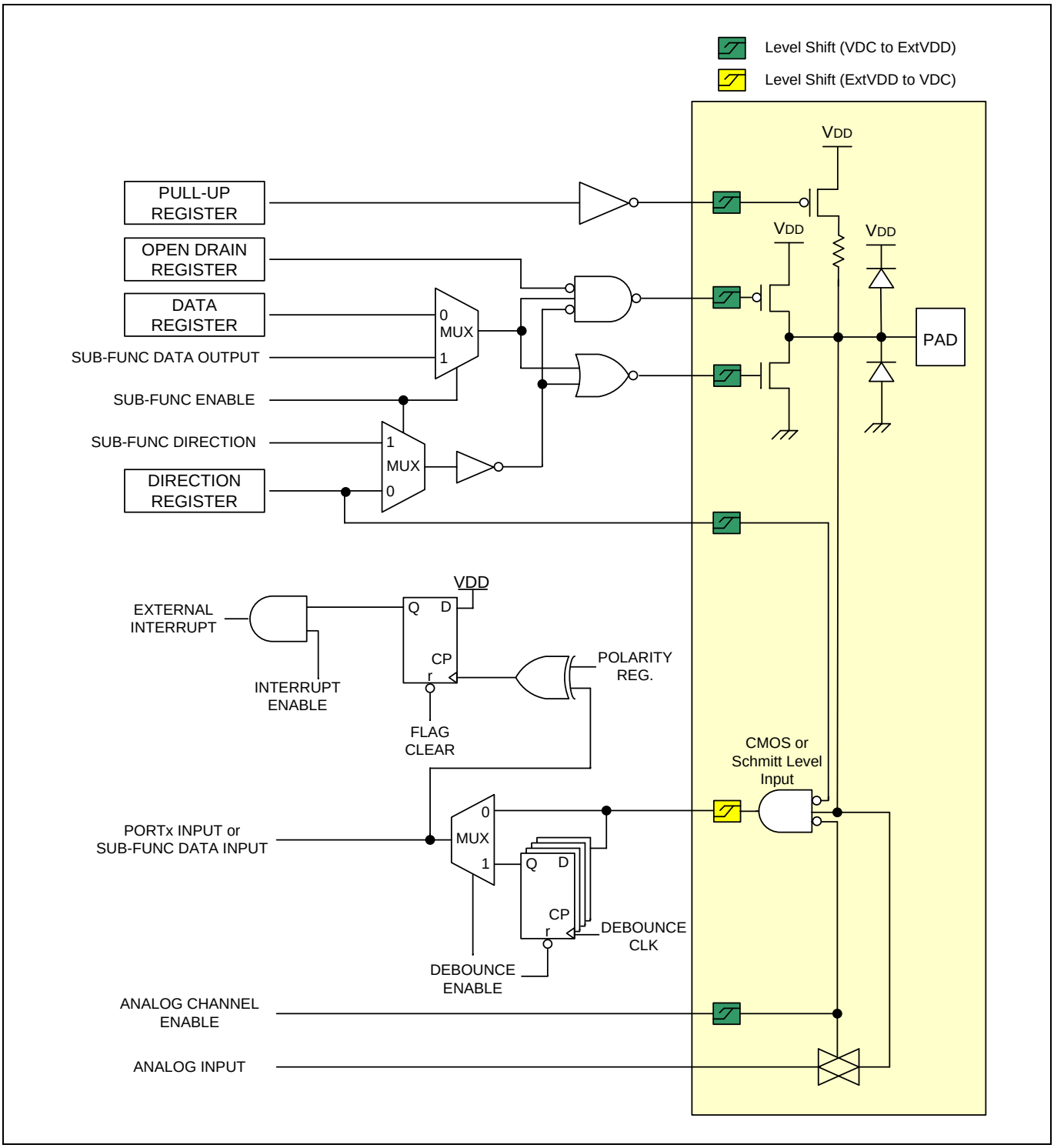


Figure 6.2 External Interrupt I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3 ~ +6.0	V	–
Normal Voltage Pin	V_I	-0.3 ~ VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 ~ VDD+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	120	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65 ~ +150	°C	–

Table 7.1 Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A=-40°C ~ +85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 0.125 ~ 1.0MHz, Internal RC	2.0	–	5.5	V
Operating Temperature	T_{OPR}	VDD= 2.0 ~ 5.5V	-40	–	85	°C

Table 7.2 Recommended Operating Conditions

7.3 A/D Converter Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	–	–		–	10	–	bit
Integral Linear Error	ILE	AVREF= 2.7V – 5.5V fx= 1MHz		–	–	±3	LSB
Differential Linearity Error	DLE			–	–	±1	
Top Offset Error	TOE			–	–	±5	
Zero Offset Error	ZOE			–	–	±5	
Conversion Time	t_{CON}	AVREF= 2.7V – 5.5V		54	–	–	us
Analog Input Voltage	V_{AN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	*Note 3		2.0	–	VDD	
Sample/Hold Time	t_{SH}	–		2	–	–	us
A/DC Input Leakage Current	IAN	AVREF=3.3V		–	–	2	uA
A/DC Current	I_{ADC}	Enable	VDD= 3.3V	–	300	500	uA
		Disable		–	–	0.1	uA

Table 7.3 A/D Converter Characteristics

NOTE)

1. Zero offset error is the difference between 0000000000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 1111111111 and the converted output for top input voltage (AVREF).
3. If AVREF is less than 2.7V, the resolution degrades by 1-bit whenever AVREF drops 0.1V. (@ADCLK = 0.5MHz, Under 2.7V resolution has no test.)

7.4 Power-On Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	–	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

Table 7.4 Power-on Reset Characteristics

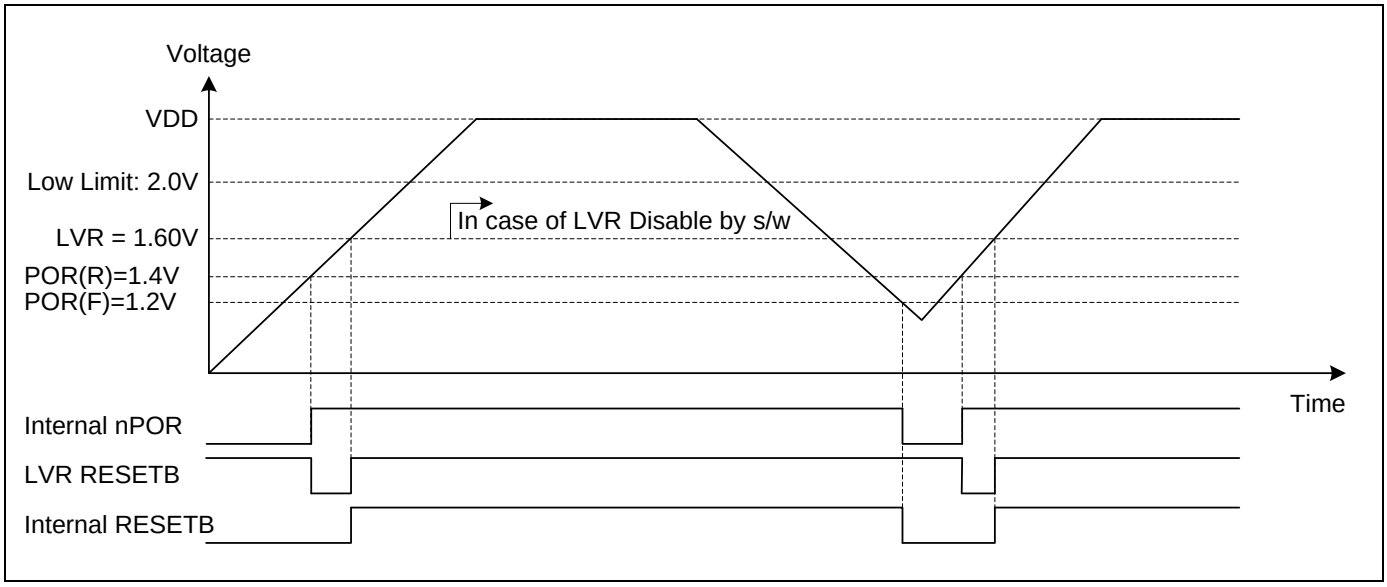


Figure 7.1 Power-on Reset Timing

7.5 Low Voltage Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR}	The LVR can select all levels		–	1.60	1.79	V
				2.05	2.20	2.35	
				2.50	2.70	2.90	
Hysteresis	△V	–		–	10	100	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR Current	I_{LVR}	Enable	VDD= 3V, Run mode	–	3.0	6.0	uA
		Disable		–	–	0.1	

Table 7.5 LVR Characteristics

7.6 Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{IRC}	VDD=3.3V	–	1	–	MHz
Tolerance	–	T_A = -10°C to +40°C, with user(S/W) trim	–	–	±1.0	%
		T_A = -10°C to +40°C			±2.0	
		T_A = -40°C to +85°C			±3.0	
Clock Duty Ratio	T_{OD}	–	40	50	60	%
Stabilization Time	T_{FS}	–	–	–	100	us
IRC Current	I_{IRC}	Enable	–	15	–	uA
		Disable	–	–	0.1	uA

Table 7.6 Internal RC Oscillator Characteristics

7.7 Internal Watch-Dog Timer RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	–	0.5	1	2	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

Table 7.7 Internal WDTRC Oscillator Characteristics

7.8 DC Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.0V ~ 5.5V, VSS= 0V, f_{IRC} = 1MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P00, P01, P06, P07, P1, RESETB		0.8VDD	–	VDD	V
	V_{IH2}	All input pins except VIH1		0.7VDD	–	VDD	
Input Low Voltage	V_{IL1}	P00, P01, P06, P07, P1, RESETB		–	–	0.2VDD	V
	V_{IL2}	All input pins except VIL1		–	–	0.3VDD	
Output High Voltage	V_{OH}	VDD=4.5V, IOH = – 2mA; All output ports		VDD-1.0	–	–	V
Output Low Voltage	V_{OL}	VDD=4.5V, IOL=10mA; All output ports		–	–	1.0	V
Input High Leakage Current	I_{IH}	All Input ports		–	–	1.0	uA
Input Low Leakage Current	I_{IL}	All Input ports		- 1.0	–	–	uA
Pull-Up Resistor	R_{PU1}	VI=0V, TA=25°C, All Input ports	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
	R_{PU2}	VI=0V, TA=25°C, RESETB	VDD=5.0V	150	250	400	kΩ
			VDD=3.0V	300	500	700	
Supply Current	I_{DD1} (RUN)	f_{IRC} = 1MHz	VDD=3V±10%	–	240	320	uA
		f_{IRC} = 0.5MHz		–	150	200	
	I_{DD2} (IDLE)	f_{IRC} = 1MHz	VDD=3V±10%	–	85	130	uA
		f_{IRC} = 0.5MHz		–	80	125	
	I_{DD5}	STOP, VDD= 3V±10%, T_A= 25°C		–	0.5	3.0	uA

Table 7.8 DC Characteristics

NOTE)

1. Where the fx is the selected system clock, the f_{IRC} is an internal RC oscillator.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current include the current of the power-on reset (POR) block.

7.9 AC Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.0V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RST}	VDD= 5V	10	–	–	us
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	EC0/EC1, VDD = 5V	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	EC0/EC1, VDD = 5V	20	–	–	

Table 7.9 AC Characteristics

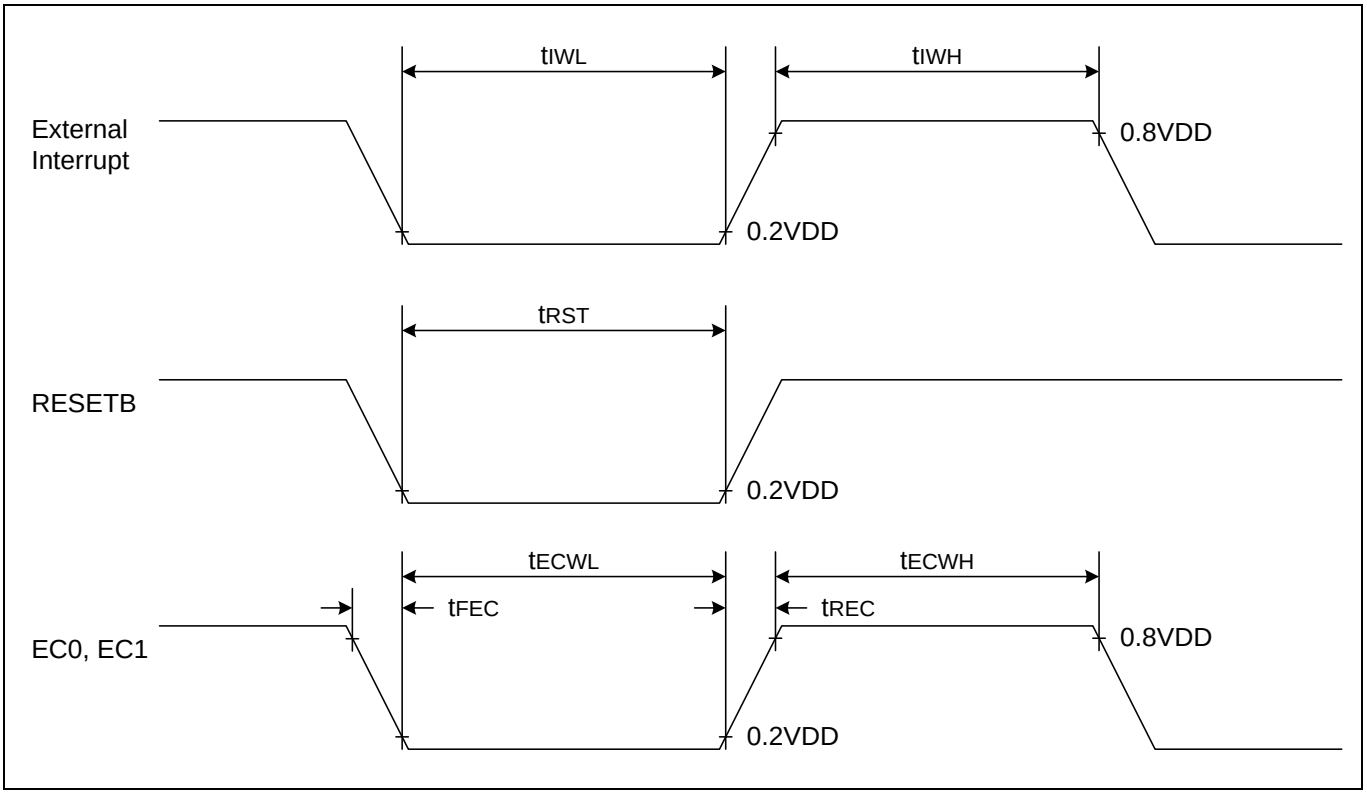


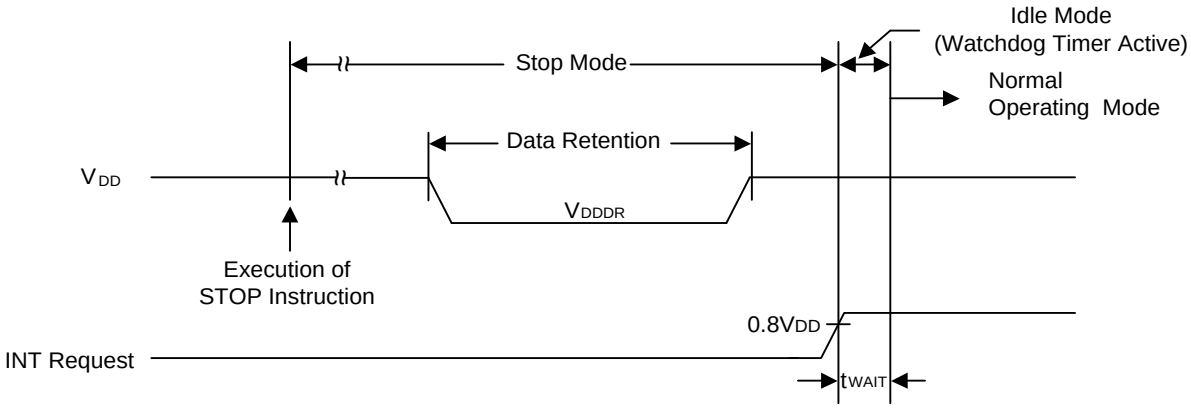
Figure 7.2 AC Timing

7.10 Data Retention Voltage in Stop Mode

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V)

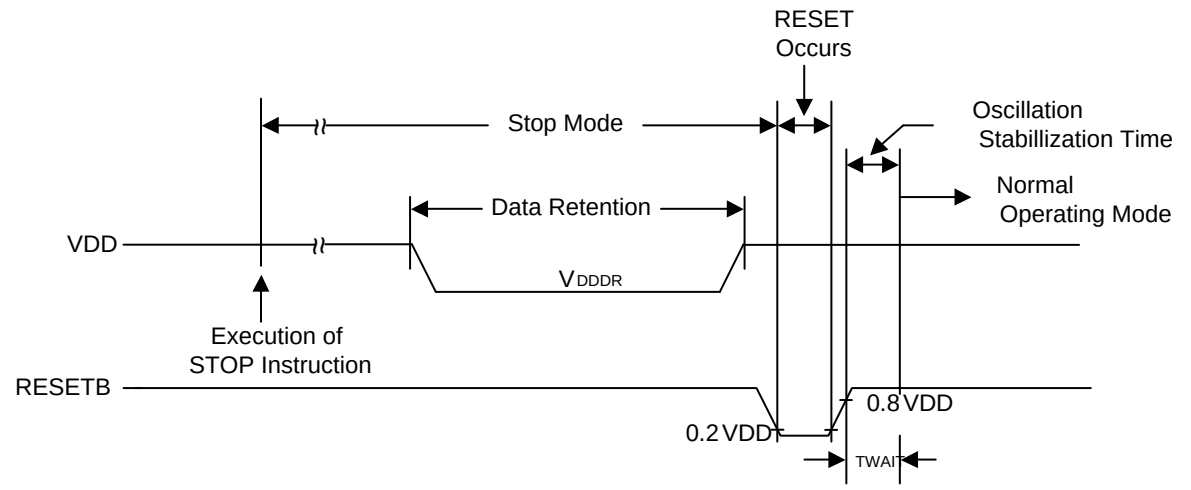
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	2.0	–	5.5	V
Data retention supply current	I_{DDDR}	VDDR= 2.0V, (T_A= 25°C), Stop mode	–	–	1	uA

Table 7.10 Data Retention Voltage in Stop Mode



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.3 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X f_{IRC}) = (16.4 mS at fx=1MHz).

Figure 7.4 Stop Mode Release Timing when Initiated by RESETB

7.11 Internal Flash Rom Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.125	–	–	MHz
Endurance of Write/Erase (Sector 0 ~ 119)	NF_{WE}	Sector Erase, Byte Write	10,000	–	–	cycles
Endurance of Write/Erase (Sector 120 ~ 127)			100,000	–	–	

Table 7.11 Internal Flash Rom Characteristics

7.12 Internal EEPROM Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{ESW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{ESE}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{EBR}	–	–	–	5	us
EEPROM Programming Frequency	f_{PGM}	–	0.125	–	–	MHz
Endurance of Write/Erase	NE_{WE}	Sector Erase, Byte Write	100,000	–	–	cycles

Table 7.12 Internal Flash Rom Characteristics

NOTE)

1. The write/erase cycles of the internal EEPROM can be increased significantly if it is divided into smaller and used in turn.
2. Ex) If 128bytes are divided into 4 areas with 32bytes and the each area from 1st to 4th is used up to 100,000 cycles, the total erase/write is for 400,000 cycles.

7.13 Input/Output Capacitance

(T_A=-40°C ~ +85°C, VDD=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 7.13 Input/Output Capacitance

7.14 Recommended Circuit and Layout

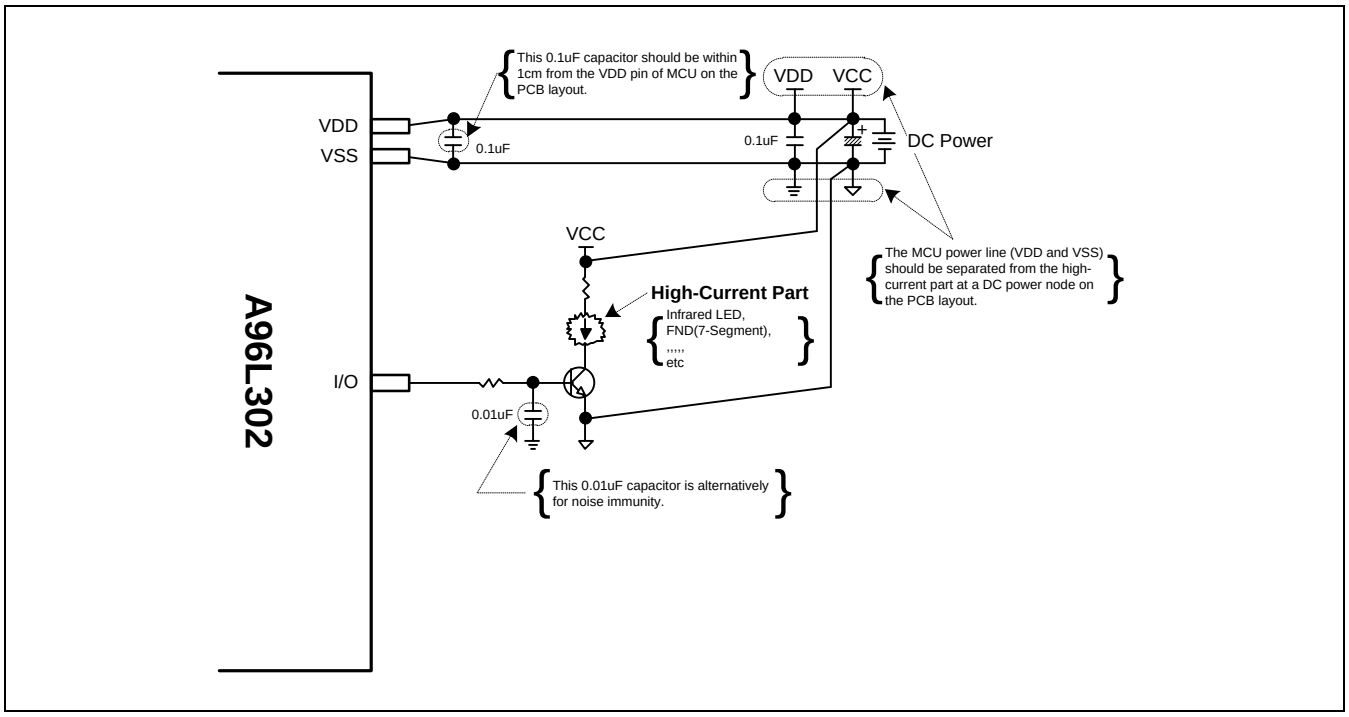


Figure 7.5 Recommended Circuit and Layout

7.15 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

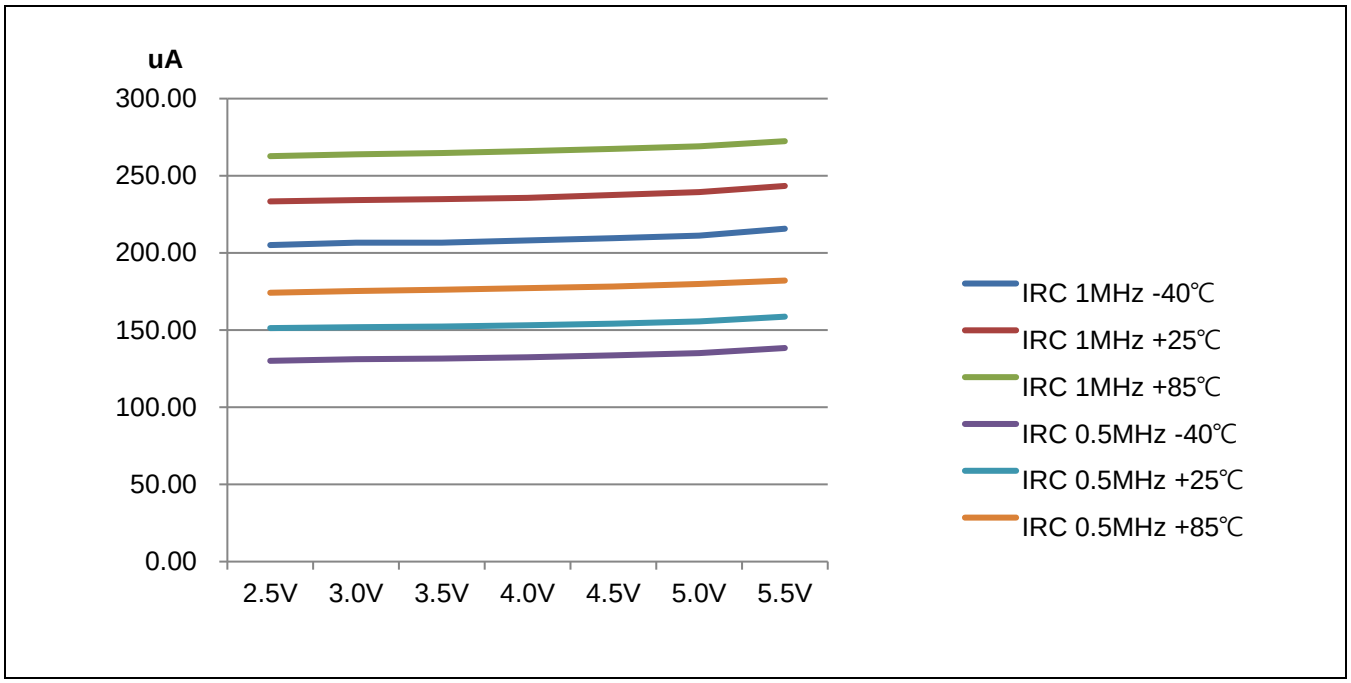


Figure 7.6 IRC RUN (IDD1) Current

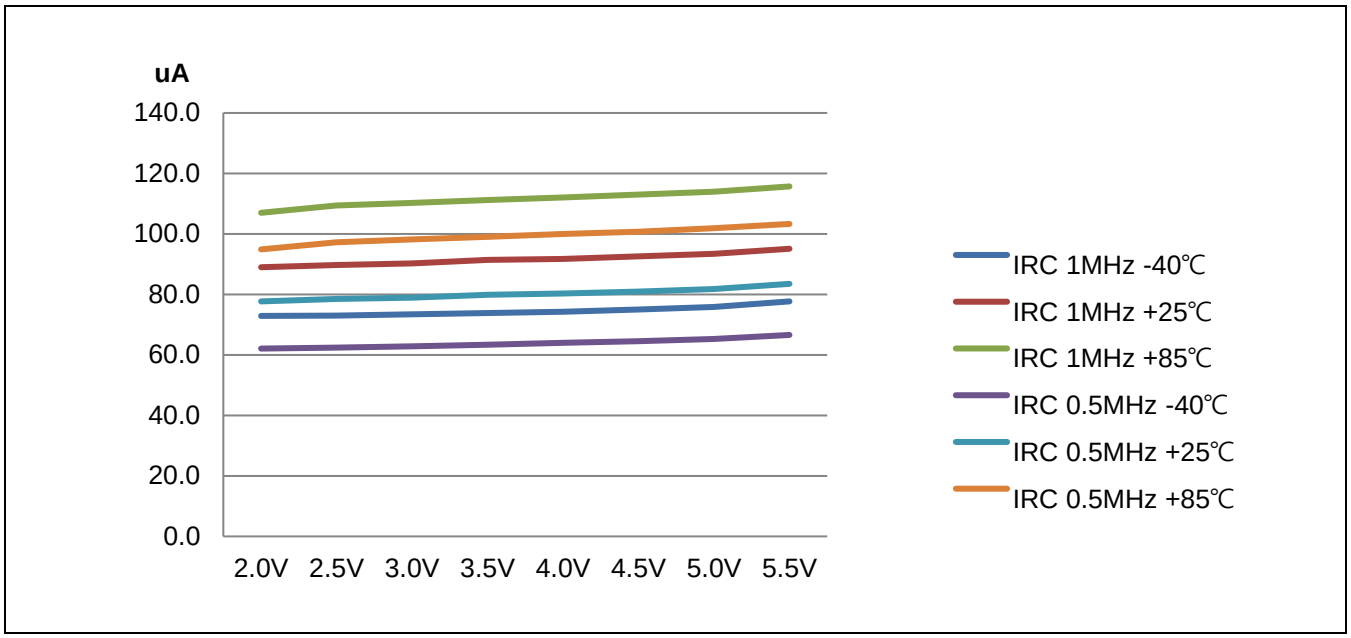


Figure 7.7 IRC IDLE (IDD2) Current

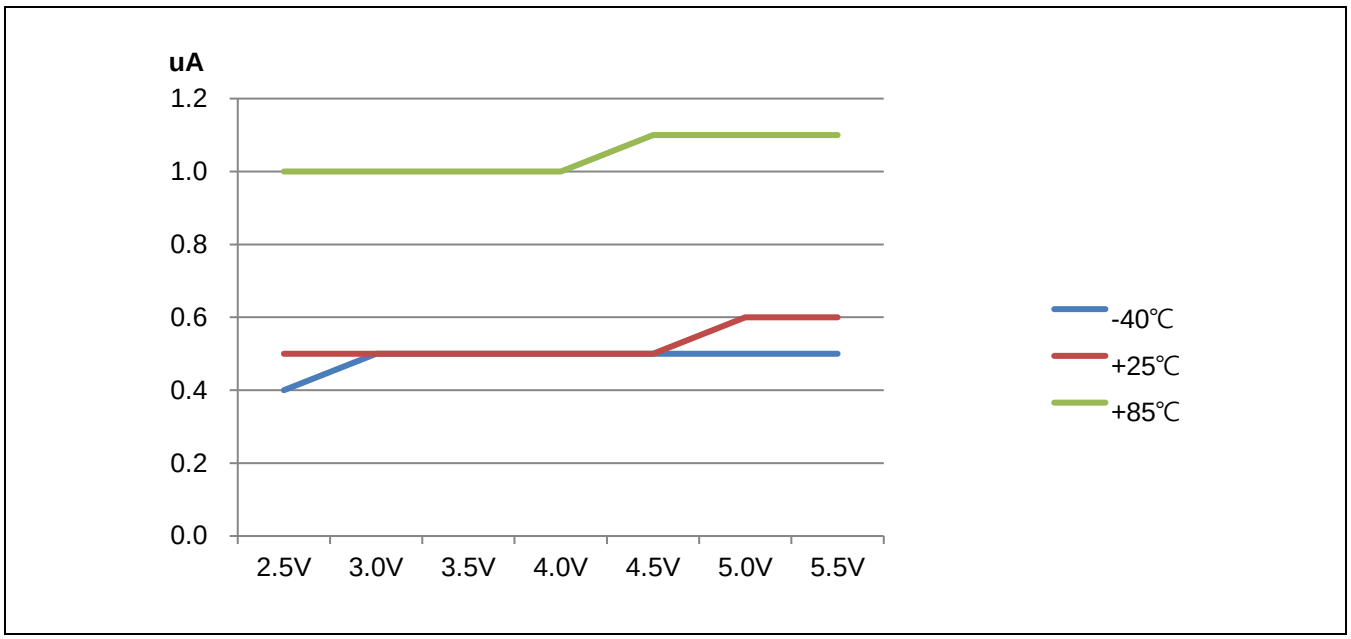


Figure 7.8 STOP (IDD5) Current

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