A96G150
Datasheet

16 MHz 8-bit A96G150 Microcontroller
64 Kbyte Flash memory, 2Kbyte EEPROM, 12-bit ADC,
6 Timers, USART, USI, High Current Port

Version 1.01

Features

Core
- 8-bit CISC M8051 core
  (8051 Compatible, 2 clocks per cycle)

64 KB On-Chip FLASH
- Endurance : 30,000 times
- In-system Programming (ISP)

2 KB EEPROM
- Endurance : 300,000 times
- Retention : 10 years

256 bytes IRAM / 2304 bytes XRAM

General Purpose I/O (GPIO)
- Normal I/O : 44 Port
  P0[7:0], P1[7:0], P2[7:0], P3[7:0]
  P4[5:0], P5[3:0]
- High sink current port : 8 ports P3[7:0]

Timer/Counter
- Basic Interval Timer (BIT) 8-bit × 1-ch
- Watchdog Timer (WDT) 8-bit × 1-ch
- 8-bit × 1-ch (T0)
- 16-bit × 5-ch (T1/T2/T3/T4/T5)

Programmable Pulse Generation
- Pulse generation (by T1/T2/T3/T4/T5)
- 8-bit PWM (by T0)

Watch Timer (WT)
- 3.91ms/0.25s/0.5s/1s /1min interval at
  32.768kHz

Buzzer
- 8-bit × 1-ch

USI0/1 (USART + SPI + I2C)
- 8-bit USART × 2-ch
- 8-bit SPI × 2-ch
- 8-bit I2C × 2-ch

USART2
- 8-bit USART × 1-ch
- 8-bit SPI × 1-ch
- Receiver Time Out(RTO)
- 0% Error Baud Rate

12-bit A/D Converter
- 15 Input channels

Power On Reset
- Reset release level (1.32V)

Low Voltage Reset
- 16 levels detect
  (1.61/1.68/1.77/1.88/2.00/2.13/2.28/2.46/2.68
  /2.81/3.06/3.21/3.56/3.73/3.91/4.25V)

Low Voltage Indicator
- 13 levels detect
  (1.88/2.00/2.13/2.28/2.46/2.68/2.81/3.06/3.21
  /3.56/3.73/ 3.91/4.25V)

LCD Driver
- 24 segments and 8 Common terminals
- Internal or external resistor bias
- 1/3, 1/4, 1/5, 1/6 and 1/8 duty selectable
- Resistor bias and 16 step contrast control

CRC

- CRC16
- Polynomial representations Normal : 0x8C81
- $f(x) = 1 + x^7 + x^{10} + x^{11} + x^{15} + x^{16}$

Interrupt Sources

- EINT40~47, EINT0, EINT1, EINT2, EINT3 (5)
- Timer(0/1/2/3/4/5) (6)
- WDT (1)
- BIT (1)
- WT (1)
- USART (RX, CRC)/TX (2)
- USI 2ch * RX/TX/I2C (6)
- ADC (1)
- LVI (1)

Internal RC Oscillator

- HSI 32MHz ±2.0% (TA=-40~ +85°C)
- HSI 32MHz ±3.0% (TA=-40~ +105°C)
- LSI 128kHz ±20% (TA= -40~ +85°C)
- LSI 128kHz ±30% (TA= -40~ +105°C)

Power Down Mode

- STOP, IDLE mode

Operating Voltage and Frequency

- 1.8V~ 5.5V (@32.768kHz Crystal)
- 2.4V~ 5.5V (@4 ~ 12MHz with Crystal)
- 1.8V~ 5.5V (@0.5 ~ 8.0MHz with Internal RC)
- 2.0V~ 5.5V (@0.5 ~ 16.0MHz with Internal RC)

Minimum Instruction Execution Time

- 125ns (@16MHz main clock)
- 61us (@ 32.768kHz sub clock)

Operating temperature

- –40 ~ +85℃, –40 ~ +105℃

Oscillator Type

- 4 ~ 12MHz Crystal or Ceramic for main clock
- 32.768kHz Crystal for sub clock

Package Type

- 44 LQFP 10x10 mm
- Pb-free package

Product selection table

Table 1. Device Summary

Part number	Flash	EEPROM	XRAM	IRAM	Timer (PWM)	Communication function		ADC 12-bit (channel)	GPIO	High current port	Package	Temp. range
						USI	USART					
A96G150SN	64KB	2KB	2304 bytes	256 bytes	6	2	1	15	42	8	44 LQFP	-40°C ~ 85°C
A96G150SN2	64KB	2KB	2304 bytes	256 bytes	6	2	1	15	42	8	44 LQFP	-40°C ~ 105°C

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1 Description

A96G150 is an advanced CMOS 8-bit microcontroller with 64Kbytes of FLASH. This is a powerful microcontroller which provides a highly flexible and cost-effective solution to many embedded control applications.

1.1 Device overview

In this section, features of A96G150 and peripheral counts are introduced.

Table 2. A96G150 Device Features and Peripheral Counts

Peripherals		Description
Core	CPU	8-bit CISC core (M8051, 2 clocks per cycle)
	Interrupt	Up to 23 peripheral interrupts supported. • EINT40 to 47, EINT0, EINT1, EINT2, EINT3 (5) • Timer (0/1/2/3/4/5) (6) • WDT (1) • BIT (1) • WT (1) • USART (Rx, CRC)/Tx (2) • USI 2-ch. *Rx/Tx/I2C (6) • ADC (1) • LVI (1)
Memory	ROM (FLASH) capacity	• 64 KB FLASH with self-read and write capability • In-system programming (ISP) • Endurance: 30,000times
	IRAM	256 bytes
	XRAM	2304 bytes
	EEPROM	• 2 KB • Endurance: 300,000 times at room temperature • Retention: 10 years
Programmable pulse generation		• Pulse generation (by T1/T2/T3/T4/T5) • 8-bit PWM (by T0)
Buzzer		8-bit × 1-ch
Minimum instruction execution time		• 125 ns (@ 16 MHz main clock) • 61 us (@ 32.768 kHz sub clock)
Power down mode		• STOP mode • IDLE mode

Table 2. A96G150 Device Features and Peripheral Counts (continued)

Peripherals		Description
General Purpose I/O (GPIO)		• Normal I/O: 42ports • High sink current port: 8 ports P3[7:0]
Reset	Power on reset	Reset release level: 1.2 V
	Low voltage reset	• 16 levels detect • 1.61 / 1.68 / 1.77 / 1.88 / 2.00 / 2.13 / 2.28 / 2.46 / 2.68 / 2.81 / 3.06 / 3.21 / 3.56 / 3.73 / 3.91 / 4.25V
Low voltage indicator		• 13 levels detect • 1.88 / 2.00 / 2.13 / 2.28 / 2.46 / 2.68 / 2.81 / 3.06 / 3.21 / 3.56 / 3.73 / 3.91 / 4.25V
Watch Timer (WT)		3.91 ms / 0.25 s / 0.5 s / 1 s / 1 min interval at 32.768 kHz
Timer/counter		• Basic interval timer (BIT) 8-bit x 1-ch. • Watchdog Timer (WDT) 8-bit x 1-ch. • 8-bit x 1-ch (T0), 16-bit x 5-ch (T1 / T2 / T3 / T4 / T5)
Communication function	USART2	• 8-bit USART x 1-ch or 8-bit SPI x 1-ch • Receiver timer out (RTO) • 0% error baud rate
	USI0/1	• USART + SPI + I2C • 8-bit USART x 2-ch or 8-bit SPI x 2-ch or I2C x 2-ch
12-bit A/D converter		15 input channels
Oscillator type		• 4 MHz to 12 MHz crystal or ceramic for main clock • 32.768 kHz Crystal for sub clock
LCD Driver		• 24 segments and 8 common terminals • Internal or external resistor bias • 4 Internal Resistors Selectable • 1/3, 1/4, 1/5, 1/6 and 1/8 duty selectable • Resistor Bias and 16-step contrast control
CRC		• CRC16 • Polynomial representations Normal : 0x8C81 $f_{(x)} = 1 + x^7 + x^{10} + x^{11} + x^{15} + x^{16}$

Table 2. A96G150 Device Features and Peripheral Counts (continued)

Peripherals	Description
Internal RC oscillator	• HSI 32MHz ±2.0% (T_A=-40~ +85°C) • HSI 32MHz ±3.0% (T_A=-40~ +105°C) • LSI 128kHz ±20% (T_A= -40~ +85°C) • LSI 128kHz ±30% (T_A= -40~ +105°C)
Operating voltage and frequency	• LVR (<1.8V) to 5.5V @ 32.768KHz with crystal • 2.4V to 5.5V @ 4MHz to 12MHz with crystal • LVR (<1.8V) to 5.5V @ 0.5MHz to 16MHz with internal RC
Operating temperature	-40℃ to +85℃, -40℃ to +105℃
Package	• Pb-free packages • 44 LQFP 1010

1.2 A96G150 block diagram

In this section, A96G150 device with peripherals are described in a block diagram.

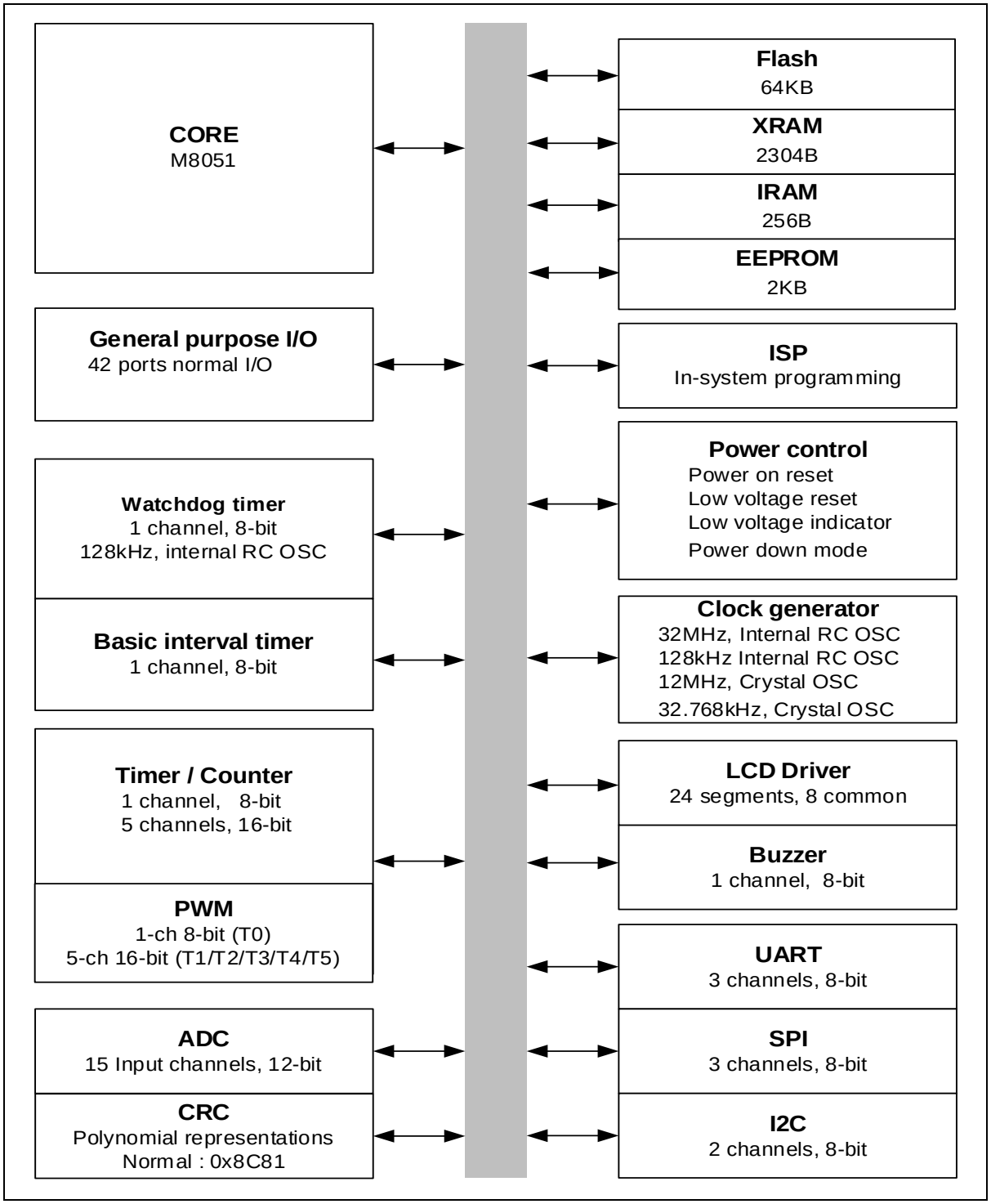
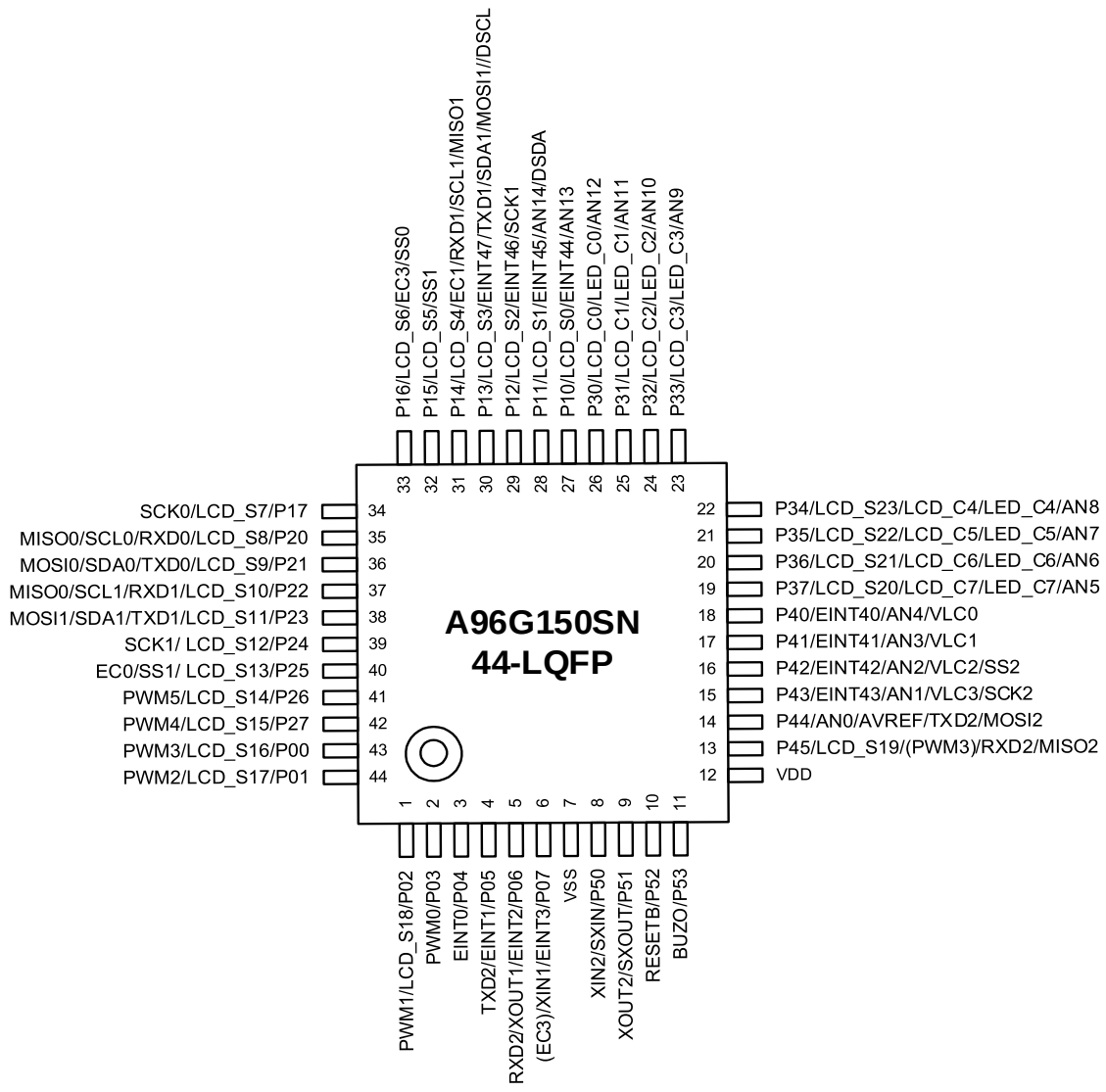


Figure 1. A96G150 Block Diagram

2 Pinouts and pin description

In this chapter, A96G150 device pinouts and pin descriptions are introduced.

2.1 Pinouts



NOTE: The programmer (E-PGM+, E-Gang4/6) uses P1[3], P1[1] pin as DSCL, DSDA.

Figure 2. A96G150 44LQFP-1010 Pin Assignment

2.2 Pin description

Table 3. Normal Pin Description

Pin no.	Pin name	I/O(1)	Description	Remark
44				
43	P00*	IOUS	Port 0 bit 0 Input/output	
	LCD_S16	O	LCD Segment Signal 16 Output	
	T3O	O	Timer 3 interval output	
	PWM3O	O	Timer 3 PWM output	
44	P01*	IOUS	Port 0 bit 1 Input/output	
	LCD_S17	O	LCD Segment Signal 17 Output	
	T2O	O	Timer 2 interval output	
	PWM2O	O	Timer 2 PWM output	
1	P02*	IOUS	Port 0 bit 2 Input/output	
	LCD_S18	O	LCD Segment Signal 18 Output	
	T1O	O	Timer 1 interval output	
	PWM1O	O	Timer 1 PWM output	
2	P03*	IOUS	Port 0 bit 3 Input/output	
	T0O	O	Timer 0 interval output	
	PWM0O	O	Timer 0 PWM output	
3	P04*	IOUS	Port 0 bit 4 Input/output	
	EINT0	I	External interrupt input ch-0	
4	P05*	IOUS	Port 0 bit 5 Input/output	
	EINT1	I	External interrupt input ch-1	
	TXD2	O	USART2 data transmit	
5	P06*	IOUS	Port 0 bit 6 Input/output	
	EINT2	I	External interrupt input ch-2	
	XOUT1	O	Main Oscillator Output ch-1	
	RXD2	I	USART2 data receive	
6	P07*	IOUS	Port 0 bit 7 Input/output	
	EINT3	I	External interrupt input ch-3	
	XIN1	I	Main Oscillator Input ch-1	
	EC3	I	Timer 3(Event Capture) input	

Table 3. Normal Pin Description (continue)

Pin no.	Pin name	I/O(1)	Description	Remark
44				
27	P10*	IOUS	Port 1 bit 0 Input/output	
	LCD_S0	O	LCD Segment Signal 0 Output	
	EINT44	I	External interrupt input ch-44	
	AN13	IA	ADC input ch-13	
28	P11*	IOUS	Port 1 bit 1 Input/output	
	LCD_S1	O	LCD Segment Signal 1 Output	
	EINT45	I	External interrupt input ch-45	
	AN14	IA	ADC input ch-14	
	DSDA	IOU	OCD debugger data input/output	Pull-up
29	P12*	IOUS	Port 1 bit 2 Input/output	
	LCD_S2	O	LCD Segment Signal 2 Output	
	EINT46	I	External interrupt input ch-46	
	SCK1	IO	USART1 clock signal	
30	P13*	IOUS	Port 1 bit 3 Input/output	
	LCD_S3	O	LCD Segment Signal 3 Output	
	EINT47	I	External interrupt input ch-47	
	TXD1	O	USART1 data transmit	
	SDA1	IO	I2C1 data signal	
	MOSI1	IO	USART1 SPI MOSI	
	DSCL	IOU	OCD debugger clock	Pull-up
31	P14*	IOUS	Port 1 bit 4 Input/output	
	LCD_S4	O	LCD Segment Signal 4 Output	
	EC1	I	Timer 1(Event Capture) input	
	RXD1	I	USART1 data receive	
	SCL1	IO	I2C1 clock signal	
	MISO1	IO	USART1 SPI MISO	
32	P15*	IOUS	Port 1 bit 5 Input/output	
	LCD_S5	O	LCD Segment Signal 5 Output	
	SS1	IO	USART1 slave select signal	
33	P16*	IOUS	Port 1 bit 6 Input/output	
	LCD_S6	O	LCD Segment Signal 6 Output	
	EC3	I	Timer 3(Event Capture) input	
	SS0	IO	USART0 slave select signal	
34	P17*	IOUS	Port 1 bit 7 Input/output	
	LCD_S7	O	LCD Segment Signal 7 Output	
	SCK0	IO	USART0 clock signal	

Table 3. Normal Pin Description (continue)

Pin no.	Pin name	I/O(1)	Description	Remark
44				
35	P20*	IOUS	Port 2 bit 0 Input/output	
	LCD_S8	O	LCD Segment Signal 8 Output	
	RXD0	I	USART0 data receive	
	SCL0	IO	I2C0 clock signal	
	MISO0	IO	USART0 SPI MISO	
36	P21*	IOUS	Port 2 bit 1 Input/output	
	LCD_S9	O	LCD Segment Signal 9 Output	
	TXD0	O	USART0 data transmit	
	SDA0	IO	I2C0 data signal	
	MOSI0	IO	USART0 SPI MOSI	
37	P22*	IOUS	Port 2 bit 2 Input/output	
	LCD_S10	O	LCD Segment Signal 10 Output	
	RXD1	I	USART1 data receive	
	SCL1	IO	I2C1 clock signal	
	MISO1	IO	USART1 SPI MISO	
38	P23*	IOU	Port 2 bit 3 Input /output	
	LCD_S11	O	LCD Segment Signal 11 Output	
	TXD1	O	USART1 data transmit	
	SDA1	IO	I2C1 data signal	
	MOSI1	IO	USART1 SPI MOSI	
39	P24*	IOU	Port 2 bit 4 Input /output	
	LCD_S12	O	LCD Segment Signal 12 Output	
	SCK1	IO	USART1 clock signal	
40	P25*	IOU	Port 2 bit 5 Input /output	
	LCD_S13	O	LCD Segment Signal 13 Output	
	EC0	I	Timer 0(Event Capture) input	
	SS1	IO	USART1 slave select signal	
41	P26*	IOU	Port 2 bit 6 Input /output	
	LCD_S14	O	LCD Segment Signal 14 Output	
	T5O	O	Timer 5 interval output	
	PWM5O	O	Timer 5 PWM output	
42	P27*	IOU	Port 2 bit 7 Input /output	
	LCD_S15	O	LCD Segment Signal 15 Output	
	T4O	O	Timer 4 interval output	
	PWM4O	O	Timer 4 PWM output	

Table 3. Normal Pin Description (continue)

Pin no.	Pin name	I/O(1)	Description	Remark
44				
26	P30*	IOUS	Port 3 bit 0 Input /output	
	LED_C0	O	High sink current ports	
	LCD_C0	O	LCD Common Signal 0 Output	
	AN12	IA	ADC input ch-12	
25	P31*	IOUS	Port 3 bit 1 Input /output	
	LED_C1	O	High sink current ports	
	LCD_C1	O	LCD Common Signal 1 Output	
	AN11	IA	ADC input ch-11	
24	P32*	IOUS	Port 3 bit 2 Input /output	
	LED_C2	O	High sink current ports	
	LCD_C2	O	LCD Common Signal 2 Output	
	AN10	IA	ADC input ch-10	
23	P33*	IOUS	Port 3 bit 3 Input /output	
	LED_C3	O	High sink current ports	
	LCD_C3	O	LCD Common Signal 3 Output	
	AN9	IA	ADC input ch-9	
22	P34*	IOUS	Port 3 bit 4 Input /output	
	LED_C4	O	High sink current ports	
	LCD_C4	O	LCD Common Signal 4 Output /	
	LCD_S23	O	LCD Segment Signal 23 Output	
	AN8	IA	ADC input ch-8	
21	P35*	IOUS	Port 3 bit 5 Input /output	
	LED_C5	O	High sink current ports	
	LCD_C5	O	LCD Common Signal 5 Output	
	LCD_S22	O	LCD Segment Signal 22 Output	
	AN7	IA	ADC input ch-7	
20	P36*	IOUS	Port 3 bit 6 Input/output	
	LED_C6	O	High sink current ports	
	LCD_C6	O	LCD Common Signal 6 Output	
	LCD_S21	O	LCD Segment Signal 21 Output	
	AN6	IA	ADC input ch-6	
19	P37*	IOUS	Port 3 bit 7 Input/output	
	LED_C7	O	High sink current ports	
	LCD_C7	O	LCD Common Signal 7 Output	
	LCD_S20	O	LCD Segment Signal 20 Output	
	AN5	IA	ADC input ch-5	

Table 3. Normal Pin Description (continue)

Pin no.	Pin name	I/O(1)	Description	Remark
44				
18	P40*	IOUS	Port 4 bit 0 Input/output	
	EINT40	I	External interrupt input ch-40	
	AN4	IA	ADC input ch-4	
	VLC0	IA	External LCD Voltage bias 0	
17	P41*	IOUS	Port 4 bit 1 Input/output	
	EINT41	I	External interrupt input ch-41	
	AN3	IA	ADC input ch-3	
	VLC1	IA	External LCD Voltage bias 1	
16	P42*	IOUS	Port 4 bit 2 Input/output	
	EINT42	I	External interrupt input ch-42	
	AN2	IA	ADC input ch-2	
	VLC2	IA	External LCD Voltage bias 2	
	SS2	IO	USART2 slave select signal	
15	P43*	IOUS	Port 4 bit 3 Input/output	
	EINT43	I	External interrupt input ch-43	
	AN1	IA	ADC input ch-1	
	VLC3	IA	External LCD Voltage bias 3	
	XCK2	IO	USART2 clock signal	
14	P44*	IOUC	Port 4 bit 4 Input/output	
	AN0	IA	ADC input ch-0	
	AVREF	P	A/D converter reference voltage	
	MOSI2	IO	USART2 SPI MOSI	
	TXD2	O	USART2 data transmit	
13	P45*	IOUC	Port 4 bit 5 Input/output	
	LCD_S19	O	LCD Segment Signal 19 Output	
	T3O	O	Timer 3 interval output	
	PWM3O	O	Timer 3 PWM output	
	MISO2	IO	USART2 SPI MISO	
	RXD2	I	USART2 data receive	

Table 3. Normal Pin Description (continue)

Pin no.	Pin name	I/O(1)	Description	Remark
44				
8	P50*	IOUS	Port 5 bit 0 Input/output	
	XIN2	I	Main Oscillator Input ch-2	
	SXIN	I	Sub Oscillator Input	
9	P51*	IOUS	Port 5 bit 1 Input/output	
	XOUT2	O	Main Oscillator Output ch-2	
	SXOUT	O	Sub Oscillator Output	
10	P52*	IOUS	Port 5 bit 2 Input/output	
	RESETB	IU	Reset pin	Pull-up
11	P53*	IOUS	Port 5 bit 3 Input/output	
	BUZO	O	Buzzer output	

NOTES:

1. The P52/RESETB pin is configured as one of the P52 and RESETB pin by the “CONFIGURE OPTION.”
2. If the P11/LCD_S1/EINT45/AN14/DSDA and P13/LCD_S3/EINT47/DSCL pins are connected to the programmer during power-on reset, the pins are automatically configured as In-system programming pins.
3. The P11/LCD_S1/EINT45/AN14/DSDA and P13/LCD_S3/EINT47/DSCL pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.
4. The P50/XIN2/SXIN, P51/XOUT2/SXOUT, P06/RXD2/XOUT/EINT2, and P07/XIN/EINT3 pins are configured as a function pin by software control.
5. (1) I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
6. The * means ‘Selected pin function after reset condition’.

3 Port structures

In this chapter, two port structures are introduced in Figure 3 and Figure 4 regarding general purpose I/O port and external interrupt I/O port respectively.

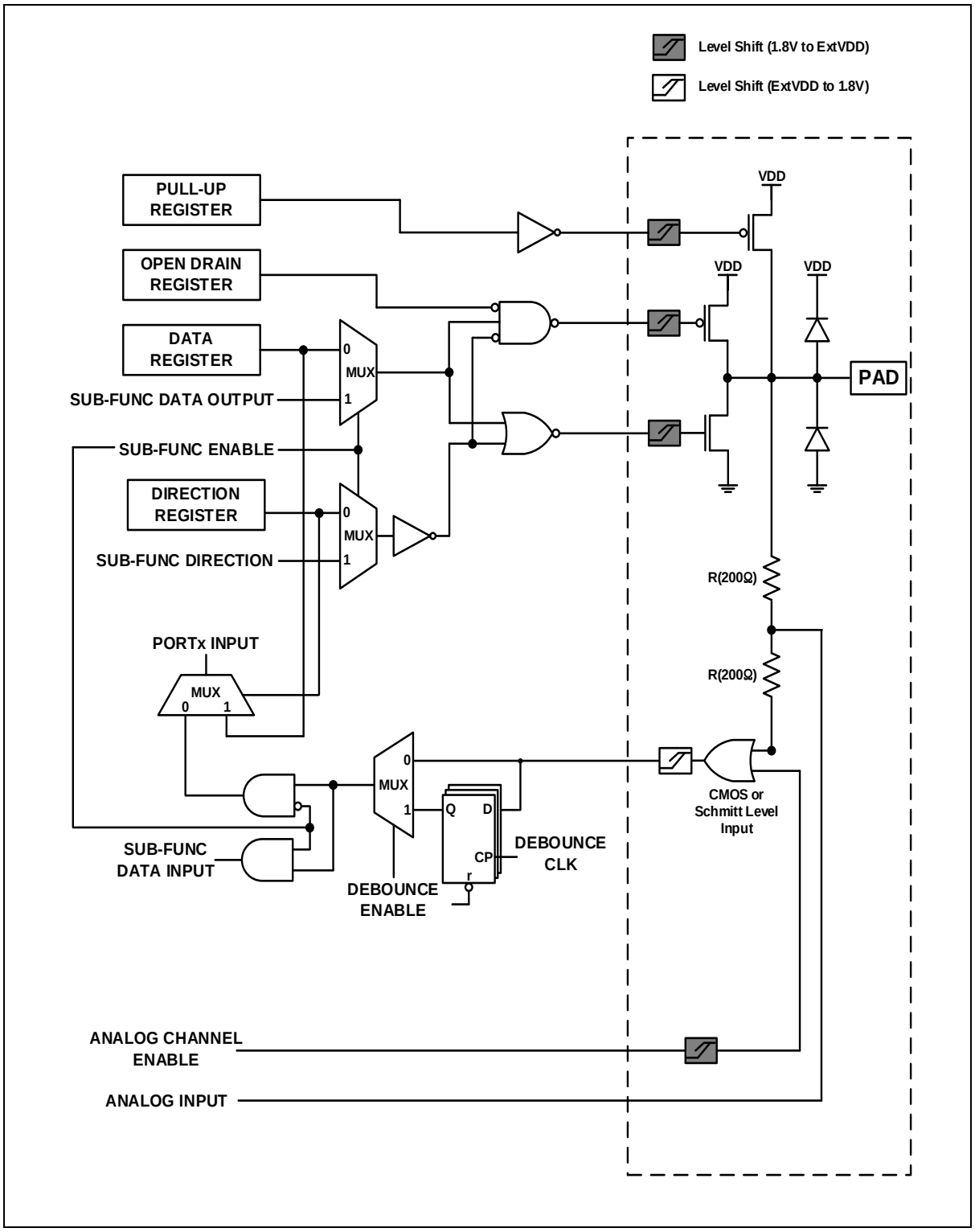


Figure 3. General Purpose I/O Port

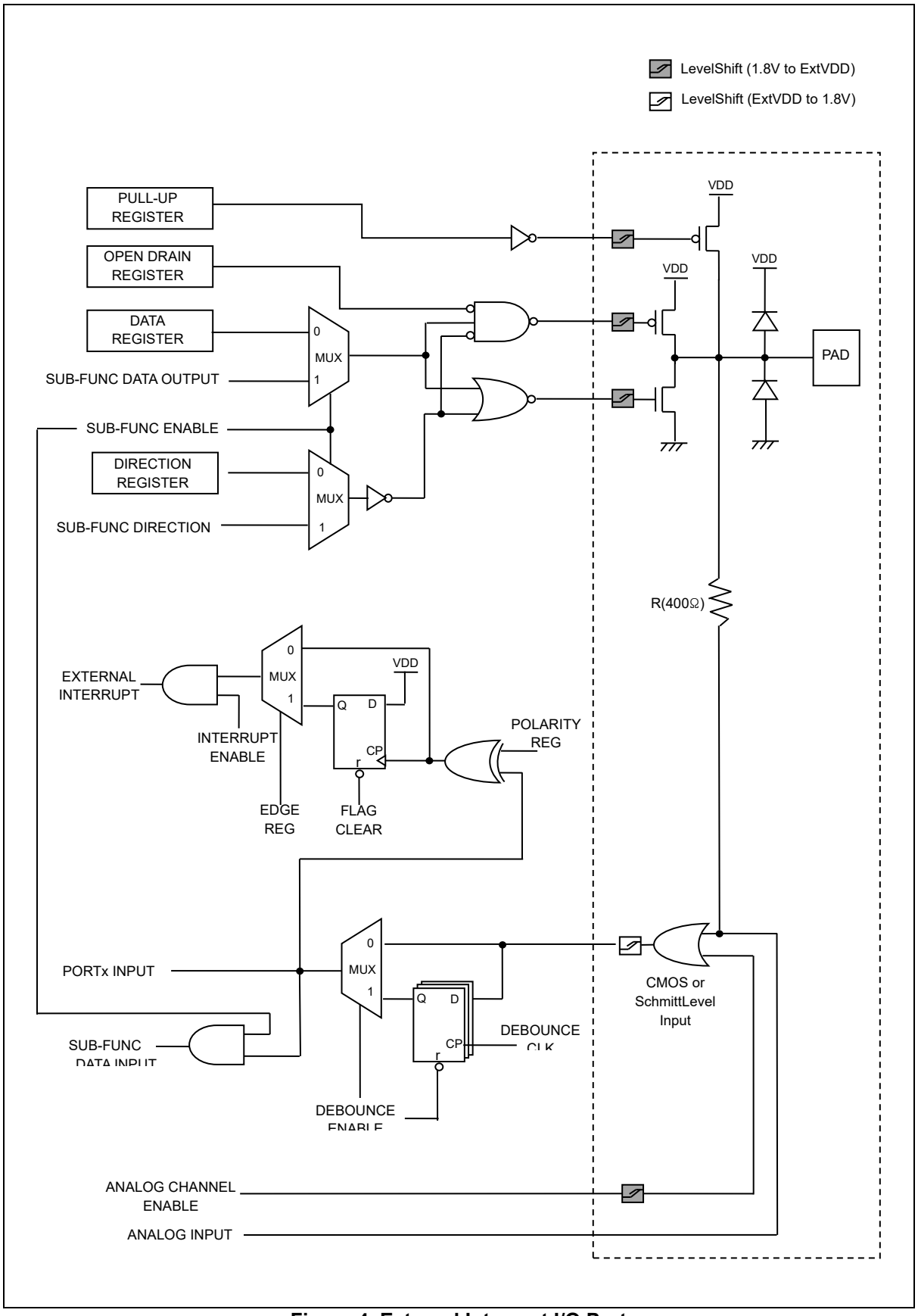


Figure 4. External Interrupt I/O Port

4 Central Processing Unit (CPU)

This is based on Mentor Graphics M8051EW core, and it improves code efficiency and performance.

4.1 Architecture and registers

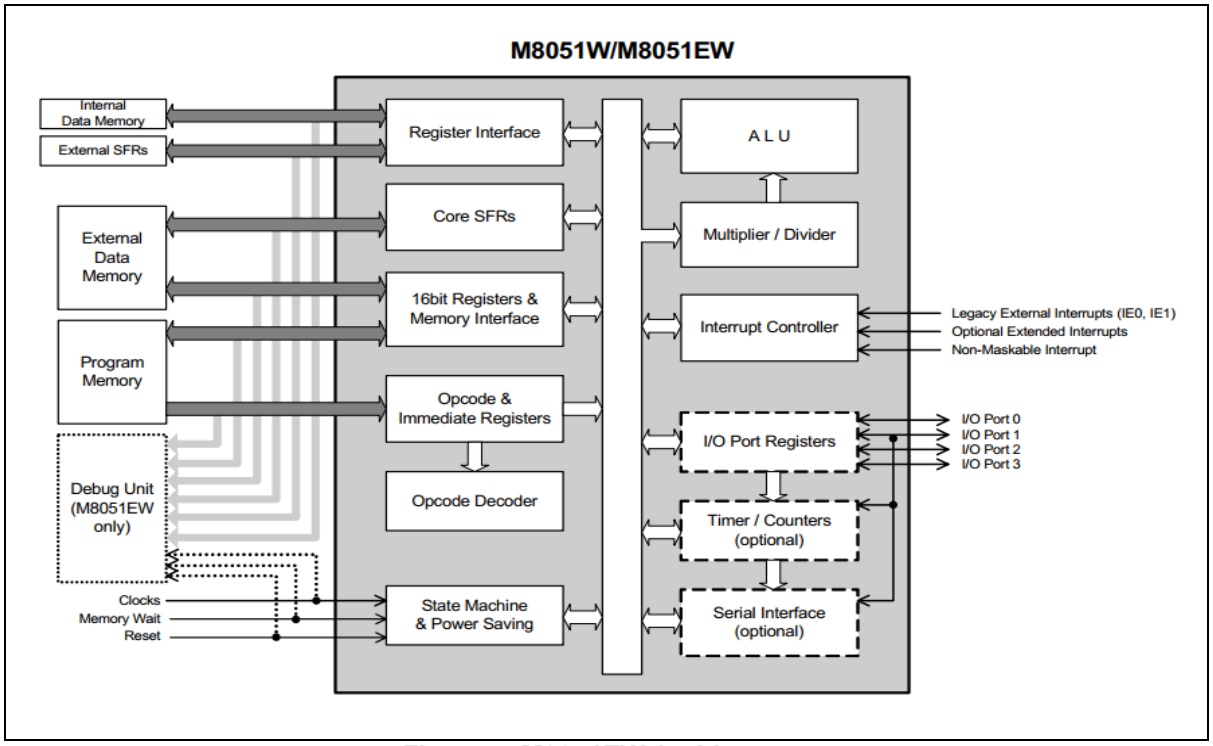


Figure 5. M8051EW Architecture

- Two clocks per machine cycle architecture
- Debug support of OCD and OCD II
- Separate program and external data memory interfaces or a single multiplexed interface
- Support for synchronous and asynchronous Program, External Data & Internal Data Memory
- Wait states support for slow Program and External Data Memory
- 16-bit Data Memory address is generated through the DPTR(Data Point register).
- 16-bit program counter - capable of addressing up to Flash size in Each device
- A single data pointer, two memory-mapped data pointers, or 2, 4 or 8 banked data pointers
- Support 2 or 4 level of priority scheme – Up to 24 maskable Interrupt sources
- External Special Function Register(SFR) are memory mapped into Direct Memory between addresses 80 hex and FF hex

4.2 Addressing

- 6 addressing modes
- Direct addressing
- Indirect addressing
- Register addressing
- Register specific addressing
- Immediate DATA
- Indexed addressing

4.3 Instruction set

If you need an Instruction table, please refer to Appendix.

- Instructions are either 1, 2 or 3 bytes long as listed in the ‘Bytes’
- Each instruction takes either 1, 2 or 4 machine cycles to execute.
  1 machine cycle comprises 2 CCLK clock cycles.
- An M8051EW-specific instruction MOVC @(DPTR++), A is provided to enable software to be downloaded into Program Memory where this is implemented as RAM. This instruction can also be used subsequently to modify contents of the Program Memory RAM.
- Arithmetic Instruction
- Logical Instruction
- Internal data memory
- External data memory
- Unconditional Jumps
- Subroutine calls and returns
- Conditional Jumps
- Boolean Instructions
- Flag

5 Memory organization

A96G150 addresses two separate address memory spaces:

- Program memory
- Data memory

By means of this logical separation of the memory, 8-bit CPU address can access the Data Memory more rapidly. 16-bit Data Memory address is generated through the DPTR register.

A96G150 provides on-chip 64Kbytes of the ISP type flash program memory, which readable and writable. Internal data memory (IRAM) is 256bytes and it includes the stack area. External data memory (XRAM) is 2304bytes and internal EEPROM is 2Kbytes.

5.1 Program memory

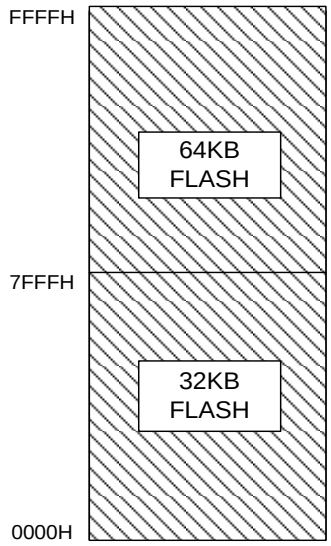
A 16-bit program counter is capable of addressing up to 64Kbytes, and A96G150 has just 64Kbytes program memory space.

Figure 6 shows a map of the lower part of the program memory.

After reset, CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in the program memory. An interrupt causes the CPU to jump to the corresponding location, where it commences execution of the service routine.

An external interrupt 11, for example, is assigned to location 000BH. If the external interrupt 11 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within an interval of 8-bytes.

Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.



NOTE: The 64Kbytes includes the Interrupt Vector Region.

Figure 6. Program Memory Map

5.2 Data memory

Internal data memory space is divided into three blocks, which are generally referred to as lower 128bytes, upper 128bytes, and SFR space. Internal data memory addresses are always one byte wide, which implies an address space of 256bytes. In fact, the addressing modes for the internal data memory can accommodate up to 384bytes by using a simple trick. Direct addresses higher than 7FH access one memory space, while indirect addresses higher than 7FH access a different memory space. Thus as shown in Figure 7, the upper 128bytes and SFR space occupy the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128bytes of RAM are present in all 8051 devices as mapped in Figure 8. The lowest 32bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128bytes can be accessed by either direct or indirect addressing. The upper 128bytes of RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

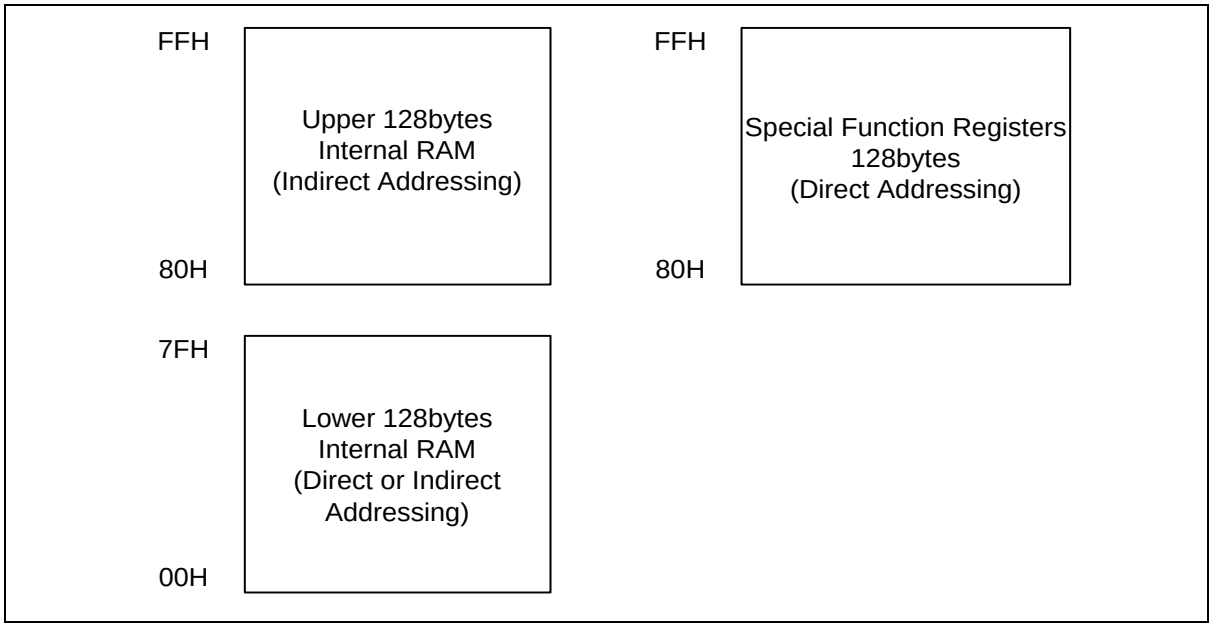


Figure 7. Data Memory Map

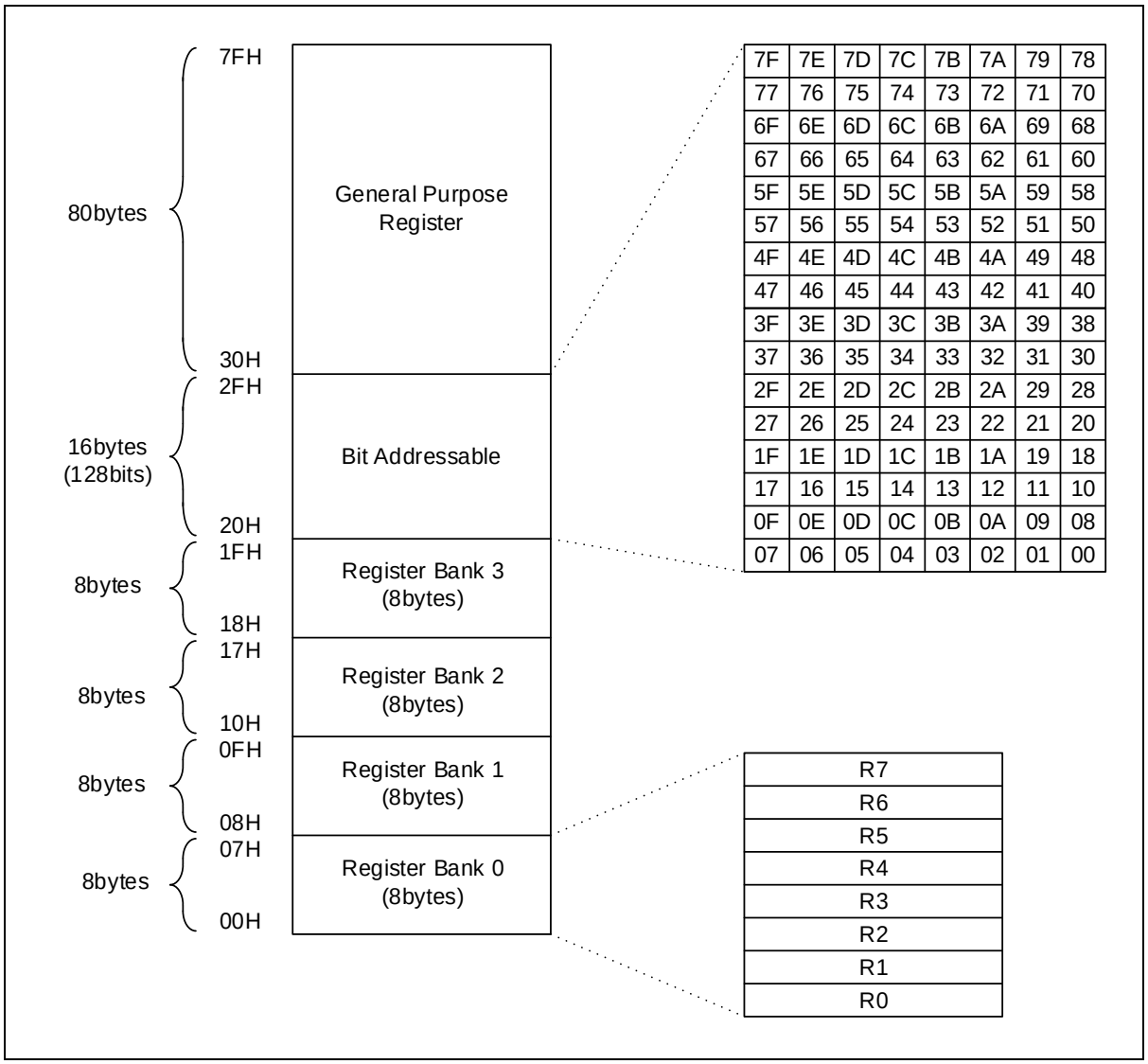


Figure 8. Lower 128bytes of RAM

5.3 EEPROM data memory and External data memory

A96G150 has 2048bytes of EEPROM, 2304bytes of XRAM and XSFR. This area has no relation with RAM/FLASH. It can be read and written to through SFR with 8-bit unit.

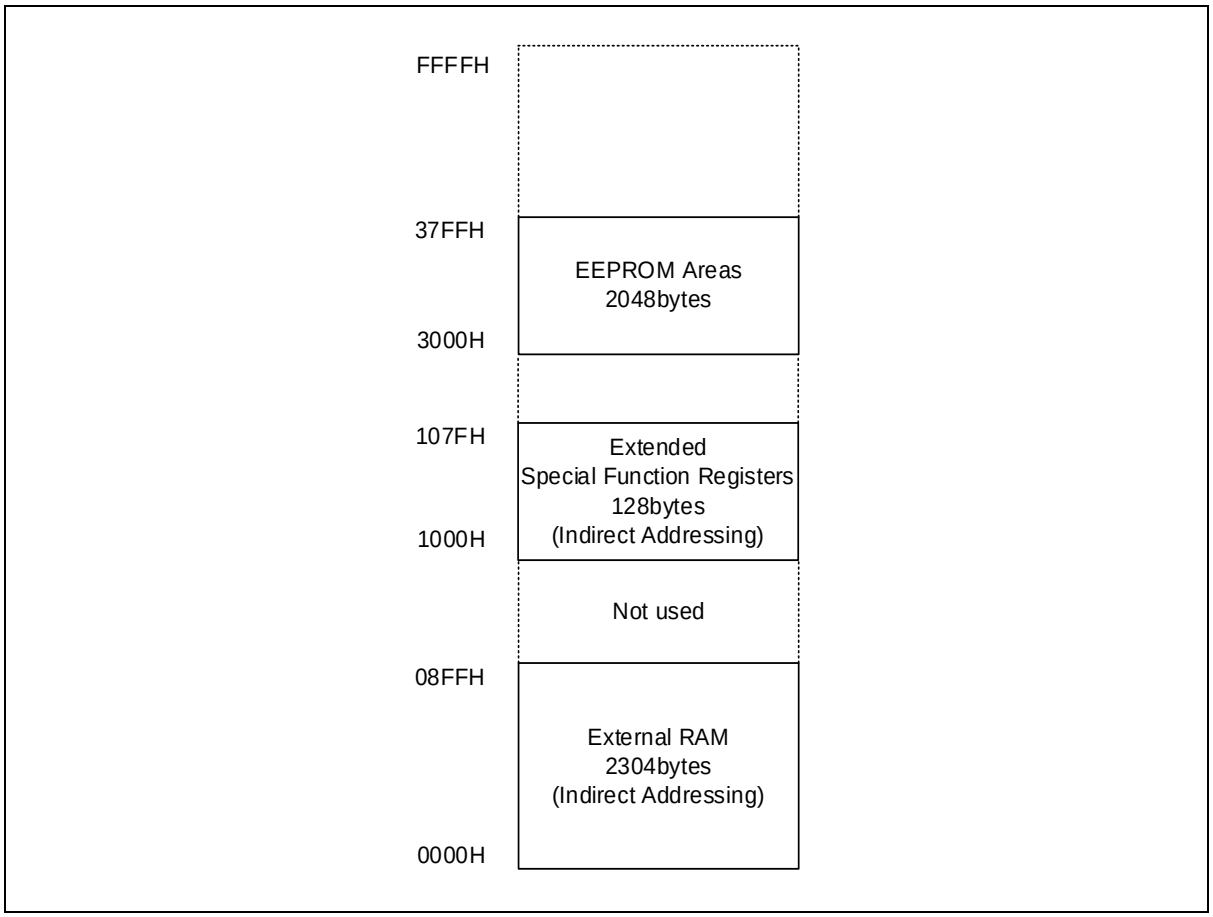


Figure 9. XDATA Memory Area

5.4 SFR map

5.4.1 SFR map summary

Table 4. SFR Map Summary

—	Reserved
	M8051 compatible

	00H/8H[1]	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	P4FSRL	P4FSRH	–	UBAUD	UDATA	–	P5FSR
0F0H	B	USI1ST1	USI1ST2	USI1BD	USI1SDHR	USI1DR	USI1SCLR	USI1SCHR
0E8H	RSTFR	USI1CR1	USI1CR2	USI1CR3	USI1CR4	USI1SAR	P3FSRL	P3FSRH
0E0H	ACC	USI0ST1	USI0ST2	USI0BD	USI0SDHR	USI0DR	USI0SCLR	USI0SCHR
0D8H	LVRCR	USI0CR1	USI0CR2	USI0CR3	USI0CR4	USI0SAR	P0DB	P14DB
0D0H	PSW	P5IO	P0FSRL	P0FSRH	P1FSRL	P1FSRH	P2FSRL	P2FSRH
0C8H	OSCCR	P4IO	–	UCTRL1	UCTRL2	UCTRL3	–	USTAT
0C0H	EIFLAG0	P3IO	T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH
0B8H	IP	P2IO	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH
0B0H	P5	P1IO	T0CR	T0CNT	T0DR/ T0CDR	P1SSR	–	–
0A8H	IE	IE1	IE2	IE3	P0PU	P1PU	P2PU	P3PU
0A0H	P4	P0IO	EO	P4PU	EIPOL0L	EIPOL0H	EIFLAG1	EIPOL1
98H	P3	–	–	–	ADCCRL	ADCCRH	ADCDRL	ADCDRH
90H	P2	P0OD	P1OD	P2OD	P4OD	P5PU	WTCR	BUZCR
88H	P1	WTDR/ WTCNT	SCCR	BITCR	BITCNT	WDTCR	WDTDR/ WDTCNT	BUZDR
80H	P0	SP	DPL	DPH	DPL1	DPH1	LVICR	PCON

NOTE: 00H/8H, these registers are bit-addressable.

Table 5. XSFR Map Summary

	00H/8H[1]	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
1078H	—	CRC_ADDR_START_H	CRC_ADDR_START_M	CRC_ADDR_START_L	CRC_ADDR_END_H	CRC_ADDR_END_M	CRC_ADDR_END_L	—
1070H	CRC_CON	—	CRC_H	CRC_L	CRC_MNT_H	CRC_MNT_L	—	—
1068H	—	—	—	—	—	—	—	—
1060H	LCD_DR16	LCD_DR17	LCD_DR18	LCD_DR19	LCD_DR20	LCD_DR21	LCD_DR22	LCD_DR23
1058H	LCD_DR8	LCD_DR9	LCD_DR10	LCD_DR11	LCD_DR12	LCD_DR13	LCD_DR14	LCD_DR15
1050H	LCD_DR0	LCD_DR1	LCD_DR2	LCD_DR3	LCD_DR4	LCD_DR5	LCD_DR6	LCD_DR7
1048H	LCDCR	LCDBCCRH	LCDBCCRL	LCDBSSRH	LCDBSSRL	—	—	—
1040H	—	—	—	—	—	—	—	—
1038H	XTFLSR	—	—	—	—	—	—	—
1030H	—	—	—	—	—	—	—	—
1028H	FEARH	FEARM	FEARL	FEDR	FETR	—	—	—
1020H	FEMR	FECR	FESR	FETCR	FEARM1	FEARL1	—	—
1018H	UCTRL4	FPCR	RTOCH	RTOCL	—	—	—	—
1010H	T5CRH	T5CRL	T5ADRH	T5ADRL	T5BDRH	T5BDRL	—	—
1008H	T4CRH	T4CRL	T4ADRH	T4ADRL	T4BDRH	T4BDRL	—	—
1000H	T3CRH	T3CRL	T3ADRH	T3ADRL	T3BDRH	T3BDRL	—	—

5.4.2 SFR map

Table 6. SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Low Voltage Indicator Control Register	LVICR	R/W	–	–	0	0	0	0	0	0
87H	Power Control Register	PCON	R/W	0	–	–	–	0	0	0	0
88H	P1 Data Register	P1	R/W	0	0	0	0	0	0	0	0
89H	Watch Timer Data Register	WTDR	W	0	1	1	1	1	1	1	1
	Watch Timer Counter Register	WTCNT	R	–	0	0	0	0	0	0	0
8AH	System and Clock Control Register	SCCR	R/W	–	–	–	–	–	–	0	0
8BH	Basic Interval Timer Control Register	BITCR	R/W	0	1	0	0	0	1	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watchdog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	0	0
8EH	Watchdog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1
	Watchdog Timer Counter Register	WDTCNT	R	0	0	0	0	0	0	0	0
8FH	BUZZER Data Register	BUZDR	R/W	1	1	1	1	1	1	1	1
90H	P2 Data Register	P2	R/W	0	0	0	0	0	0	0	0
91H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
92H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0
93H	P2 Open-drain Selection Register	P2OD	R/W	0	0	0	0	0	0	0	0
94H	P4 Open-drain Selection Register	P4OD	R/W	0	0	0	0	0	0	0	0
95H	P5 Pull-up Resistor Selection Register	P5PU	R/W	–	–	0	0	0	0	0	0
96H	Watch Timer Control Register	WTCR	R/W	0	–	–	0	0	0	0	0
97H	BUZZER Control Register	BUZCR	R/W	–	–	–	–	–	0	0	0
98H	P3 Data Register	P3	R/W	0	0	0	0	0	0	0	0
9CH	A/D Converter Control Low Register	ADCCRL	R/W	0	0	0	0	0	0	0	0
9DH	A/D Converter Control High Register	ADCCRH	R/W	0	0	0	0	0	0	0	1
9EH	A/D Converter Data Low Register	ADCDRL	R	x	x	x	x	x	x	x	x
9FH	A/D Converter Data High Register	ADCDRH	R	x	x	x	x	x	x	x	x

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
A0H	P4 Data Register	P4	R/W	0	0	0	0	0	0	0	0
A1H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A3H	P4 Pull-up Resistor Selection Register	P4PU	R/W	0	0	0	0	0	0	0	0
A4H	External Interrupt Polarity 0 Low Register	EIPOL0L	R/W	0	0	0	0	0	0	0	0
A5H	External Interrupt Polarity 0 High Register	EIPOL0H	R/W	0	0	0	0	0	0	0	0
A6H	External Interrupt Flag 1 Register	EIFLAG1	R/W	0	0	–	–	0	0	0	0
A7H	External Interrupt Polarity 1 Register	EIPOL1	R/W	0	0	0	0	0	0	0	0
A8H	Interrupt Enable Register	IE	R/W	0	–	0	0	0	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	0	0	0	0	0
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	0	0	0	0	0	0
ABH	Interrupt Enable Register 3	IE3	R/W	–	–	0	0	0	0	0	0
ACH	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
ADH	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
AEH	P2 Pull-up Resistor Selection Register	P2PU	R/W	0	0	0	0	0	0	0	0
AFH	P3 Pull-up Resistor Selection Register	P3PU	R/W	0	0	0	0	0	0	0	0
B0H	P5 Data Register	P5	R/W	–	–	0	0	0	0	0	0
B1H	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0
B2H	Timer 0 Control Register	T0CR	R/W	0	–	0	0	0	0	0	0
B3H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0
B4H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1
	Timer 0 Capture Data Register	T0CDR	R	0	0	0	0	0	0	0	0
B5H	P1 SEG Option Selection Register	P1SSR	R/W	0	0	0	0	0	0	0	0
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	P2 Direction Register	P2IO	R/W	0	0	0	0	0	0	0	0
BAH	Timer 1 Control Low Register	T1CRL	R/W	0	0	0	0	–	0	0	0
BBH	Timer 1 Counter High Register	T1CRH	R/W	0	–	0	0	–	–	–	0
BCH	Timer 1 A Data Low Register	T1ADRL	R/W	1	1	1	1	1	1	1	1
BDH	Timer 1 A Data High Register	T1ADRH	R/W	1	1	1	1	1	1	1	1
BEH	Timer 1 B Data Low Register	T1BDRL	R/W	1	1	1	1	1	1	1	1
BFH	Timer 1 B Data High Register	T1BDRH	R/W	1	1	1	1	1	1	1	1

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
C0H	External Interrupt Flag 0 Register	EIFLAG0	R/W	0	0	0	0	0	0	0	0
C1H	P3 Direction Register	P3IO	R/W	0	0	0	0	0	0	0	0
C2H	Timer 2 Control Low Register	T2CRL	R/W	0	0	0	0	–	0	–	0
C3H	Timer 2 Control High Register	T2CRH	R/W	0	–	0	0	–	–	–	0
C4H	Timer 2 A Data Low Register	T2ADRL	R/W	1	1	1	1	1	1	1	1
C5H	Timer 2 A Data High Register	T2ADRH	R/W	1	1	1	1	1	1	1	1
C6H	Timer 2 B Data Low Register	T2BDRL	R/W	1	1	1	1	1	1	1	1
C7H	Timer 2 B Data High Register	T2BDRH	R/W	1	1	1	1	1	1	1	1
C8H	Oscillator Control Register	OSCCR	R/W	–	0	1	0	1	0	0	0
C9H	P4 Direction Register	P4IO	R/W	0	0	0	0	0	0	0	0
CBH	USART Control Register 1	UCTRL1	R/W	0	0	0	0	0	0	0	0
CCH	USART Control Register 2	UCTRL2	R/W	0	0	0	0	0	0	0	0
CDH	USART Control Register 3	UCTRL3	R/W	0	0	0	0	–	0	0	0
CFH	USART Status Register	USTAT	R/W	1	0	0	0	0	0	0	0
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	P5 Direction Register	P5IO	R/W	–	–	–	–	0	0	0	0
D2H	P0 Function Selection Low Register	P0FSRL	R/W	0	0	0	0	0	0	0	0
D3H	P0 Function Selection High Register	P0FSRH	R/W	0	0	0	0	0	0	0	0
D4H	P1 Function Selection Low Register	P1FSRL	R/W	0	0	0	0	0	0	0	0
D5H	P1 Function Selection High Register	P1FSRH	R/W	0	0	0	0	0	0	0	0
D6H	P2 Function Selection Low Register	P2FSRL	R/W	0	0	0	0	0	0	0	0
D7H	P2 Function Selection High Register	P2FSRH	R/W	0	0	0	0	0	0	0	0
D8H	Low Voltage Reset Control Register	LVRCR	R/W	–	–	–	0	0	0	0	0
D9H	USI0 Control Register 1	USI0CR1	R/W	0	0	0	0	0	0	0	0
DAH	USI0 Control Register 2	USI0CR2	R/W	0	0	0	0	0	0	0	0
DBH	USI0 Control Register 3	USI0CR3	R/W	0	0	0	0	0	0	0	0
DCH	USI0 Control Register 4	USI0CR4	R/W	0	–	0	0	0	0	0	0
DDH	USI0 Slave Address Register	USI0SAR	R/W	0	0	0	0	0	0	0	0
DEH	P0 De-bounce Enable Register	P0DB	R/W	0	0	0	0	0	0	0	0
DFH	P1/P4 De-bounce Enable Register	P14DB	R/W	0	0	0	0	0	0	0	0

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	USI0 Status Register 1	USI0ST1	R/W	0	0	0	0	–	0	0	0
E2H	USI0 Status Register 2	USI0ST2	R	0	0	0	0	0	0	0	0
E3H	USI0 Baud Rate Generation Register	USI0BD	R/W	1	1	1	1	1	1	1	1
E4H	USI0 SDA Hold Time Register	USI0SHDR	R/W	0	0	0	0	0	0	0	1
E5H	USI0 Data Register	USI0DR	R/W	0	0	0	0	0	0	0	0
E6H	USI0 SCL Low Period Register	USI0SCLR	R/W	0	0	1	1	1	1	1	1
E7H	USI0 SCL High Period Register	USI0SCHR	R/W	0	0	1	1	1	1	1	1
E8H	Reset Flag Register	RSTFR	R/W	1	x	0	0	x	–	–	–
E9H	USI1 Control Register 1	USI1CR1	R/W	0	0	0	0	0	0	0	0
EAH	USI1 Control Register 2	USI1CR2	R/W	0	0	0	0	0	0	0	0
EBH	USI1 Control Register 3	USI1CR3	R/W	0	0	0	0	0	0	0	0
ECH	USI1 Control Register 4	USI1CR4	R/W	0	–	–	0	0	–	0	0
EDH	USI1 Slave Address Register	USI1SAR	R/W	0	0	0	0	0	0	0	0
EEH	P3 Function Selection Low Register	P3FSRL	R/W	0	0	0	0	0	0	0	0
EFH	P3 Function Selection High Register	P3FSRH	R/W	0	0	0	0	0	0	0	0
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	USI1 Status Register 1	USI1ST1	R/W	0	0	0	0	–	0	0	0
F2H	USI1 Status Register 2	USI1ST2	R	0	0	0	0	0	0	0	0
F3H	USI1 Baud Rate Generation Register	USI1BD	R/W	1	1	1	1	1	1	1	1
F4H	USI1 SDA Hold Time Register	USI1SHDR	R/W	0	0	0	0	0	0	0	1
F5H	USI1 Data Register	USI1DR	R/W	0	0	0	0	0	0	0	0
F6H	USI1 SCL Low Period Register	USI1SCLR	R/W	0	0	1	1	1	1	1	1
F7H	USI1 SCL High Period Register	USI1SCHR	R/W	0	0	1	1	1	1	1	1
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
F9H	P4 Function Selection Low Register	P4FSRL	R/W	0	0	0	0	0	0	0	0
FAH	P4 Function Selection High Register	P4FSRH	R/W	0	0	0	0	0	0	0	0
FCH	USART Baud Rate Generation Register	UBAUD	R/W	1	1	1	1	1	1	1	1
FDH	USART Data Register	UDATA	R/W	0	0	0	0	0	0	0	0
FFH	P5 Function Selection Register	P5FSR	R/W	0	0	0	0	0	0	0	0

Table 7. XSFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
1000H	Timer 3 Control High Register	T3CRH	R/W	0	–	0	0	–	–	–	0
1001H	Timer 3 Control Low Register	T3CRL	R/W	0	0	0	0	–	0	0	0
1002H	Timer 3 A Data High Register	T3ADRH	R/W	1	1	1	1	1	1	1	1
1003H	Timer 3 A Data Low Register	T3ADRL	R/W	1	1	1	1	1	1	1	1
1004H	Timer 3 B Data High Register	T3BDRH	R/W	1	1	1	1	1	1	1	1
1005H	Timer 3 B Data Low Register	T3BDRL	R/W	1	1	1	1	1	1	1	1
1008H	Timer 4 Control High Register	T4CRH	R/W	0	–	0	0	–	–	–	0
1009H	Timer 4 Control Low Register	T4CRL	R/W	0	0	0	0	–	0	–	0
100AH	Timer 4 A Data High Register	T4ADRH	R/W	1	1	1	1	1	1	1	1
100BH	Timer 4 A Data Low Register	T4ADRL	R/W	1	1	1	1	1	1	1	1
100CH	Timer 4 B Data High Register	T4BDRH	R/W	1	1	1	1	1	1	1	1
100DH	Timer 4 B Data Low Register	T4BDRL	R/W	1	1	1	1	1	1	1	1
1010H	Timer 5 Control High Register	T5CRH	R/W	0	–	0	0	–	–	–	0
1011H	Timer 5 Control Low Register	T5CRL	R/W	0	0	0	0	–	0	–	0
1012H	Timer 5 A Data High Register	T5ADRH	R/W	1	1	1	1	1	1	1	1
1013H	Timer 5 A Data Low Register	T5ADRL	R/W	1	1	1	1	1	1	1	1
1014H	Timer 5 B Data High Register	T5BDRH	R/W	1	1	1	1	1	1	1	1
1015H	Timer 5 B Data Low Register	T5BDRL	R/W	1	1	1	1	1	1	1	1
1018H	USART Control Register 4	UCTRL4	R/W	–	–	–	0	0	0	0	0
1019H	USART Floating Point Counter	FPCR	R/W	0	0	0	0	0	0	0	0
101AH	Receiver Time Out Counter High Register	RTOCH	R	0	0	0	0	0	0	0	0
101BH	Receiver Time Out Counter Low Register	RTOCL	R	0	0	0	0	0	0	0	0
1020H	Flash Mode Register	FEMR	R/W	0	–	0	0	0	0	0	0
1021H	Flash Control Register	FECR	R/W	0	–	0	0	0	0	1	1
1022H	Flash Status Register	FESR	R/W	1	–	–	–	0	0	0	0
1023H	Flash Time Control Register	FETCR	R/W	0	0	0	0	0	0	0	0
1024H	Flash Address Middle Register 1	FEARM1	R/W	0	0	0	0	0	0	0	0
1025H	Flash Address Low Register 1	FEARL1	R/W	0	0	0	0	0	0	0	0
1028H	Flash Address High Register	FEARH	R/W	0	0	0	0	0	0	0	0
1029H	Flash Address Middle Register	FEARM	R/W	0	0	0	0	0	0	0	0
102AH	Flash Address Low Register	FEARL	R/W	0	0	0	0	0	0	0	0
1038H	Main Crystal OSC Filter Selection Register	XTFLSR	R/W	–	–	0	0	0	0	0	0

Table 7. XSFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
1048H	LCD Driver Control Register	LCDCR	R/W	0	0	0	0	0	0	0	0
1049H	LCD Automatic Bias and Contrast Control High Register	LCDBCCRH	R/W	0	0	–	0	–	0	0	0
104AH	LCD Automatic Bias and Contrast Control Low Register	LCDBCCRL	R/W	–	–	0	–	0	0	0	0
104BH	LCD source Selection High Register	LCDBSSRH	R/W	0	–	–	–	0	–	0	0
104CH	LCD source Selection Low Register	LCDBSSRL	R/W	0	0	0	0	0	0	0	0
1050H	LCD Display Data Register 0	LCDDR0	R/W	0	0	0	0	0	0	0	0
1051H	LCD Display Data Register 1	LCDDR1	R/W	0	0	0	0	0	0	0	0
1052H	LCD Display Data Register 2	LCDDR2	R/W	0	0	0	0	0	0	0	0
1053H	LCD Display Data Register 3	LCDDR3	R/W	0	0	0	0	0	0	0	0
1054H	LCD Display Data Register 4	LCDDR4	R/W	0	0	0	0	0	0	0	0
1055H	LCD Display Data Register 5	LCDDR5	R/W	0	0	0	0	0	0	0	0
1056H	LCD Display Data Register 6	LCDDR6	R/W	0	0	0	0	0	0	0	0
1057H	LCD Display Data Register 7	LCDDR7	R/W	0	0	0	0	0	0	0	0
1058H	LCD Display Data Register 8	LCDDR8	R/W	0	0	0	0	0	0	0	0
1059H	LCD Display Data Register 9	LCDDR9	R/W	0	0	0	0	0	0	0	0
105AH	LCD Display Data Register 10	LCDDR10	R/W	0	0	0	0	0	0	0	0
105BH	LCD Display Data Register 11	LCDDR11	R/W	0	0	0	0	0	0	0	0
105CH	LCD Display Data Register 12	LCDDR12	R/W	0	0	0	0	0	0	0	0
105DH	LCD Display Data Register 13	LCDDR13	R/W	0	0	0	0	0	0	0	0
105EH	LCD Display Data Register 14	LCDDR14	R/W	0	0	0	0	0	0	0	0
105FH	LCD Display Data Register 15	LCDDR15	R/W	0	0	0	0	0	0	0	0
1060H	LCD Display Data Register 16	LCDDR16	R/W	0	0	0	0	0	0	0	0
1061H	LCD Display Data Register 17	LCDDR17	R/W	0	0	0	0	0	0	0	0
1062H	LCD Display Data Register 18	LCDDR18	R/W	0	0	0	0	0	0	0	0
1063H	LCD Display Data Register 19	LCDDR19	R/W	0	0	0	0	0	0	0	0
1064H	LCD Display Data Register 20	LCDDR20	R/W	0	0	0	0	0	0	0	0
1065H	LCD Display Data Register 21	LCDDR21	R/W	0	0	0	0	0	0	0	0
1066H	LCD Display Data Register 22	LCDDR22	R/W	0	0	0	0	0	0	0	0
1067H	LCD Display Data Register 23	LCDDR23	R/W	0	0	0	0	0	0	0	0

Table 7. XSFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
1070H	CRC Control Register	CRC_CON	R/W	0	0	0	0	0	0	0	0
1072H	CRC High Register	CRC_H	R/W	0	0	0	0	0	0	0	0
1073H	CRC Low Register	CRC_L	R/W	0	0	0	0	0	0	0	0
1074H	CRC Monitor High Register	CRC_MNT_H	R/W	0	0	0	0	0	0	0	0
1075H	CRC Monitor Low Register	CRC_MNT_L	R/W	0	0	0	0	0	0	0	0
1079H	CRC Start Address High Register	CRC_ADDR_START_H	R/W	–	–	–	–	–	–	–	0
107AH	CRC Start Address Middle Register	CRC_ADDR_START_M	R/W	0	0	0	0	0	0	0	0
107BH	CRC Start Address Low Register	CRC_ADDR_START_L	R/W	0	0	0	0	0	0	0	0
107CH	CRC End Address High Register	CRC_ADDR_END_H	R/W	–	–	–	–	–	–	–	0
107DH	CRC End Address Middle Register	CRC_ADDR_END_M	R/W	0	0	0	0	0	0	0	0
107EH	CRC End Address Low Register	CRC_ADDR_END_L	R/W	0	0	0	0	0	0	0	0

5.4.3 Compiler compatible SFR

ACC (Accumulator Register): E0H

7	6	5	4	3	2	1	0
ACC							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

ACC	Accumulator

B (B Register): F0H

7	6	5	4	3	2	1	0
B							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

B	B Register

SP (Stack Pointer): 81H

7	6	5	4	3	2	1	0
SP							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 07H

SP	Stack Pointer

DPL (Data Pointer Register Low): 82H

7	6	5	4	3	2	1	0
DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPL	Data Pointer Low

DPH (Data Pointer Register High): 83H

7	6	5	4	3	2	1	0
DPH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPH	Data Pointer High

DPL1 (Data Pointer Register Low 1): 84H

7	6	5	4	3	2	1	0
DPL1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPL1	Data Pointer Low 1

DPH1 (Data Pointer Register High 1): 85H

7	6	5	4	3	2	1	0
DPH1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

DPH1	Data Pointer High 1

PSW (Program Status Word Register): D0H

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

CY	Carry Flag
AC	Auxiliary Carry Flag
F0	General Purpose User-Definable Flag
RS1	Register Bank Select bit 1
RS0	Register Bank Select bit 0
OV	Overflow Flag
F1	User-Definable Flag
P	Parity Flag. Set/Cleared by hardware each instruction cycle to indicate an odd/even number of ‘1’ bits in the accumulator

EO (Extended Operation Register): A2H

7	6	5	4	3	2	1	0
–	–	–	TRAP_EN	–	DPSEL2	DPSEL1	DPSEL0
–	–	–	R/W	–	R/W	R/W	R/W

Initial value: 00H

TRAP_EN	Select the Instruction **(Keep always ‘0’)**.			
	0	Select MOVC @(DPTR++), A		
	1	Select Software TRAP Instruction		
DPSEL[2:0]	Select Banked Data Pointer Register			
	DPSEL2	DPSEL1	SPSEL0	Description
	0	0	0	DPTR0
	0	0	1	DPTR1
	Reserved			

6 I/O ports

A96G150 has ten groups of I/O ports (P0 ~ P5). Each port can be easily configured by software as I/O pin, internal pull up and open-drain pin to meet various system configurations and design requirements. P0 includes a function that can generate interrupt signals according to state of a pin.

6.1 Port description

6.1.1 P0 port description

P0 is an 8-bit I/O port. P0 control registers consist of P0 data register (P0), P0 direction register (P0IO), debounce enable register (P0DB), P0 pull-up resistor selection register (P0PU), and P0 open-drain selection register (P0OD). Refer to the port function selection registers for the P0 function selection.

6.1.2 P1 port description

P1 is an 8-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), debounce enable register (P14DB), P1 pull-up resistor selection register (P1PU), andP1 open-drain selection register (P1OD). Refer to the port function selection registers for the P1 function selection.

6.1.3 P2 port description

P2 is an 8-bit I/O port. P2 control registers consist of P2 data register (P2), P2 direction register (P2IO), P2 pull-up resistor selection register (P2PU) andP2 open-drain selection register (P2OD). Refer to the port function selection registers for the P2 function selection.

6.1.4 P3 port description

P3 is an 8-bit I/O port. P3 control registers consist of P3 data register (P3), P3 direction register (P3IO) and P3 pull-up resistor selection register (P3PU). Refer to the port function selection registers for the P3 function selection.

6.1.5 P4 port description

P4 is a 6-bit I/O port. P4 control registers consist of P4 data register (P4), P4 direction register (P4IO), P4 pull-up resistor selection register (P4PU) andP4 open-drain selection register (P4OD). Refer to the port function selection registers for the P4 function selection.

6.1.6 P5 port description

P5 is a 4-bit I/O port. P5 control registers consist of P5 data register (P5), P5 direction register (P5IO) and P5 pull-up resistor selection register (P5PU). Refer to the port function selection registers for the P5 function selection.

7 Interrupt controller

A96G150 supports up to 23 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. In addition, they have four levels of priority assigned to themselves.

A non-maskable interrupt source is always enabled with a higher priority than any other interrupt sources, and is not controllable by software.

Interrupt controller of A96G150 has following features:

- Request receive from the 23 interrupt sources
- 6 groups of priority
- 4 levels of priority
- Multi Interrupt possibility
- A request of higher priority level is served first, when multiple requests of different priority levels are received simultaneously.
- Each interrupt source can be controlled by EA bit and each IEx bit
- Interrupt latency of 3 to 9 machine cycles in single interrupt system

A non-maskable interrupt is always enabled, while maskable interrupts are enabled through four pairs of interrupt enable registers (IE, IE1, IE2, and IE3). Each bit of IE, IE1, IE2, IE3 register individually enables/disables the corresponding interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to ‘0’, all interrupts are disabled: when EA is set to ‘1’, interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to ‘0’ jumping to an interrupt service vector and set to ‘1’ executing the [RETI] instruction. The A96G150 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP and IP1.

Default interrupt mode is level-trigger mode basically, but if needed, it is possible to change to edge-trigger mode.

Figure 10 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority of a group is set by two bits of interrupt priority registers (one bit from IP, another one from IP1). Interrupt service routine serves higher priority interrupt first. If two requests of different priority levels are received simultaneously, the request of higher priority level is served prior to the lower one.

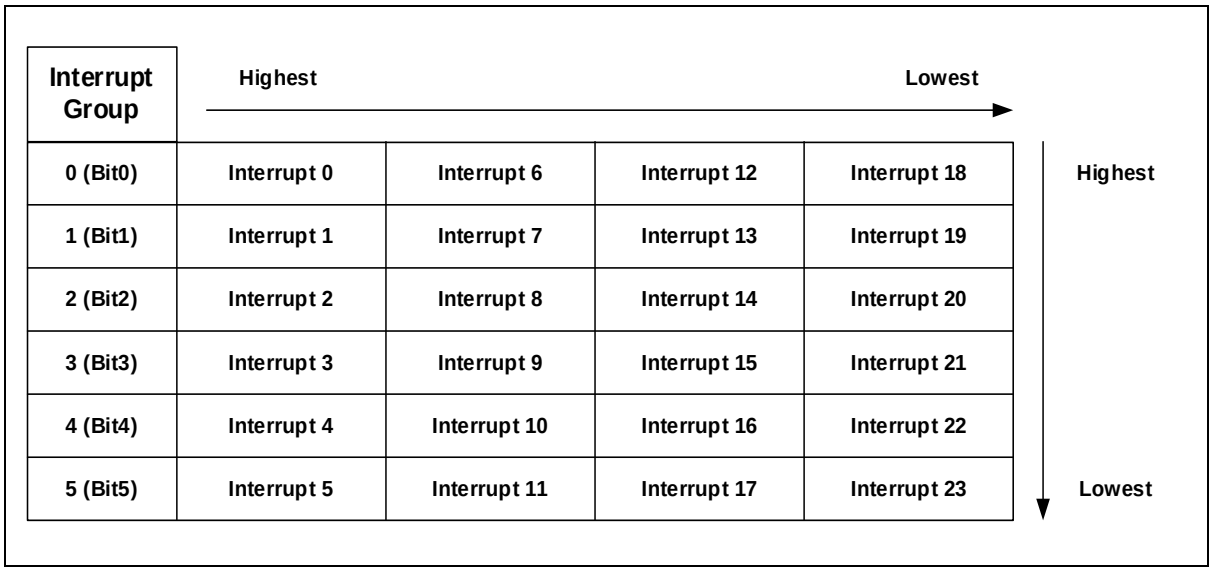
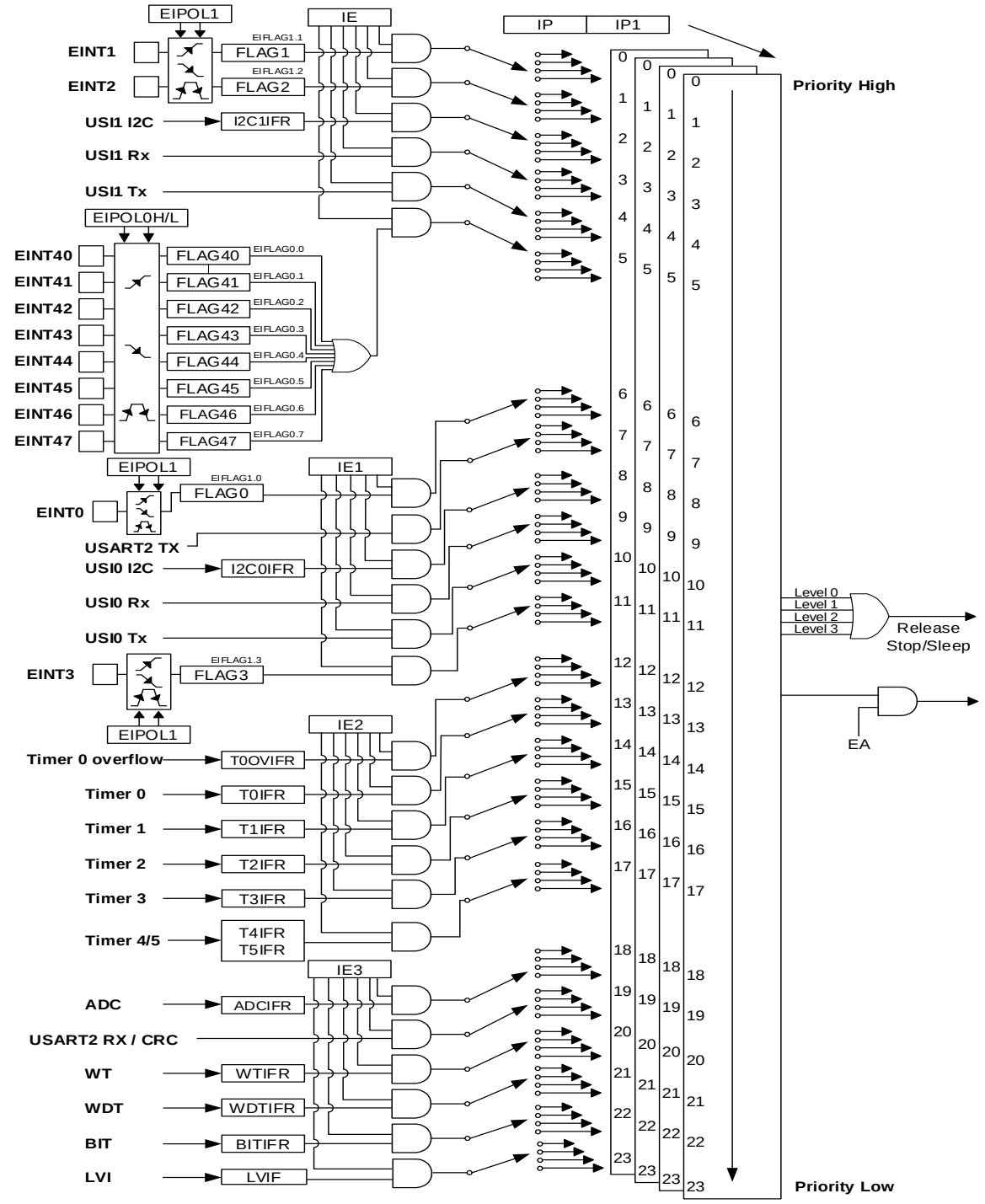


Figure 10. Interrupt Group Priority Level

7.1 Block diagram



NOTES:

1. The release signal for stop/idle mode may be generated by all interrupt sources which are enabled without reference to the priority level.
2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

Figure 11. Interrupt Controller Block Diagram

7.2 Interrupt vector table

Interrupt controller of A96G150 supports 24 interrupt sources as shown in Table 8. When interrupt is served, long call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have their own priority order.

Table 8. Interrupt Vector Address Table

Interrupt Source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector Address
Hardware Reset	RESETB	—	0	Non-Maskable	0000H
External Interrupt 1	INT0	IE.0	1	Maskable	0003H
External Interrupt 2	INT1	IE.1	2	Maskable	000BH
USI1 I2C Interrupt	INT2	IE.2	3	Maskable	0013H
USI1 Rx Interrupt	INT3	IE.3	4	Maskable	001BH
USI1 Tx Interrupt	INT4	IE.4	5	Maskable	0023H
External Interrupt 40 - 47	INT5	IE.5	6	Maskable	002BH
External Interrupt 0	INT6	IE1.0	7	Maskable	0033H
USART2 TX Interrupt	INT7	IE1.1	8	Maskable	003BH
USI0 I2C Interrupt	INT8	IE1.2	9	Maskable	0043H
USI0 Rx Interrupt	INT9	IE1.3	10	Maskable	004BH
USI0 Tx Interrupt	INT10	IE1.4	11	Maskable	0053H
External Interrupt 3	INT11	IE1.5	12	Maskable	005BH
T0 Overflow Interrupt	INT12	IE2.0	13	Maskable	0063H
T0 Match Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Match Interrupt	INT14	IE2.2	15	Maskable	0073H
T2 Match Interrupt	INT15	IE2.3	16	Maskable	007BH
T3 Match Interrupt	INT16	IE2.4	17	Maskable	0083H
T4/T5 Match Interrupt	INT17	IE2.5	18	Maskable	008BH
ADC Interrupt	INT18	IE3.0	19	Maskable	0093H
USART2 RX / CRC Interrupt	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
LVI Interrupt	INT23	IE3.5	24	Maskable	00BBH

For maskable interrupt execution, EA bit must set ‘1’ and specific interrupt must be enabled by writing ‘1’ to associated bit in the IEx. If an interrupt request is received, the specific interrupt request flag is set to ‘1’. And it remains ‘1’ until CPU accepts interrupt. If the interrupt is served, the interrupt request flag will be cleared automatically.

8 Clock generator

As shown in Figure 12, a clock generator produces basic clock pulses which provide a system clock for CPU and peripheral hardware.

It contains main/sub-frequency clock oscillator. The main/sub clock can operate easily by attaching a crystal between the XIN1/XIN2/SXIN and XOUT1/XOUT2/SXOUT pin, respectively. The main/sub clock can be also obtained from the external oscillator. For this, it is necessary to place external clock signal into the XIN1/XIN2/SXIN pin and open XOUT1/XOUT2/SXOUT pin.

Default system clock is 1MHz INT-RC Oscillator. To stabilize the system internally, 128KHz LOW INT-RC oscillator on POR is recommended.

Oscillators in the clock generator are introduced in the followings:

- Calibrated high internal RC oscillator (32MHz)
  - HSIRC OSC/2 (16MHz, default system clock)
  - HSIRC OSC/4 (8MHz)
  - HSIRC OSC/8 (4MHz)
  - HSIRC OSC/16 (2MHz)
  - HSIRC OSC/32 (1MHz)
  - HSIRC OSC/64 (0.5MHz)
- Main crystal oscillator (4~12MHz)
- Sub-crystal Oscillator (32.768kHz)
- Internal LSIRC oscillator (128kHz)

8.1 Clock generator block diagram

In this section, a clock generator of A96G150 is described in a block diagram.

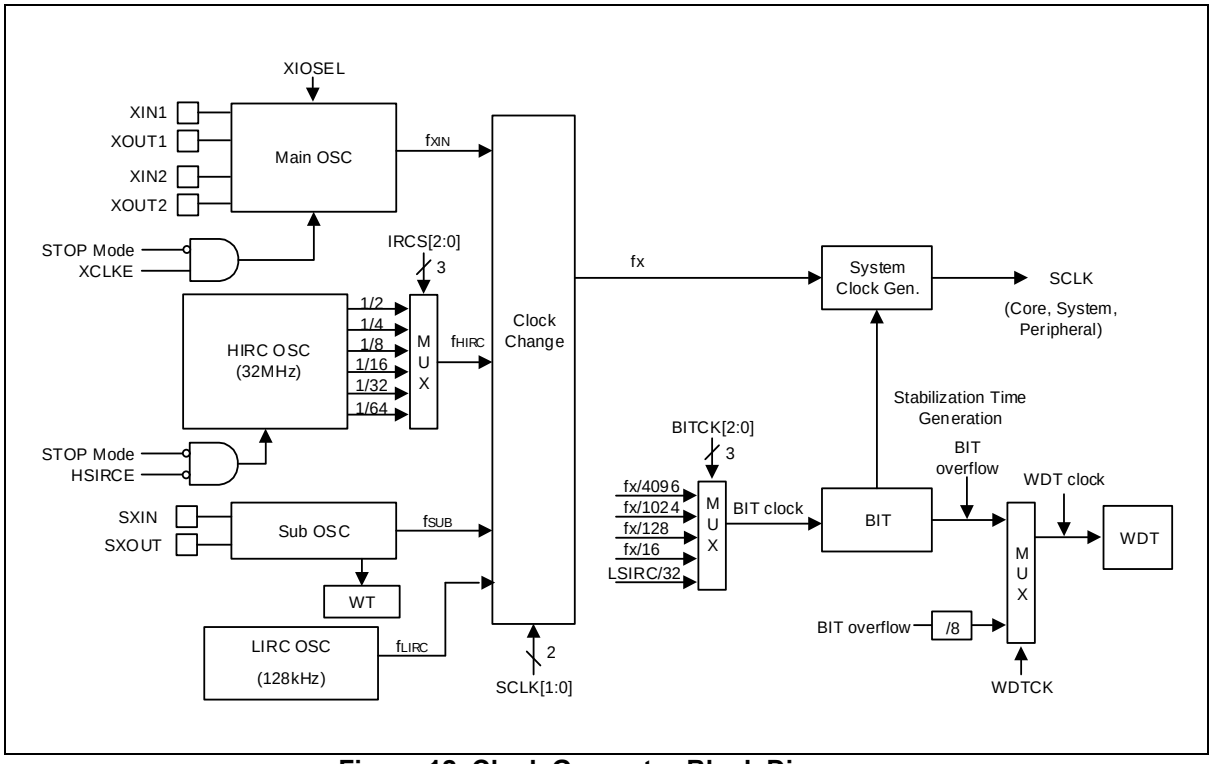


Figure 12. Clock Generator Block Diagram

9 Basic Interval Timer (BIT)

A96G150 has a free running 8-bit Basic Interval Timer (BIT). BIT generates the time base for Watchdog Timer counting, and provides a basic interval timer interrupt (BITIFR).

BIT of A96G150 features the followings:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As a timer, BIT generates a timer interrupt.

9.1 BIT block diagram

In this section, basic interval timer of A96G150 is described in a block diagram.

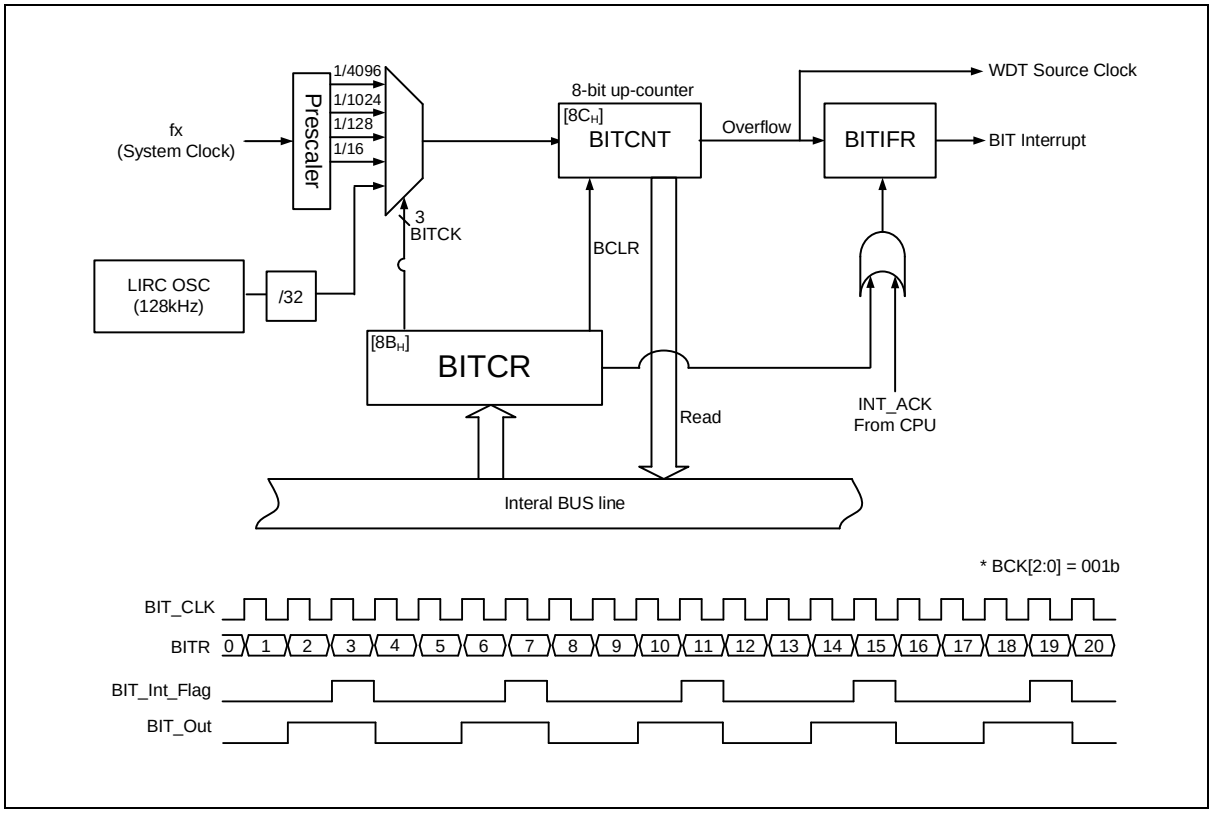


Figure 13. Basic Interval Timer Block Diagram

10 Watchdog Timer (WDT)

Watchdog Timer (WDT) rapidly detects the CPU malfunction such as endless looping caused by noise or something like that, and resumes the CPU to the normal state. Watchdog Timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the Watchdog Timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals.

It is possible to use free running 8-bit timer mode (WDTRSON='0') or watchdog timer mode (WDTRSON='1') by setting WDTCR[6] bit. If WDTCR[5] is set to '1', the WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically.

The WDT consists of an 8-bit binary counter and a watchdog timer data register. When value of the 8-bit binary counter is equal to the 8 bits of WDTCNT, an interrupt request flag is generated. This can be used as a watchdog timer interrupt or a reset signal of CPU in accordance with a bit WDTRSON.

Input clock source of the WDT is BIT overflow. An interval between watchdog timer interrupts is decided by BIT overflow period and WDTDR set value. The equation can be described as the followings:

- WDT Interrupt Interval = (BIT Interrupt Interval) X (WDTDR Value+1)

10.1 WDT block diagram

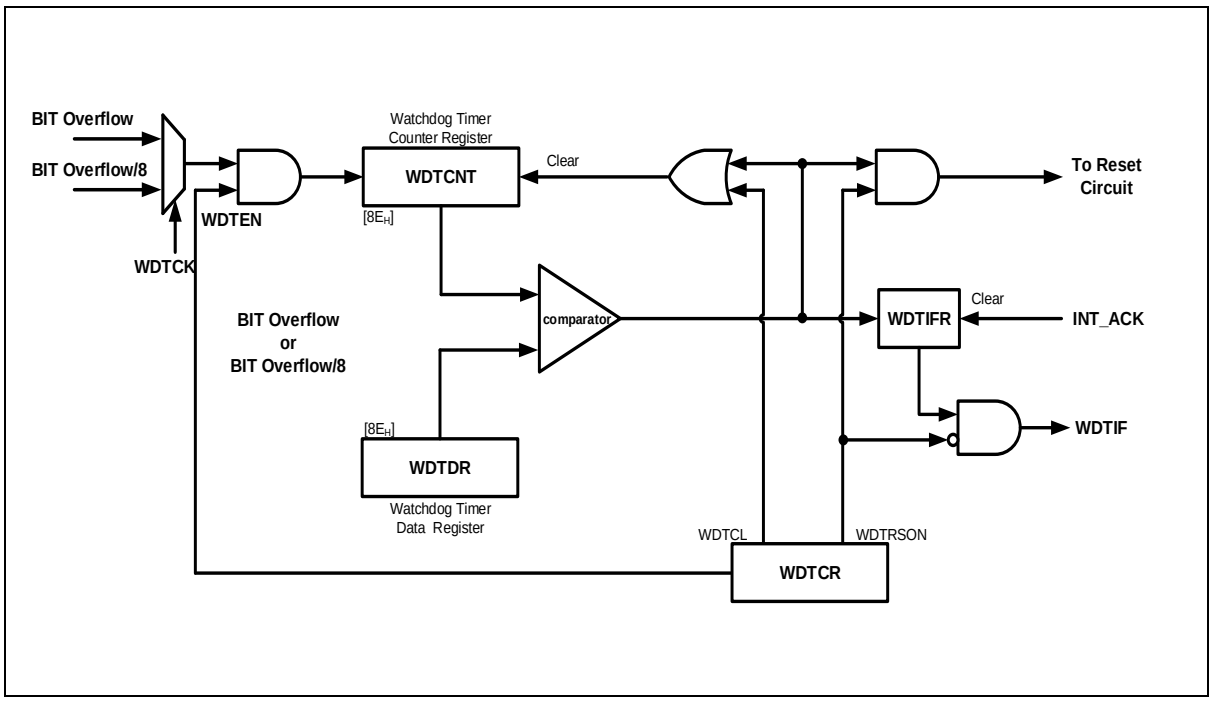


Figure 14. Watchdog Timer Block Diagram

11 Watch Timer (WT)

Watch Timer (WT) has functions for RTC (Real Time Clock) operation. It is generally used for RTC design. WT consists of a clock source select circuit, a timer counter circuit, an output select circuit and watch timer control registers.

Prior to operate WT, a user needs to determine an input clock source and output interval, and to set WTEN to '1' in watch timer control register (WTCR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WTCR register.

Although CPU is in STOP mode, a sub clock can be alive so that WT continues its operation. Watch timer counter circuits may be composed of 21-bit counter which contains low 14-bit with binary counter and high 7-bit counter in order to increase resolution. In WTDR, it can control WT clear and set interval value at write time, and it can read 7-bit WT counter value at read time.

11.1 WT block diagram

In this section, watch timer of A96G150 is described in a block diagram.

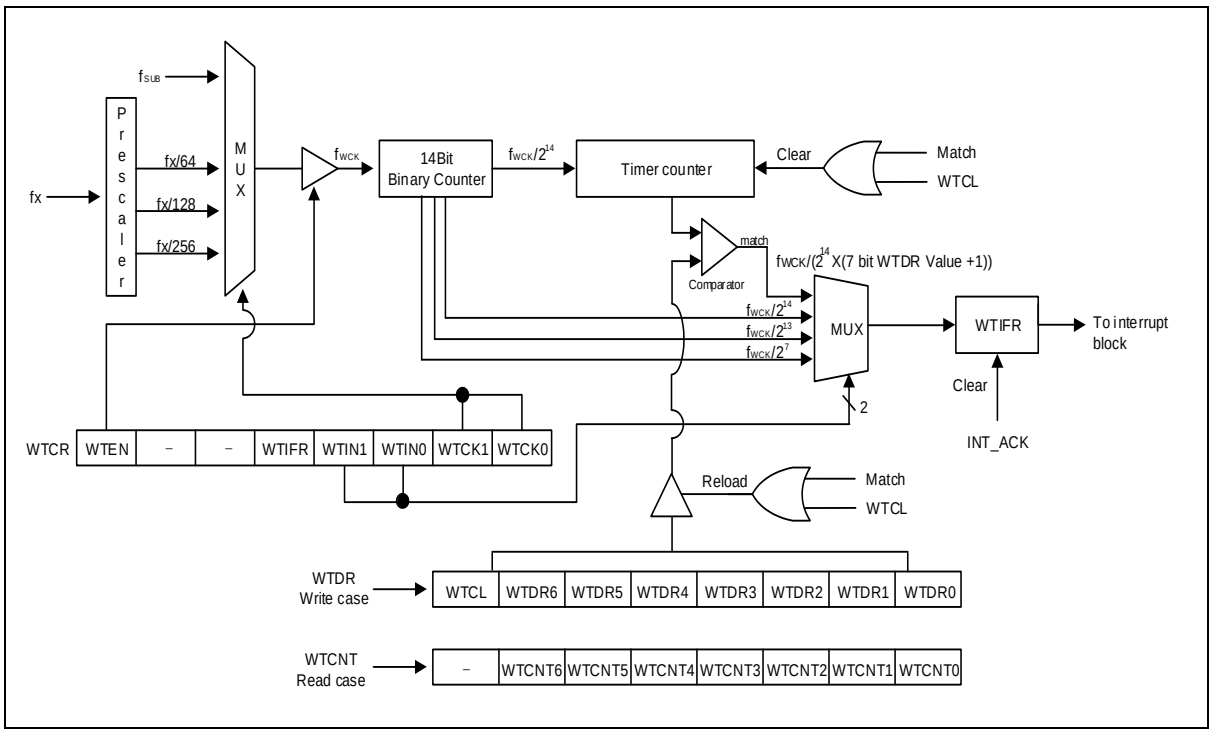


Figure 15. Watch Timer Block Diagram

12 Timer 0/1/2/3/4/5

12.1 Timer 0

An 8-bit timer 0 consists of a multiplexer, a timer 0 counter register, a timer 0 data register, a timer 0 capture data register and a timer 0 control register (T0CNT, T0DR, T0CDR, T0CR).

Timer 0 operates in one of three modes introduced in the followings:

- 8-bit timer/counter mode
- 8-bit PWM output mode
- 8-bit capture mode

Timer/counter 0 can be clocked by an internal or an external clock source (EC0). The clock source is selected by clock selection logic which is controlled by clock selection bits T0CK[2:0].

- TIMER0 clock source: f_X/2, 4, 8, 32, 128, 512, 2048 and EC0

In capture mode, data is captured into input capture data register (T0CDR) by EINT1. In timer/counter mode, whenever counter value is equal to T0DR, T0O port toggles. In addition, timer 0 outputs PWM waveform through PWM0O port in the PWM mode.

Table 9. Timer 0 Operating Mode

T0EN	T0MS[1:0]	T0CK[2:0]	Timer 0
1	00	XXX	8-bit Timer/Counter Mode
1	01	XXX	8-bit PWM Mode
1	1X	XXX	8-bit Capture Mode

12.1.1 Timer 0 block diagram

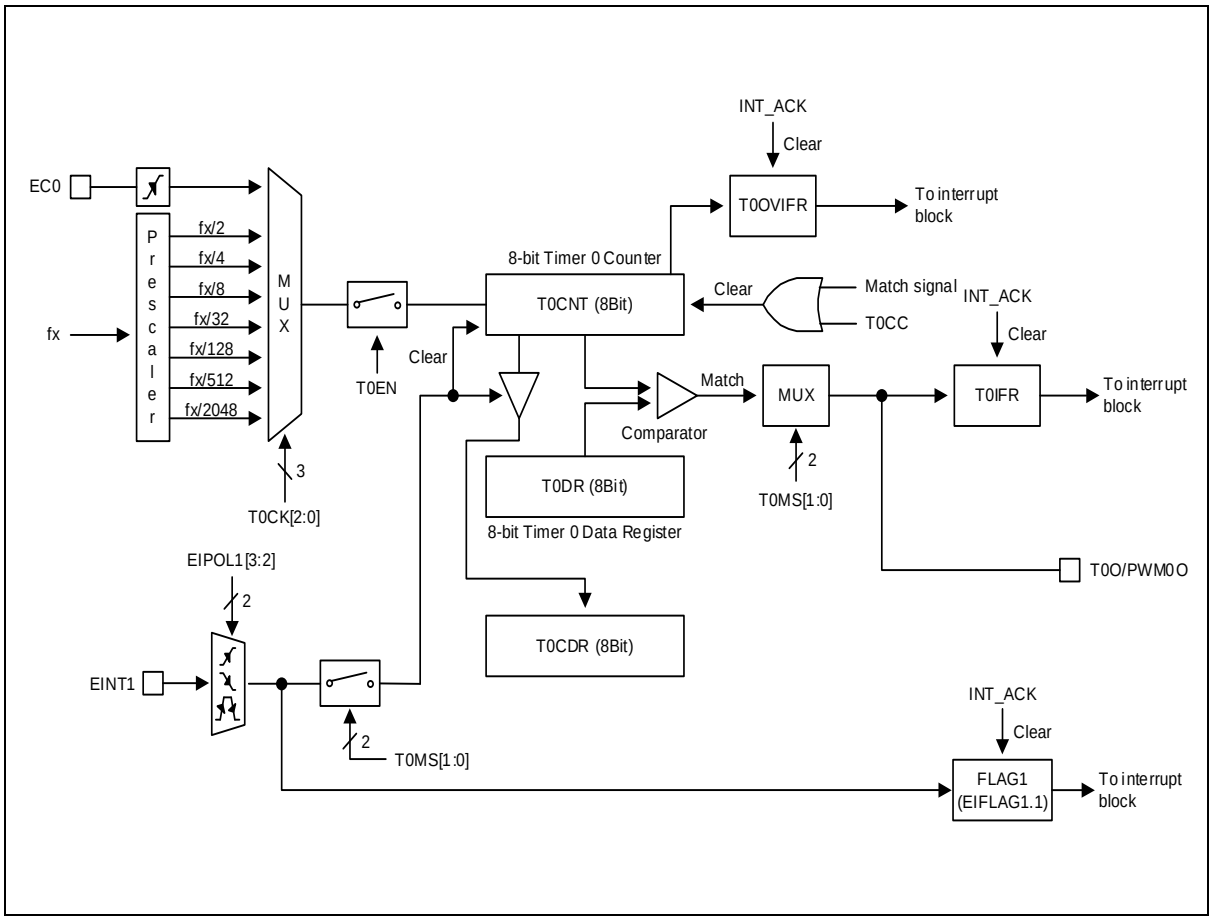


Figure 16. 8-bit Timer 0 Block Diagram

12.2 Timer 1

A 16-bit timer 1 consists of multiplexer, timer 1 A data register high/low, timer 1 B data register high/low and timer 1 control register high/low (T1ADRH, T1ADRL, T1BDRH, T1BDRL, T1CRH, T1CRL).

Timer 1 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 1 uses an internal clock or an external clock (EC1) as an input clock source. The clock sources are introduced below, and one is selected by clock selection logic which is controlled by clock selection bits (T1CK[2:0]).

- TIMER 1 clock source: f_X/1, 2, 4, 8, 64, 512, 2048 and EC1

In capture mode, the data is captured into input capture data register (T1BDRH/T1BDRL) by EINT2. Timer 1 results in the comparison between counter and data register through T1O port in timer/counter mode. In addition, Timer 1 outputs PWM waveform through PWM1Oport in the PPG mode.

Table 10. TIMER 1 Operating Modes

T1EN	P1FSRL[5:4]	T1MS[1:0]	T1CK[2:0]	Timer 1
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

12.2.1 16-bit timer 1 block diagram

In this section, a 16-bit timer 1 is described in a block diagram.

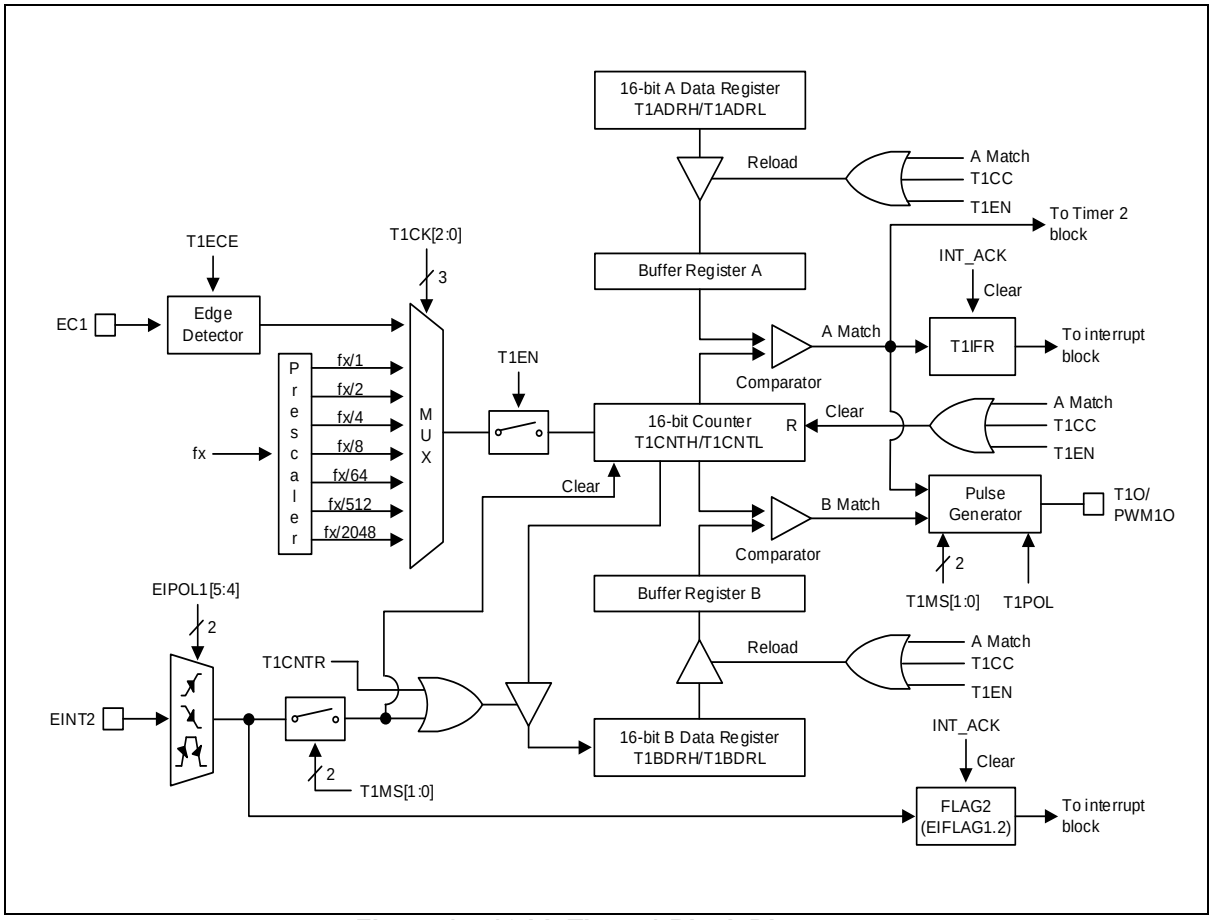


Figure 17. 16-bit Timer 1 Block Diagram

12.3 Timer 2

A 16-bit timer 2 consists of a multiplexer, timer 2 A data high/low register, timer 2 B data high/low register and timer 2 control high/low register (T2ADRH, T2ADRL, T2BDRH, T2BDRL, T2CRH, and T2CRL).

Timer 2 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 2 can be a divided clock of a system clock which is selected from prescaler output and T1 A Match (timer 1 A match signal). The clock source is selected by a clock selection logic, controlled by clock selection bits (T2CK[2:0]).

- TIMER 2 clock source: fx/1, fx/2, fx/4, fx/8, fx/32, fx/128, fx/512 and T1 A Match

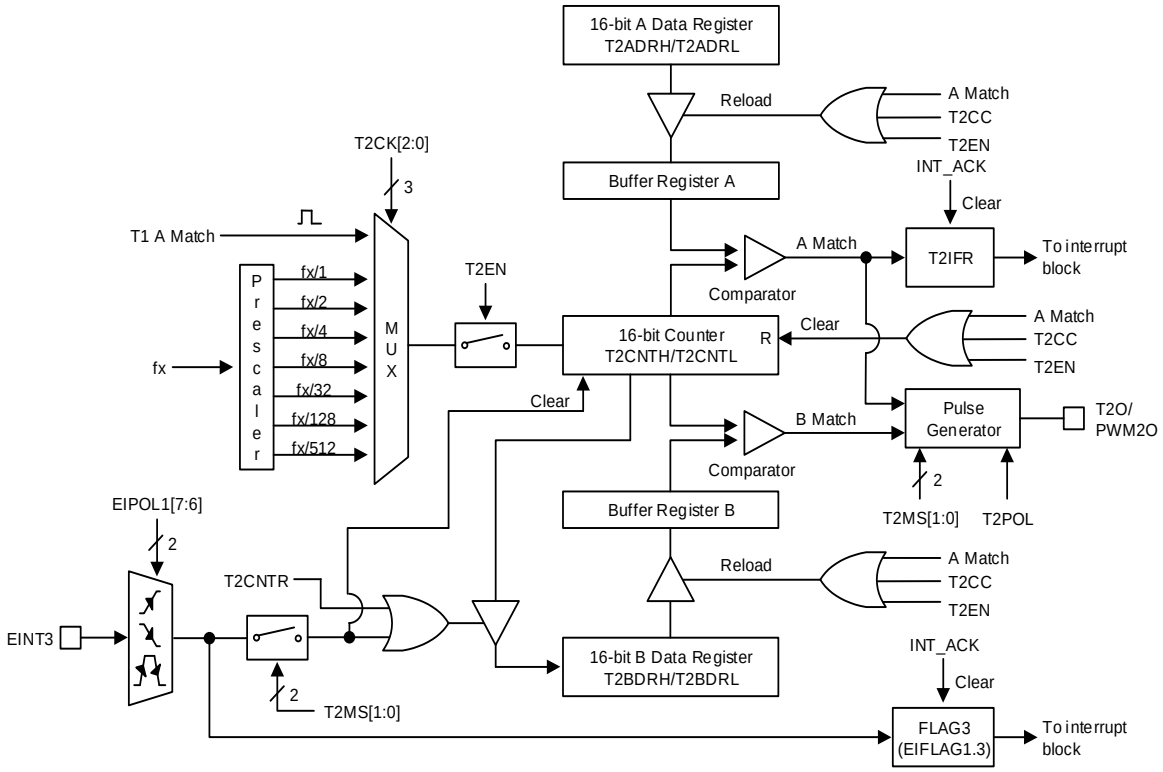
In capture mode, data is captured into input capture data registers (T2BDRH/T2BDRL) by EINT3. In timer/counter mode, whenever counter value is equal to T2ADRH/L, T2O port toggles. In addition, the timer 2 outputs PWM waveform to PWM2O port in the PPG mode.

Table 11. TIMER 2 Operating Modes

T2EN	P1FSRL[3:2]	T2MS[1:0]	T2CK[2:0]	Timer 2
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

12.3.1 16-bit timer 2 block diagram

In this section, a 16-bit timer 2 is described in a block diagram.



NOTE: T1 A Match is a pulse for the timer 2 clock source if it is selected.

Figure 18. 16-bit Timer 2 Block Diagram

12.4 Timer 3

A 16-bit timer 3 consists of a multiplexer, timer 3 A data high/low register, timer 3 B data high/low register and timer 3 control high/low register (T3ADRH, T3ADRL, T3BDRH, T3BDRL, T3CRH, and T3CRL).

Timer 3 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 3 can be clocked by an internal or an external clock source (EC3). The clock source is selected by a clock selection logic controlled by clock selection bits (T3CK[2:0]).

- TIMER 3 clock source: fx/1, fx/2, fx/4, fx/8, fx/64, fx/512, fx/2048 and EC3

In capture mode, data is captured into input capture data registers (T3BDRH/T3BDRL) by EINT43. Timer 3 results in the comparison between counter and data register through T3O port in timer/counter mode. In addition, timer 3 outputs PWM waveform through PWM3O port in the PPG mode.

Table 12. TIMER 3 Operating Modes

T3EN	P0FSRH[1:0]	T3MS[1:0]	T3CK[2:0]	Timer 3
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

12.4.1 16-bit timer 3 block diagram

In this section, a 16-bit timer 3 is described in a block diagram.

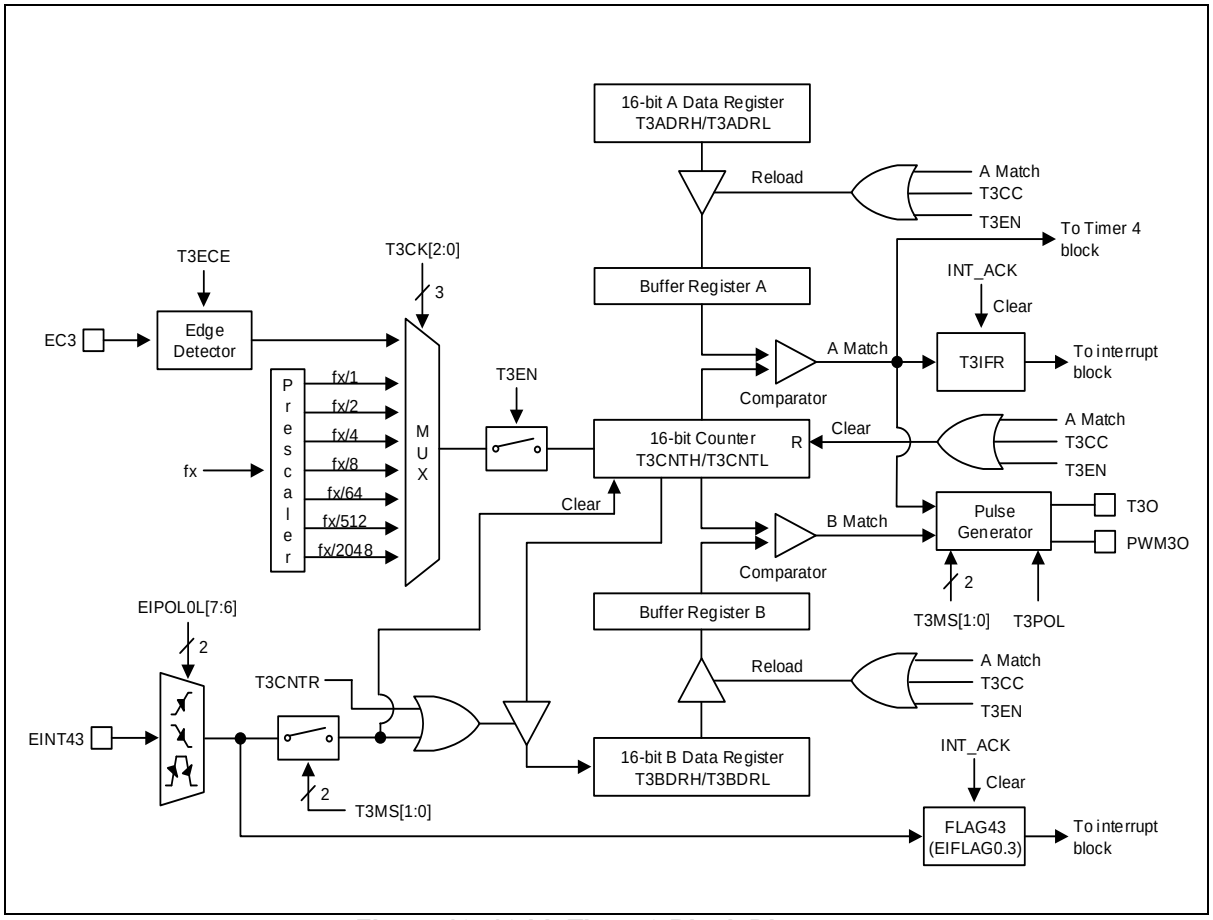


Figure 19. 16-bit Timer 3 Block Diagram

12.5 Timer 4

A 16-bit timer 4 consists of a multiplexer, timer 4 A data high/low register, timer 4 B data high/low register and timer 4 control high/low register (T4ADRH, T4ADRL, T4BDRH, T4BDRL, T4CRH, and T4CRL).

Timer 4 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 4 can be a divided clock of a system clock selected from prescaler output and T3 A Match (timer 3 A match signal). The clock source is selected by a clock selection logic controlled by clock selection bits (T4CK[2:0]).

- TIMER 4 clock source: fx/1, fx/2, fx4, fx/8, fx/32, fx/128, fx/512 and T3 A Match

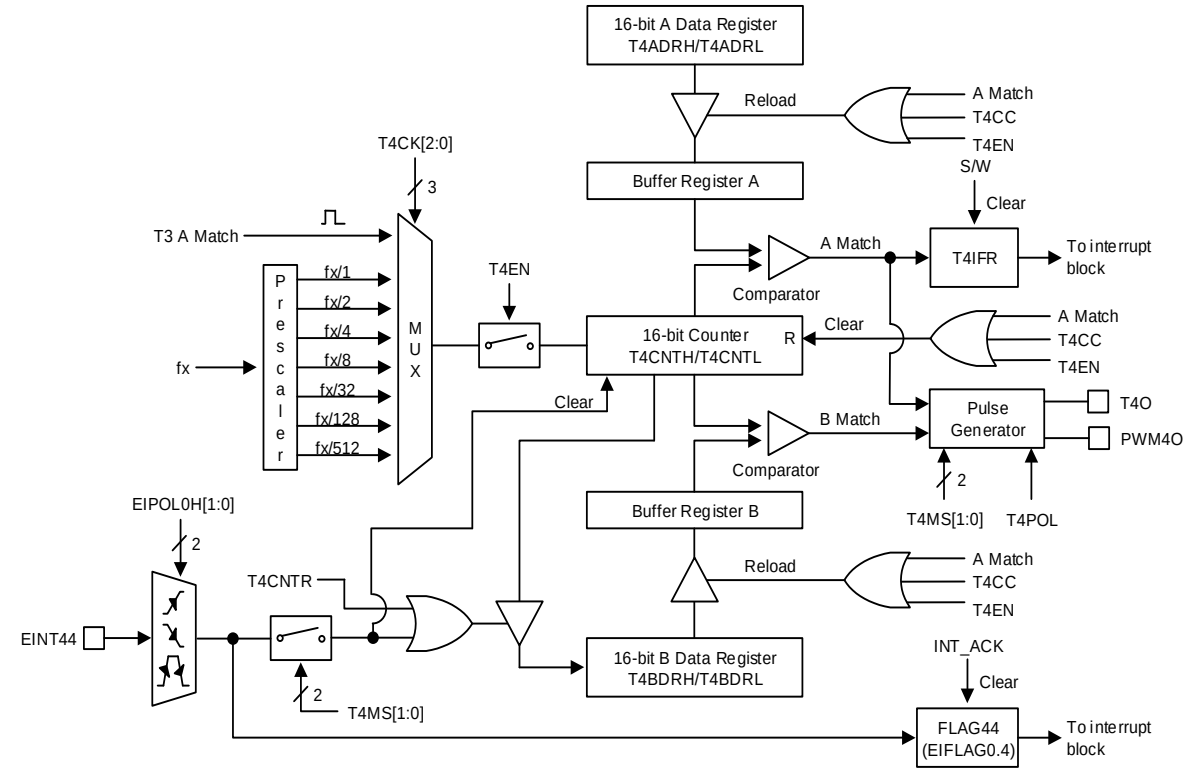
In capture mode, data is captured into input capture data registers (T4BDRH/T4BDRL) by EINT44. In timer/counter mode, whenever counter value is equal to T4ADRH/L, T4O port toggles. In addition, the TIMER 4 outputs PWM waveform to PWM4O port in the PPG mode.

Table 13. TIMER 4 Operating Modes

T4EN	P0FSRH[3:2]	T4MS[1:0]	T4CK[2:0]	Timer 4
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

12.5.1 16-bit timer 4 block diagram

In this section, a 16-bit timer 4 is described in a block diagram.



NOTE: T3 A Match is a pulse for the timer 4 clock source if it is selected.

Figure 20. 16-bit Timer 4 Block Diagram

12.6 Timer 5

A 16-bit timer 5 consists of a multiplexer, timer 5 A data high/low register, timer 5 B data high/low register and timer 5 control high/low register (T5ADRH, T5ADRL, T5BDRH, T5BDRL, T5CRH, and T5CRL).

Timer 5 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 5 can be a divided clock of a system clock selected from prescaler output. The clock source is selected by a clock selection logic controlled by clock selection bits (T5CK[2:0]).

- TIMER 5 clock source: fx/1, fx/2, fx/4, fx/8, fx/32, fx/128, fx/512 and HSIRC

In capture mode, data is captured into input capture data registers (T5BDRH/T5BDRL) by EINT45. In timer/counter mode, whenever counter value is equal to T5ADRH/L, T5O port toggles. In addition, the TIMER 5 outputs PWM waveform to PWM5O port in the PPG mode.

Table 14. TIMER 5 Operating Modes

T5EN	P0FSRH[5:4]	T5MS[1:0]	T5CK[2:0]	Timer 5
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

12.6.1 16-bit timer 5 block diagram

In this section, a 16-bit timer 5 is described in a block diagram.

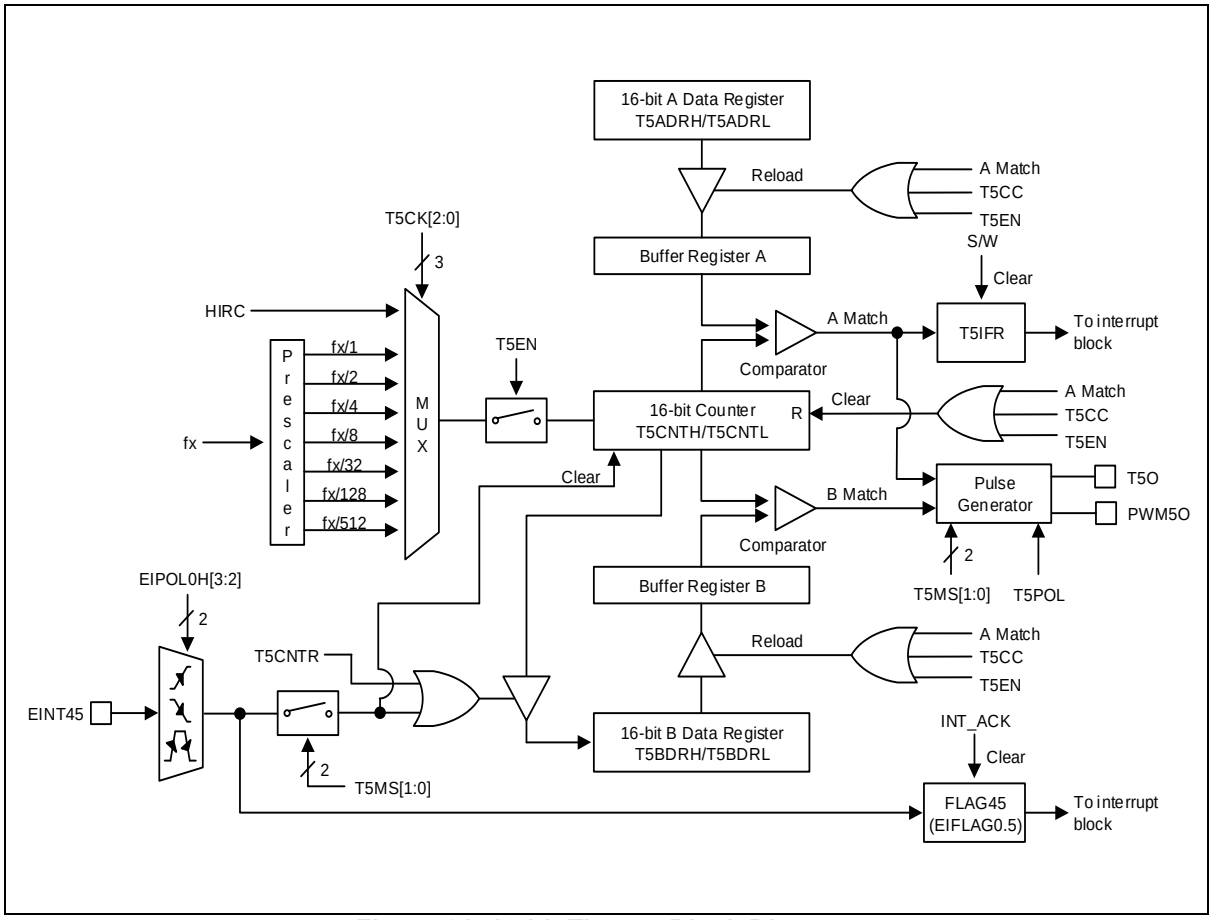


Figure 21. 16-bit Timer 5 Block Diagram

13 Buzzer driver

A buzzer of A96G150 consists of 8-bit counter, a buzzer data register (BUZDR), and a buzzer control register (BUZCR). It outputs square wave (61.035Hz to 125.0KHz @ 8MHz) through P53/BUZO pin, and its buzzer data register (BUZDR) controls the buzzer frequency (refer to the following expression). In a buzzer control register (BUZCR), BUCK[1:0] bits select a source clock divided by prescaler.

$$f_{BUZ}(Hz) = \frac{\text{Oscillator Frequency}}{2 \times \text{Prescaler Ratio} \times (\text{BUZDR} + 1)}$$

Table 15. Buzzer Frequency at 8MHz

BUZDR[7:0]	Buzzer frequency (KHz)			
	BUZCR[2:1]=00	BUZCR[2:1]=01	BUZCR[2:1]=10	BUZCR[2:1]=11
0000_0000	125KHz	62.5KHz	31.25KHz	15.625KHz
0000_0001	62.5KHz	31.25KHz	15.625KHz	7.812KHz
…	…	…	…	…
1111_1101	492.126Hz	246.063Hz	123.031Hz	61.515Hz
1111_1110	490.196Hz	245.098Hz	122.549Hz	61.274Hz
1111_1111	488.281Hz	244.141Hz	122.07Hz	61.035Hz

13.1 Buzzer driver block diagram

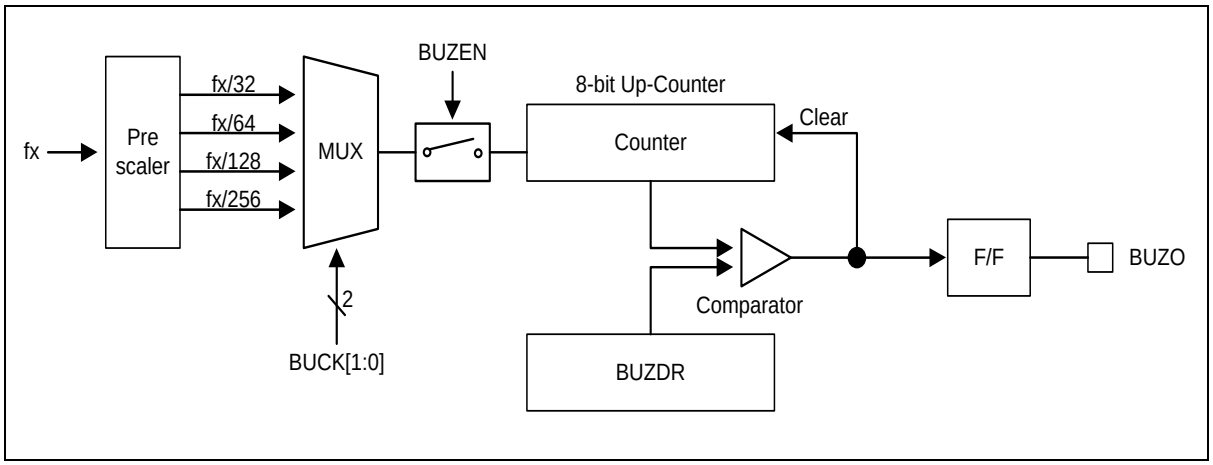


Figure 22. Buzzer Driver Block Diagram

14 12-bit Analog-to-digital Converter (ADC)

Analog-to-digital Converter (ADC) of A96G150 allows conversion of an analog input signal to corresponding 12-bit digital value. This A/D module has eight analog inputs. Output of the multiplexer becomes input into the converter which generates the result through successive approximation.

The A/D module has four registers which are the A/D converter control high register (ADCCRH), A/D converter control low register (ADCCRL), A/D converter data high register (ADCDRH), and A/D converter data low register (ADCDRL).

ADSEL[3:0] bits are used to select channels to be converted. To execute A/D conversion, TRIG[2:0] bits should be set to 'xxx'. Registers ADCDRH and ADCDRL contain the result of A/D conversion. When the conversion is completed, the result is loaded into ADCDRH and ADCDRL, A/D conversion status bit AFLAG is set to '1', and A/D interrupt is set. During the A/D conversion, AFLAG bit is read as '0'.

14.1 Block diagram

In this section, the 12-bit ADC is described in a block diagram, and an analog input pin and a power pin with capacitors respectively are introduced.

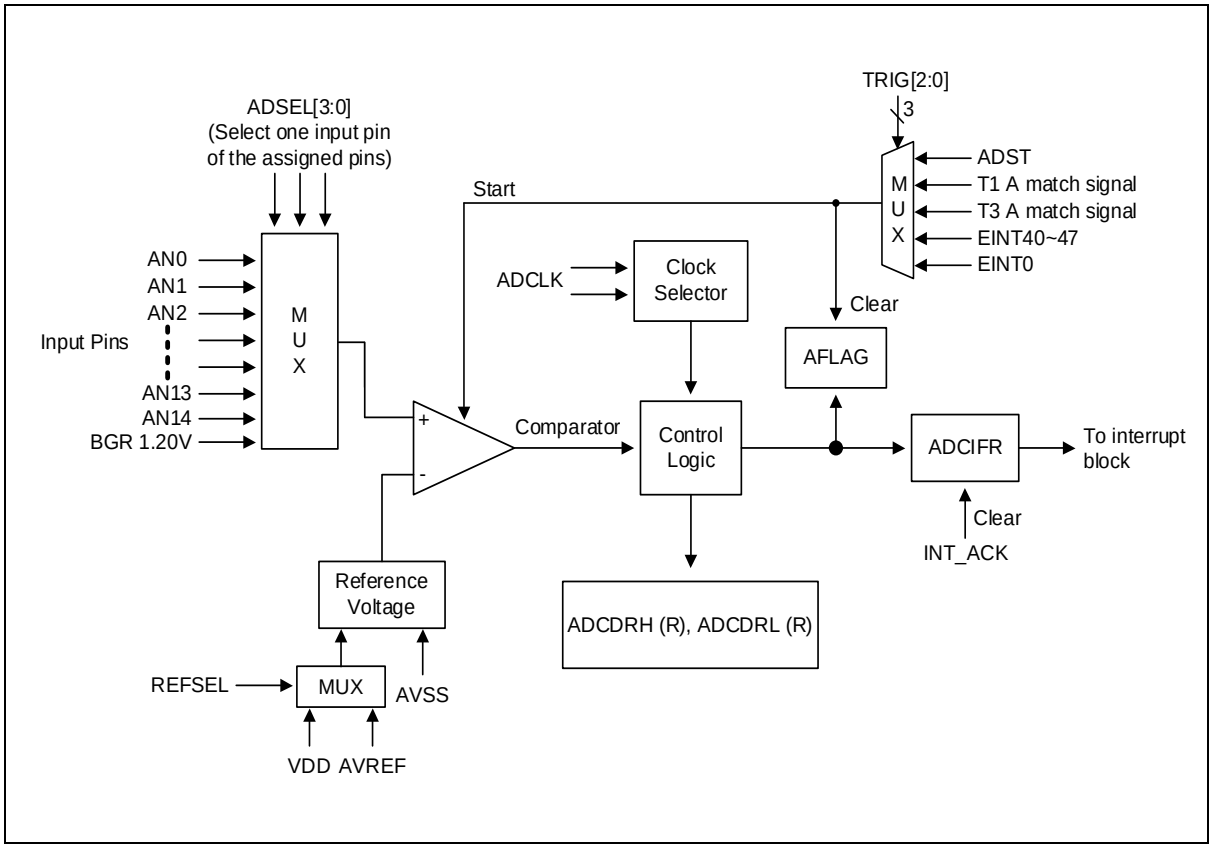


Figure 23. 12-bit ADC Block Diagram

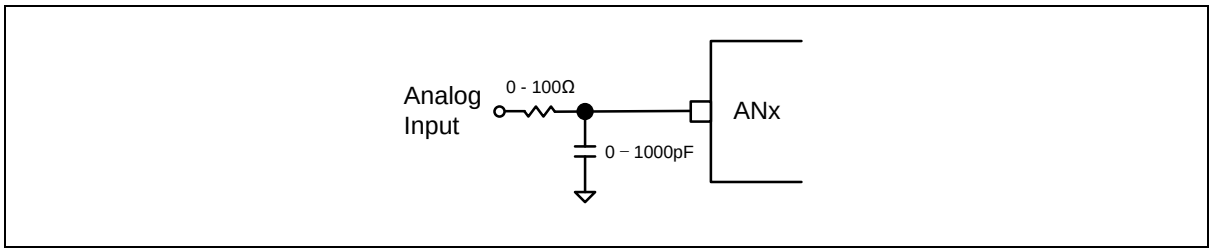


Figure 24. A/D Analog Input Pin with a Capacitor

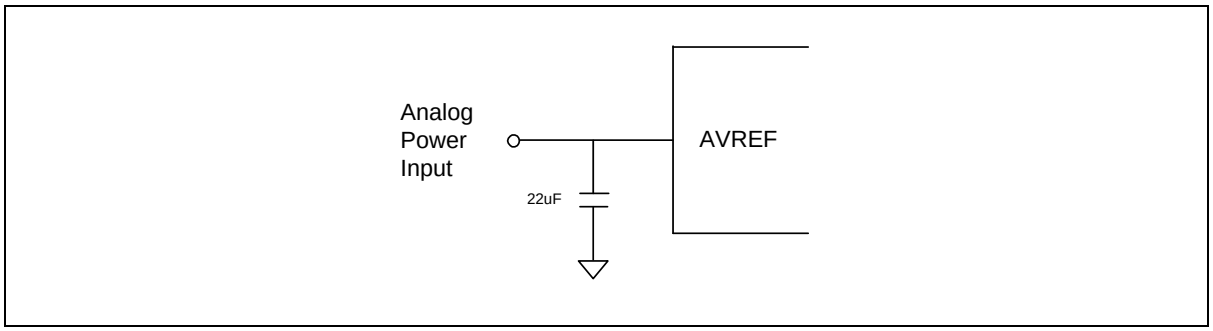


Figure 25. A/D Power (AVREF) Pin with a Capacitor

15 Combination of USART, SPI, and I2C (USI)

USI stands for the combination of USART, SPI and I2C. A96G150 has two USI function blocks, USI0 and USI1, which are identical to each other functionally. Each USI block consists of USI control registers 1/2/3/4, USI status registers 1/2, USI baud-rate generation register, USI data register, USI SDA hold time register, USI SCL high period register, USI SCL low period register, and USI slave address register (USInCR1, USInCR2, USInCR3, USInCR4, USInST1, USInST2, USInBD, USInDR, USInSDHR, USInSCHR, USInSCLR, USInSAR). The ‘n’ means ‘0’ or ‘1’.

USI operates in one of the following modes selected by USIn selection bits (USInMS[1:0]):

- Asynchronous mode (UART)
- Synchronous mode (USART)
- SPI mode
- I2C mode

15.1 USIn UART mode

Universal synchronous and asynchronous serial receiver and transmitter (USART) are highly flexible serial communication devices. Main features are listed below:

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation and Parity Check are Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion
- Double Speed Asynchronous communication mode

The USIn comprises clock generator, transmitter and receiver. Clock generation logic consists of synchronization logic for external clock input used by synchronizing or SPI slave operation, and the baud rate generator for asynchronous or master (synchronous or SPI) operation.

Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. A write buffer allows continuous transfer of data without any delay between frames.

Receiver is the most complex part of the UART module due to its clock and data recovery units. The recovery unit is used for asynchronous data reception. In addition to the recovery unit, the receiver includes a parity checker, a shift register, a two-level receive FIFO (USInDR) and control logic. The receiver supports the same frame formats as the transmitter and can detect frame error, data overrun and parity errors.

15.2 USIn UART block diagram

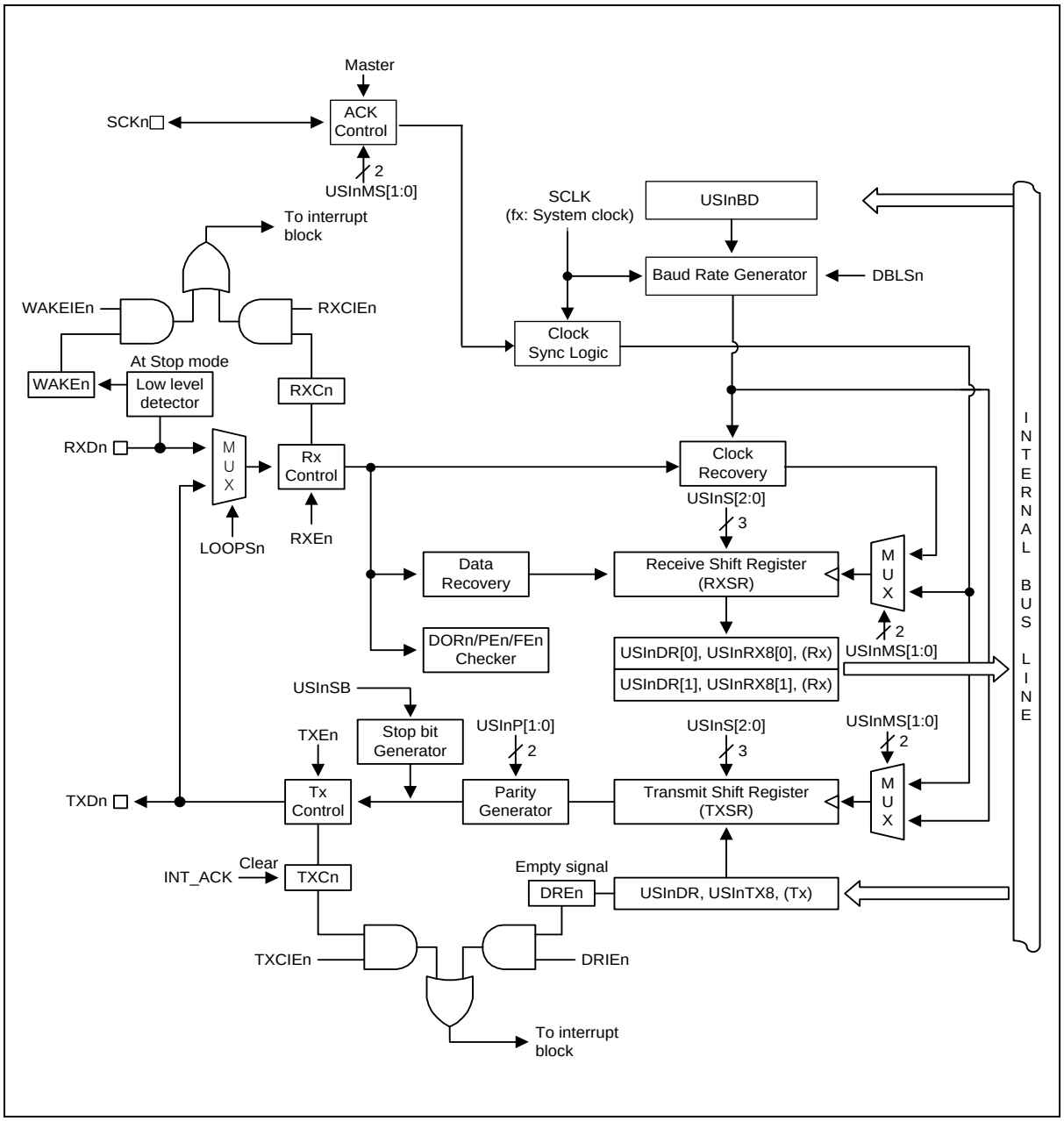


Figure 26. USIn USART Block Diagram (n = 0 and 1)

15.3 USIn SPI mode

The USIn can be set to operate in industrial standard SPI compliant mode. The SPI mode has the following features.

- Full duplex, three-wire synchronous data transfer
- Master and slave operation
- Supports all four SPIn modes of operation (mode 0, 1, 2, and 3)
- Selectable LSB first or MSB first data transfer
- Double buffered transmit and receive
- Programmable transmit bit rate

When SPI mode is enabled (USInMS[1:0]=”11”), the slave select (SSn) pin becomes active LOW input in slave mode operation, or can be output in master mode operation if USInSSEN bit is set to ‘0’.

Note that during SPI mode of operation, the pin RXDn is renamed as MISOn and TXDn is renamed as MOSIn for compatibility to other SPI devices.

15.4 USIn SPI block diagram

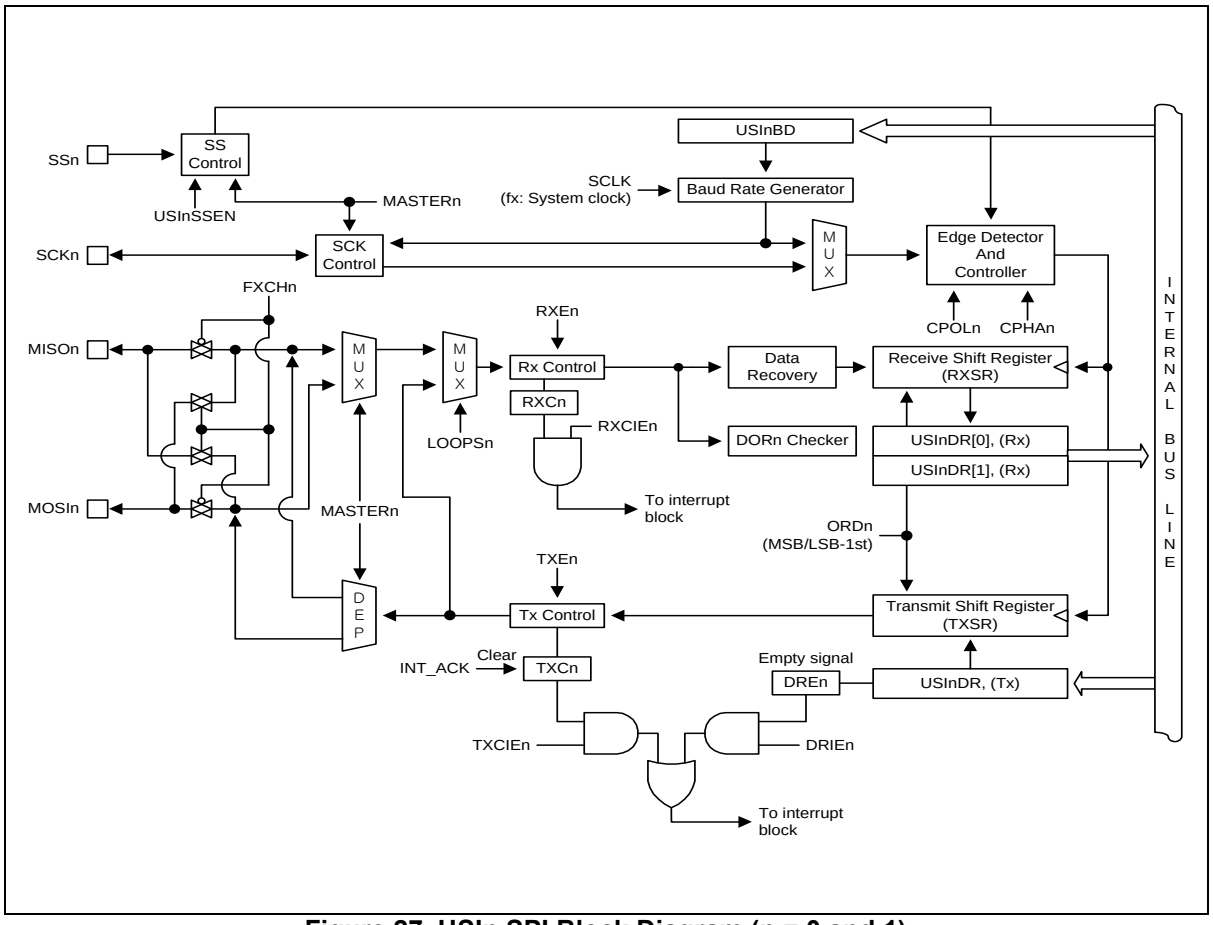


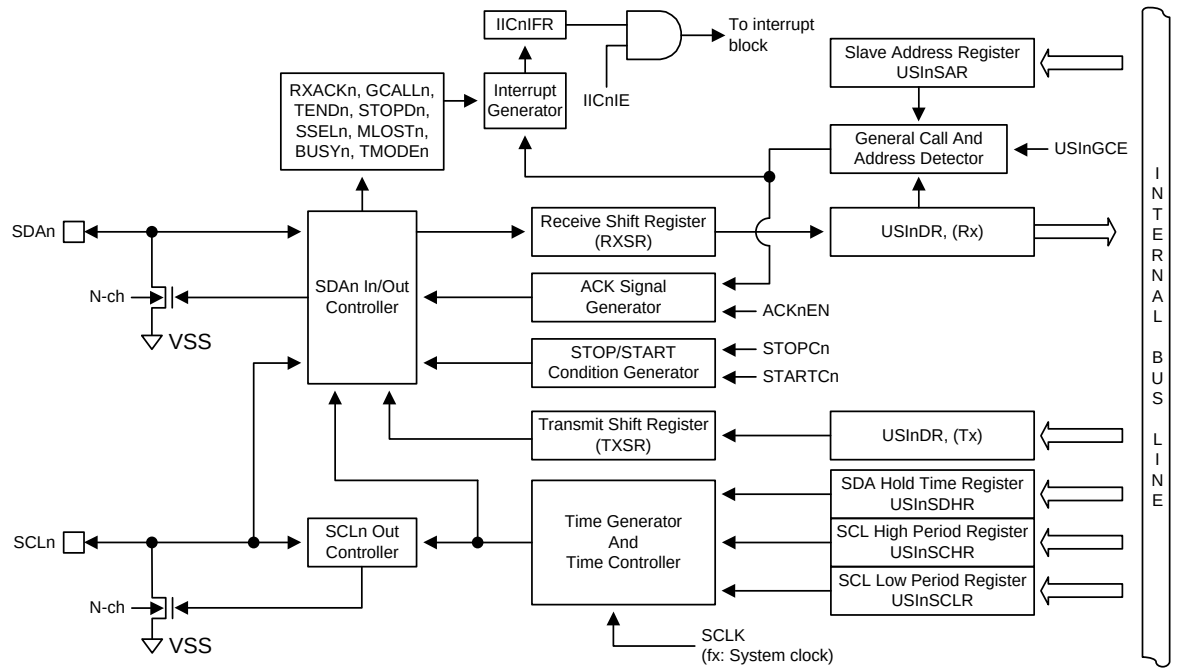
Figure 27. USIn SPI Block Diagram (n = 0 and 1)

15.5 USIn I2C mode

The USIn can be set to operate in industrial standard serial communication protocols mode. The I2C mode uses 2 bus lines serial data line (SDAn) and serial clock line (SCLn) to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs pull-up resistor. The features are as shown below.

- Compatible with I2C bus standard
- Multi-master operation
- Up to 400kHz data transfer read speed
- 7 bit address
- Both master and slave operation
- Bus busy detection

15.6 USIn I2C block diagram



NOTE: When the USIn block is an I2C mode and the corresponding port is a sub-function for SCLn/SDAn pin, The SCLn/SDAn pins are automatically set to the N-channel open-drain outputs and the input latch is read in the case of reading the pins. The corresponding pull-up resistor is determined by the control register.

Figure 28. USIn I2C Block Diagram

16 Universal Synchronous/Asynchronous Serial Rx/Tx (USART2)

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. USART2 of A96G150 features the followings:

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Master or Slave Clocked Synchronous and SPI Operation
- Supports all four SPI Modes of Operation (Mode 0, 1, 2, 3)
- LSB First or MSB First Data Transfer @SPI mode
- High Resolution Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Digital Low Pass Filter
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete
- Double Speed Asynchronous Communication Mode

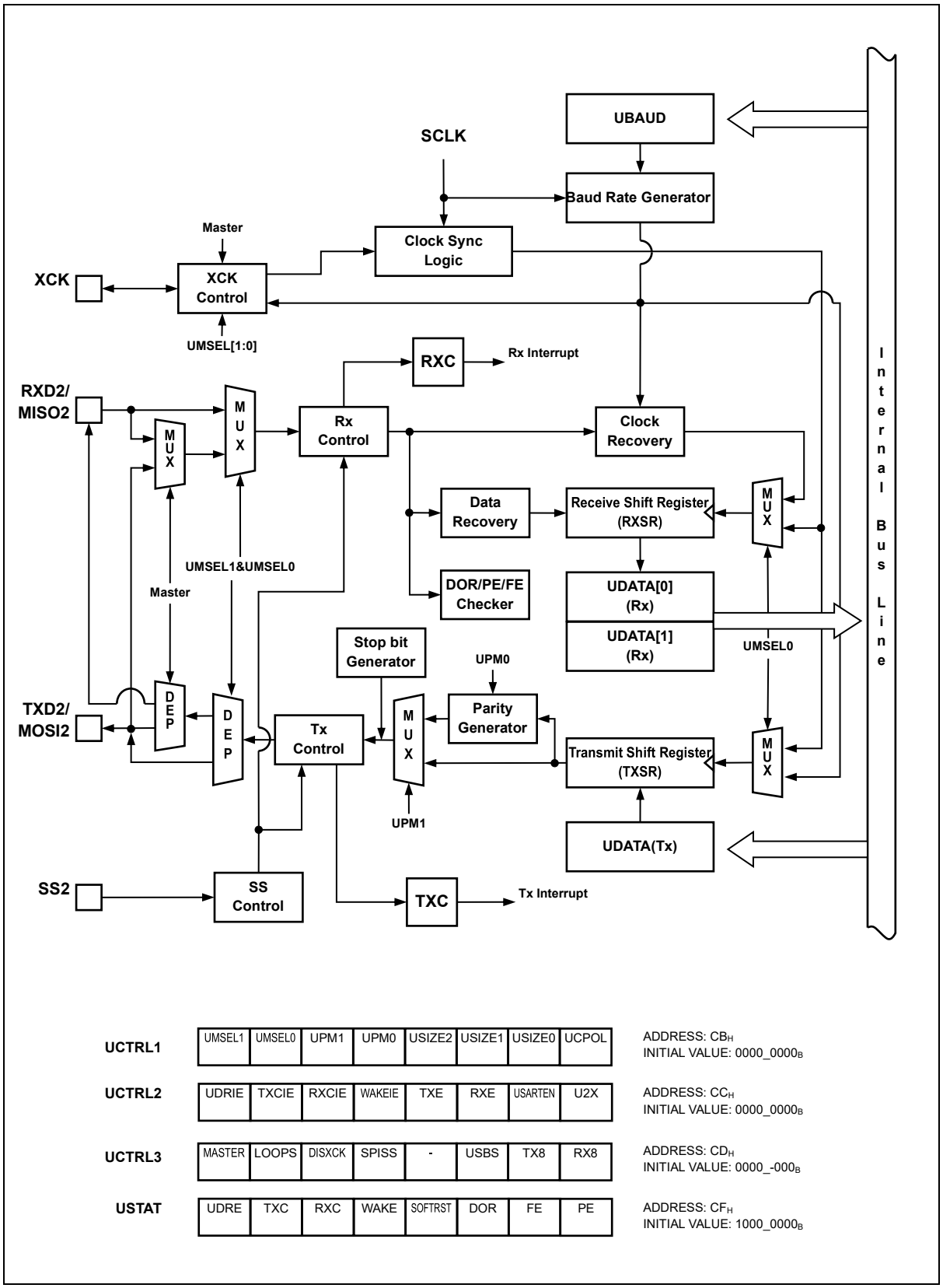
USART2 has three main parts such as a Clock Generator, Transmitter and Receiver.

Clock Generation logic consists of a synchronization logic for external clock input used by synchronous or SPI slave operation, and a baud rate generator for asynchronous or master (synchronous or SPI) operation.

Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. Write buffer allows a continuous transfer of data without any delay between frames.

Receiver is the most complex part of the USART2 module due to its clock and data recovery units. Recovery unit is used for asynchronous data reception. In addition to the recovery unit, the Receiver includes a parity checker, a shift register, a two level receive FIFO (UDATA) and control logic. The Receiver supports the same frame formats as the Transmitter and can detect Frame Error, Data OverRun and Parity Errors.

16.1 Block diagram



UCTRL1	UMSEL1	UMSEL0	UPM1	UPM0	USIZE2	USIZE1	USIZE0	UCPOL
UCTRL2	UDRIE	TXCIE	RXCIE	WAKEIE	TXE	RXE	USARTEN	U2X
UCTRL3	MASTER	LOOPS	DISXCK	SPISS	-	USBS	TX8	RX8
USTAT	UDRE	TXC	RXC	WAKE	SOFTRST	DOR	FE	PE

ADDRESS: CB_H
INITIAL VALUE: 0000_0000_B

ADDRESS: CC_H
INITIAL VALUE: 0000_0000_B

ADDRESS: CD_H
INITIAL VALUE: 0000_-000_B

ADDRESS: CF_H
INITIAL VALUE: 1000_0000_B

Figure 29. USART2 Block Diagram

17 LCD driver

The LCD driver is controlled by the LCD control register (LCD_CR) and LCD driver bias and contrast control register (LCD_BCCR). The LCLK[1:0] determines the frequency of COM signal scanning of each segment output. A RESET clears the LCD control register LCD_CR and LCD_BCCR values to logic '0'.

The LCD display can continue operating during IDLE and STOP modes.

The clock and duty for LCD driver is automatically initialized by hardware, whenever LCD_CR register data value is rewritten. So, don't rewrite LCD_CR frequently.

17.1 Block diagram

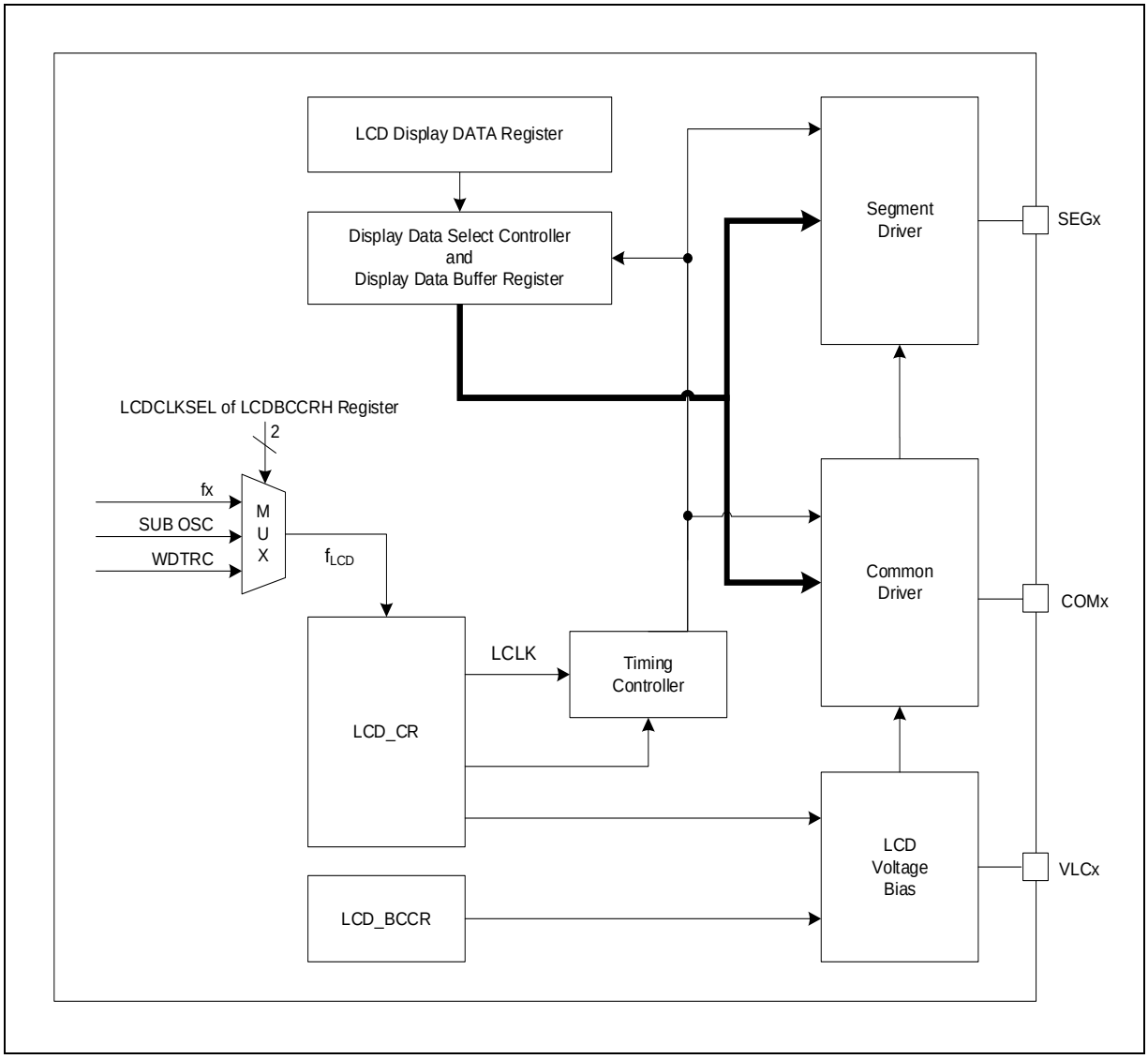


Figure 30. Block Diagram Figure

18 Cyclic Redundancy Check (CRC)

Using the CRC, it can be monitor the memory of the specified area. This is a one-time operation, and reset is required for continuous operation. In CRC MNT mode, when the CRC read is finished, CRC_FLAG occurs. In CRC validate mode, if the CRC validate fail after the CRC reading is finished, CRC_FLAG occurs. CRC_FAIL indicates the status of validate results when the CRC read is finished. If the CRC_FLAG is generated and the interrupt is enabled, interrupt service routine is served. CRC-FLAG is not cleared by hardware. CRC-TYPE 0~3 are not supported. Validate is done by comparing the CRC_MNT register and the CRC register value. CRC are not automatically initialized, you need to calculate a new CRC after CRC_H, CRC_L Clear.

Table 16. CRC Mode

CRC type	CRC mode	CRC input	Condition of CRC_FLAG	Condition of CRC reset
CRC_TYPE = 4	MNT	Flash Data	After CRC reading	-
CRC_TYPE = 6	Validate	Flash Data	After CRC reading & Validate fail	Validate fail

18.1 Block diagram

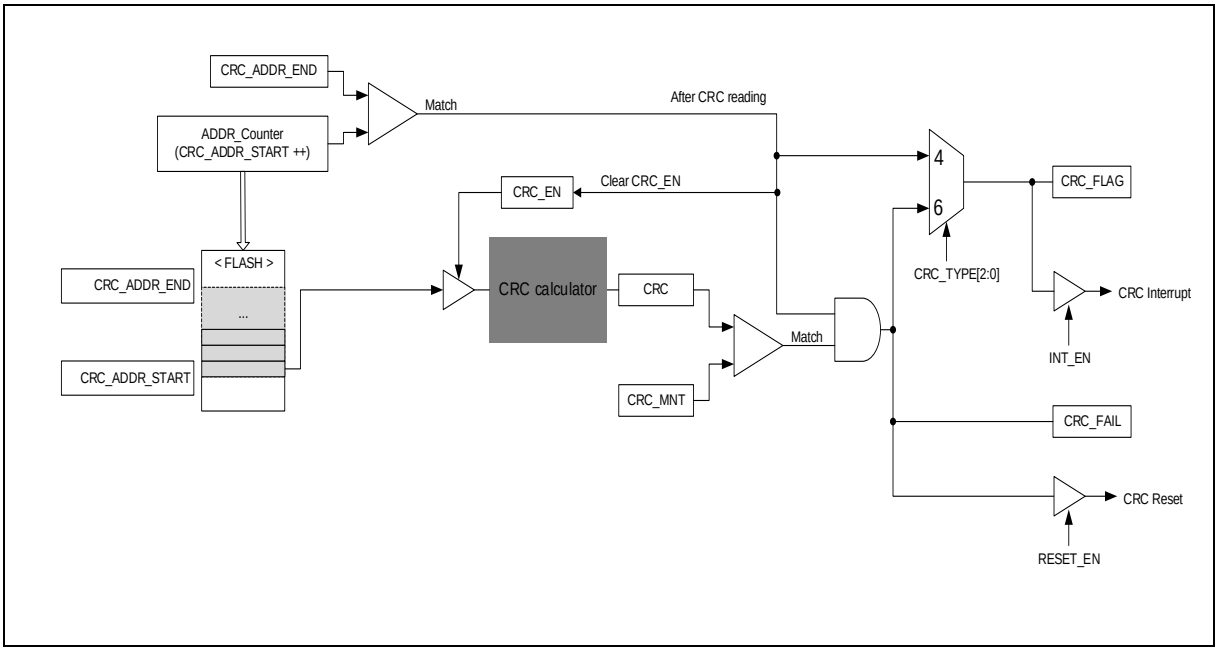


Figure 31. CRC Block Diagram

19 Power down operation

A96G150 has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. A96G150 provides three kinds of power saving functions such as Main-IDLE mode, Sub-IDLE mode and STOP mode. During one of these three modes, program will be stopped.

19.1 Peripheral operation in IDLE/ STOP mode

Table 17 shows operation status of each peripheral in IDLE mode and STOP mode.

Table 17. Peripheral Operation Status during Power Down Mode

Peripheral	IDLE mode	STOP mode
CPU	ALL CPU operations are disabled.	ALL CPU operations are disabled.
RAM	Retains.	Retains.
Basic Interval Timer	Operates continuously.	Stops (can be operated with WDTRC OSC).
Watchdog Timer	Operates continuously.	Stops (can be operated with WDTRC OSC).
Watch Timer	Operates continuously.	Stops (can be operated with sub clock).
Timer0~4	Operates continuously.	Halts (only when the event counter mode is enabled, timer operates normally).
ADC	Operates continuously.	Stops.
BUZ	Operates continuously.	Stops.
USI0/1	Operates continuously.	Only operates with external clock.
Internal OSC (32MHz)	Oscillates.	Stops when the system clock (fx) is f_{HSIRC}.
WDTRC OSC (128kHz)	Can be operated with setting value.	Can be operated programmable.
Main OSC (0.4~12MHz)	Oscillates.	Stops when fx = f_{XIN}.
Sub OSC (32.768kHz)	Oscillates.	Can be operated programmable.
I/O Port	Retains.	Retains.
Control Register	Retains.	Retains.
Address Data Bus	Retains.	Retains.

Table 17. Peripheral Operation Status during Power Down Mode (continued)

Peripheral	IDLE mode	STOP mode
Release Method	• By RESET • All Interrupts	• By RESET • Timer Interrupt (EC0, EC1, EC3) • External Interrupt • USART2 by RX, WT (sub clock), WDT • USI0/1 by RX, I2C(Slave mode)

20 Reset

Table 18 shows hardware setting values of main peripherals.

Table 18. Hardware Setting Values in Reset State

On-chip hardware	Initial value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Refer to the Peripheral Registers

A96G150 has five types of reset sources as shown in the followings:

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset (In the case of LVREN = `0 `)
- OCD Reset

20.1 Reset block diagram

In this section, reset unit is described in a block diagram.

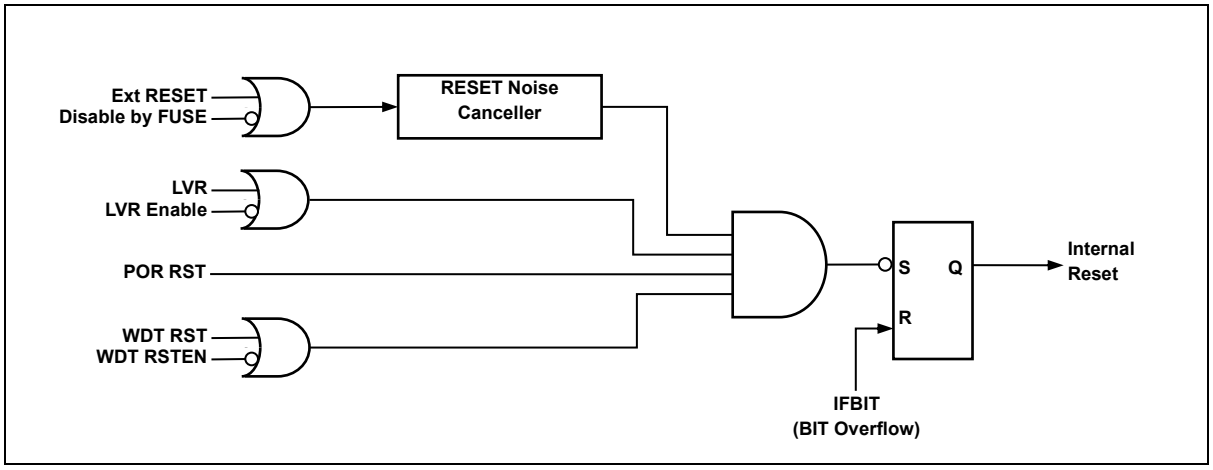


Figure 32. Reset Block Diagram

21 Memory programming

A96G150 has flash and data EEPROM memory to which a program can be written, erased, and overwritten while mounted on the board. Serial ISP mode is supported.

Flash of A96G150 features the followings:

- Flash Size : 64Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 30,000 program/erase cycles at typical voltage and temperature for flash memory
- Up to 300,000 program/erase cycles at typical voltage and temperature for data EEPROM memory
- Security feature

21.1 Memory map

21.1.1 Flash memory map

Program memory uses 64K bytes of flash memory. It is read by byte and written by byte or page. One page is 64-bytes

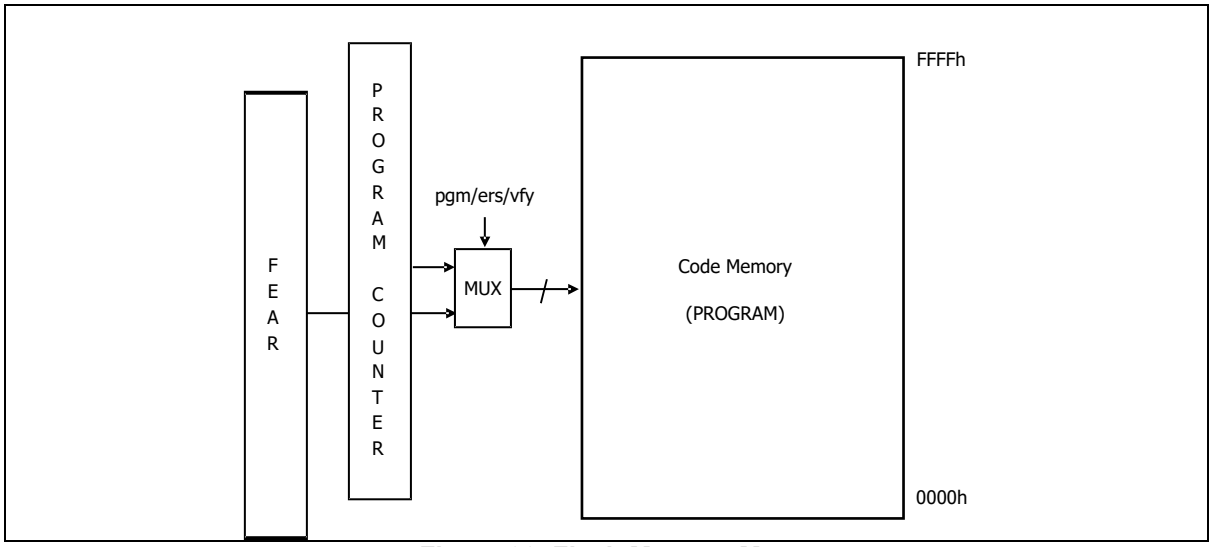


Figure 33. Flash Memory Map

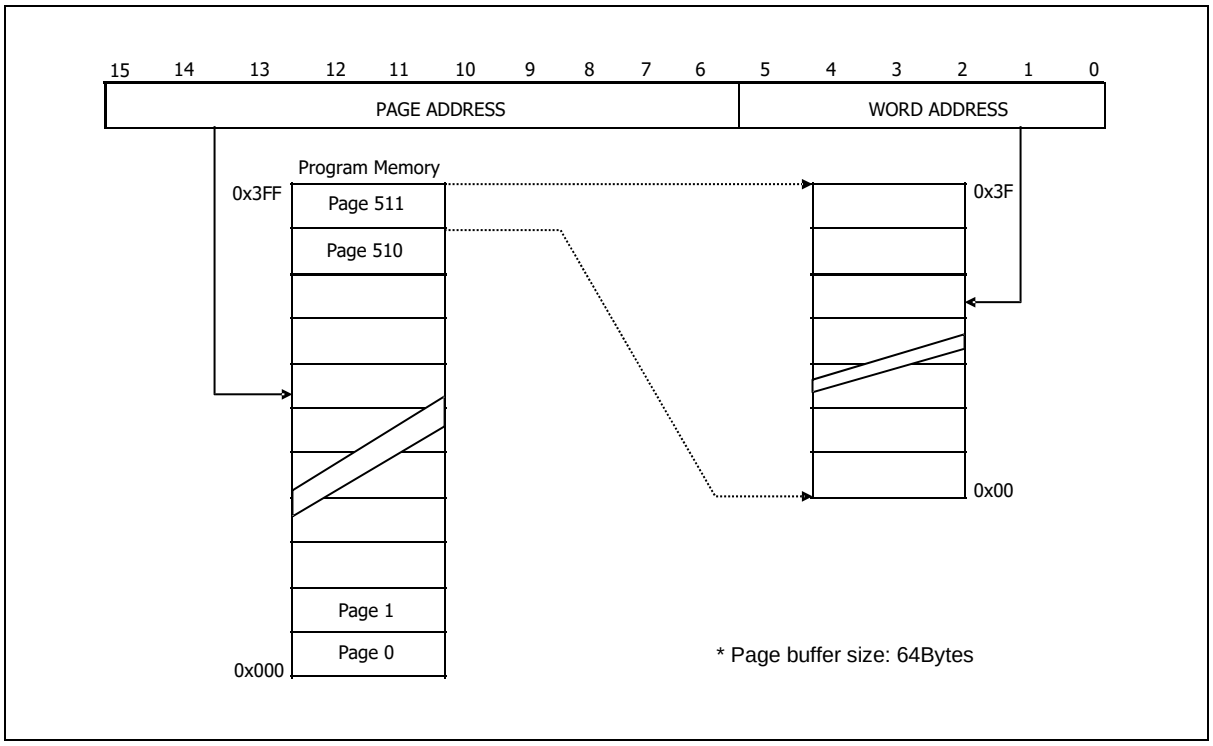


Figure 34. Address Configuration of Flash Memory

21.1.2 Data EEPROM memory map

Data EEPROM memory uses 2K bytes of flash memory. It is read by byte and written by byte or page. One page is 32-bytes

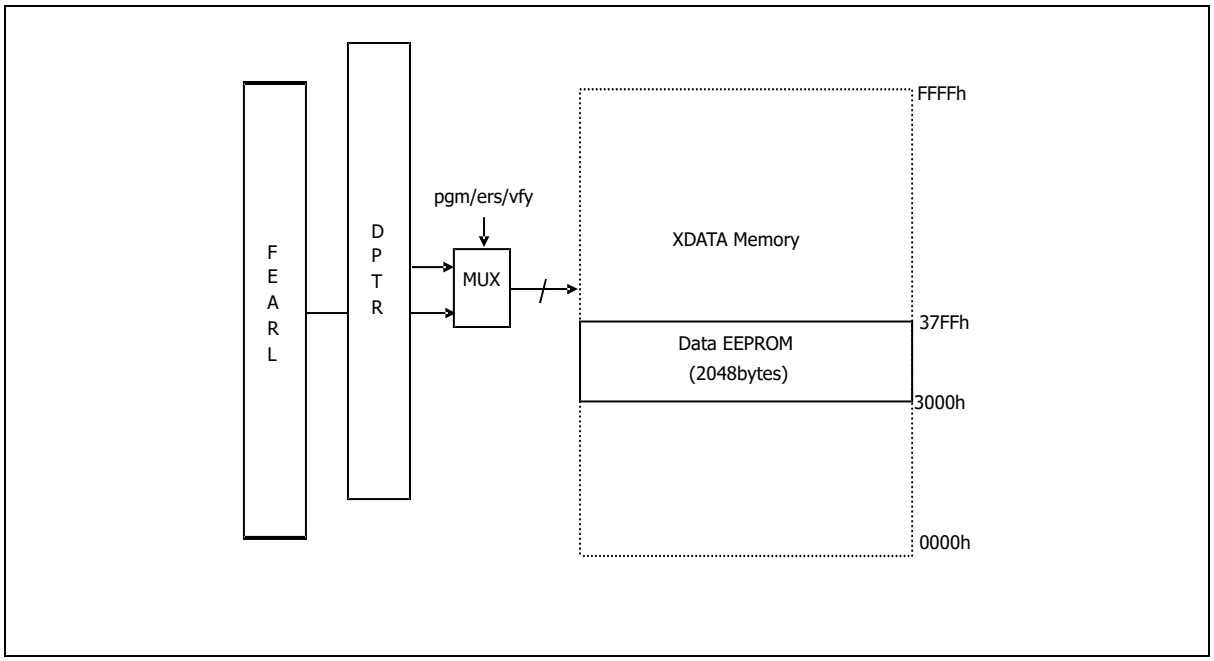


Figure 35. Data EEPROM Memory Map

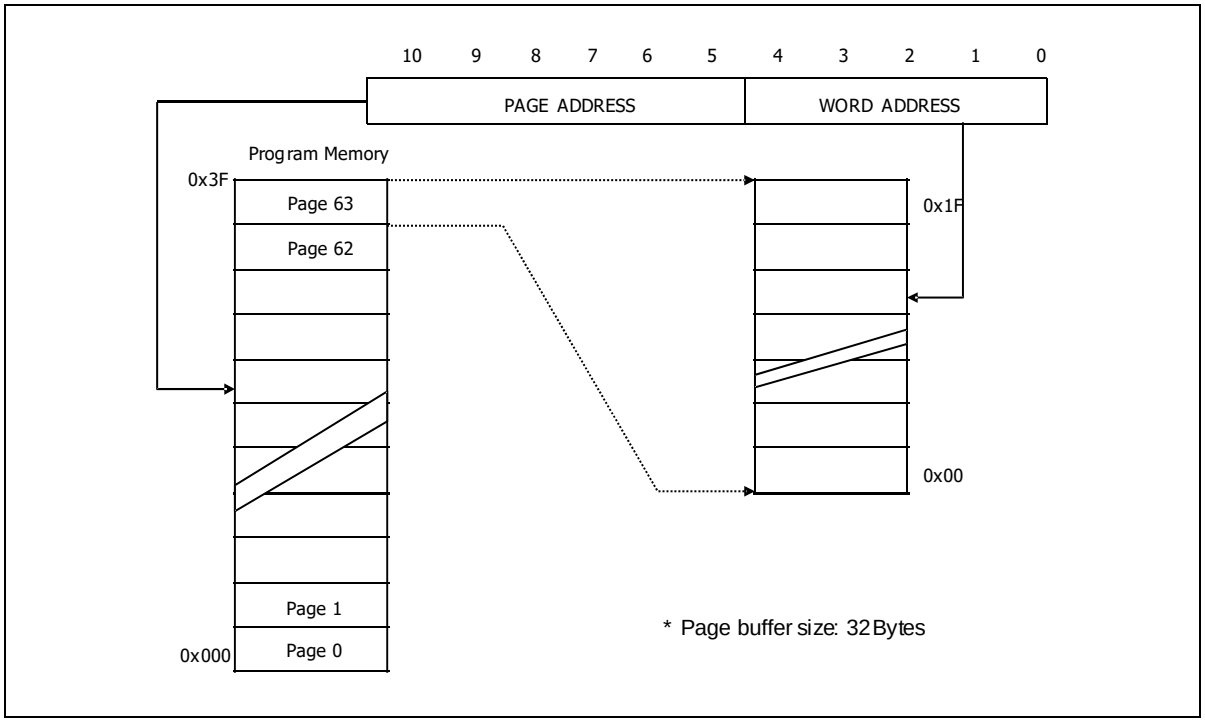


Figure 36. Address Configuration of Data EEPROM Memory

22 Electrical characteristics

22.1 Absolute maximum ratings

Table 19. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V_I	-0.3 ~ VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 ~ VDD+0.3	V	
	I_{OH}	42.5	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	112	mA	Maximum current ($\sum I_{OH}$)
	I_{OL1}	50	mA	Maximum current (I_{OL1} per I/O pin)
	$\sum I_{OL1}$	101	mA	Maximum current ($\sum I_{OL1}$)
	I_{OL2}	160	mA	Maximum current sunk by (I_{OL2} per I/O pin)
	$\sum I_{OL2}$	160	mA	Maximum current by LED Drive ($\sum I_{OL2}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65~+150	°C	–

NOTE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

22.2 Recommended operating conditions

Table 20. Recommended Operating Conditions

(T_A=-40°C ~ 85°C or T_A=-40°C ~ 105°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Operating Voltage	VDD	f_X= 32 ~ 38kHz	Sub Crystal	1.8	–	5.5	V
		f_X= 4 ~12MHz	Main Crystal	2.4	–	5.5	
		f_X= 0.5~16 MHz	Internal RC	1.8	–	5.5	
Operating Temperature	T_{OPR}	VDD=1.8~5.5V		-40	–	85	°C
				-40	-	105	

22.3 A/D converter characteristics

Table 21. A/D Converter Characteristics

(T_A=-40°C ~ +85°C or TA=-40°C ~ 105°C, VDD=2.5V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Integral Linear Error	ILE	VDD=AVDD= 5.0V MCLK = 8MHz		–	±4	±8	LSB
Differential Linearity Error	DLE			–	±1	±2	
Offset Error of Top	EOT			–	±4	±8	
Offset Error of Bottom	EOB			–	±2	±4	
Conversion Time	t_{CON}	12-bit resolution, 8MHz		7.5	–	–	us
Analog Input Voltage	V_{AN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	*Note 3		1.8	–	VDD	
Analog Input Leakage Current	I_{AN}	VDDREF=5.12V		–	–	2	uA
ADC Operating Current	I_{ADC}	Enable	VDD=5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

NOTES:

1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. Full scale error is the difference between 111111111111 and the converted output for full-scale input voltage (AVREF).
3. When AVREF is lower than 2.5V, the ADC resolution is worse.

22.4 BGR characteristics

Table 22. BGR Characteristics

(T_A=-40°C ~ +85°C or TA=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
BGR Reference Voltage	V_{BGR}	T_A=+25°C	1.164	1.200	1.236	V
		T_A=-40°C ~ +85°C	1.146	1.200	1.254	
		T_A=-40°C ~ +105°C	1.140	1.200	1.260	

22.5 Power on reset characteristics

Table 23. Power-on Reset Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESET Release Level	V_{POR}	–	–	1.32	–	V
VDD Voltage Rising Time	t_R	–	20	–	20,000	us/V
VDD Voltage Falling Time	t_f		400	–	20,000	us/V
Minimum Pulse Width	t_{LW}	–	100			us
POR Current	I_{POR}	–	–	0.2	–	uA

22.6 Low voltage reset and low voltage indicator characteristics

Table 24. LVR and LVI Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels. But LVI can select other levels except 1.61/1.68/1.77V because the minimum operation voltage is 1.8V. VLVR/VLVI can be measured when voltage drops (falling level).		-	1.61	1.75	V
				1.55	1.68	1.81	
				1.63	1.77	1.91	
				1.73	1.88	2.03	
				1.84	2.00	2.16	
				1.96	2.13	2.30	
				2.10	2.28	2.46	
				2.26	2.46	2.66	
				2.47	2.68	2.89	
				2.59	2.81	3.03	
				2.82	3.06	3.30	
				2.95	3.21	3.47	
				3.28	3.56	3.84	
				3.43	3.73	4.03	
				3.60	3.91	4.22	
				3.91	4.25	4.59	
Hysteresis	△V	–		–	30	180	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
VDD Voltage Rising Time	t_R	–		20	–	20,000	us/V
VDD Voltage Falling Time	t_f			400	–	20,000	us/V
LVR and LVI Current	I_{BL}	Enable (Both)	VDD= 3V, RUN Mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)	VDD= 3V	–	–	0.1	

NOTE: Guaranteed by design.

22.7 High speed internal RC oscillator characteristics

Table 25. High Speed Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Frequency	f_{IRC}	V_{DD} = 2.0 – 5.5V		–	32	–	MHz
Tolerance	–	T_A = 0°C to +50°C	With 0.1uF Bypass capacitor	–	–	±1.5	%
		T_A = -40°C to +85°C				±2.0	
		T_A = -40°C to +105°C				±3.0	
Clock Duty Ratio	TOD	–		40	50	60	%
Stabilization Time	T_{HFS}	–		–	–	100	us
IRC Current	I_{IRC}	Enable		–	0.2	–	mA
		Disable		–	–	0.1	uA

NOTE: A 0.1uF bypass capacitor should be connected to VDD and VSS.

22.8 Low speed internal RC oscillator characteristics

Table 26. Low Speed Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	f_{LSI}	TA=-40°C ~ +85°C	102	128	154	kHz
		TA=-40°C ~ +105°C	90	128	166	
Stabilization Time	T_{LSI}	–	–	–	1	ms
LSI Current	I_{LSI}	Enable	–	1	–	uA
		Disable	–	–	0.1	

22.9 DC characteristics

Table 27. DC Characteristics

(T_A= -40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD= 1.8V ~ 5.5V, VSS= 0V, f_{XIN}= 16MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	All input pins	0.7VDD	–	VDD	V
Input Low Voltage	V_{IL}	All input pins	–	–	0.3VDD	V
Output High Voltage	V_{OH1}	VDD=4.5V, IOH=-8.57mA, All output ports;	VDD-1.0	–	–	V
	V_{OH2}	VDD=5V, IOH= -18 mA, T_A= 25°C, P1x output ports	VDD-0.7	–	–	V
	V_{OH3}	VDD=4.5V, IOH= -19 mA, P1x output ports	VDD-2.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=4.5V, IOL= 10mA, All output ports except V_{OL2}	–	–	1.0	V
	V_{OL2}	VDD=5.0V, IOL= 160mA, T_A= 25°C P3x High sink current output	–	1.5	3	V
Input High Leakage Current	I_{IH}	All input ports	–	–	1	uA
Input Low Leakage Current	I_{IL}	All input ports	-1	–	–	uA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A= 25°C All Input ports, VDD=5.0V	25	50	100	KΩ
OSC feedback resistor	R_{X1}	XIN= VDD, XOUT= VSS T_A= 25°C, VDD= 5V	0.76	1.3	10.51	MΩ
	R_{X2}	SXIN=VDD, SXOUT=VSS T_A= 25°C, VDD=5V	6.25	13.53	36.98	MΩ

Table 27. DC Characteristics (continued)

(T_A= -40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD= 1.8V ~ 5.5V, VSS= 0V, f_{XIN}= 16MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Current	I_{DD1}(RUN)	f_{XIN}= 12MHz, VDD= 5V	–	2.5	-	mA
		f_{XIN}= 8MHz, VDD= 5V	–	2.0	-	mA
		f_{XIN}= 4MHz, VDD= 5V	–	1.5	-	mA
		f_{HSI}= 16MHz, VDD= 5V	0.7	-	4.0	mA
	I_{DD2}(IDLE)	f_{XIN}= 12MHz, VDD= 5V	–	1.8	-	mA
		f_{XIN}= 8MHz, VDD= 5V	–	1.5	-	mA
		f_{HSI}= 16MHz, VDD= 5V	0.5	-	3.0	mA
	I_{DD3}(STOP1)	STOP @ WDT on, VDD= 5.5V, T_A= 25°C	–	-	22.0	uA
	I_{DD4}(STOP2)	STOP @ WDT off & LVR off, VDD= 5.5V, T_A= 25°C	–	-	7.0	uA

NOTES:

1. Where the f_{XIN} is an external main oscillator, f_{SUB} is an external sub oscillator, the f_{HSIRC} and f_{LSIRC} are an internal RC oscillator, and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

22.10 AC characteristics

Table 28. AC Characteristics

(T_A= -40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD= 1.8V ~ 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESETB input low width	t_{RSL}	Input, VDD= 5V	50	–	–	us
Interrupt input high, low width	t_{INTH}, t_{INTL}	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	ECn, V_{DD} = 5V (n= 0, 1, 3)	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	Ecn, V_{DD} = 5V (n= 0, 1, 3)	20	–	–	

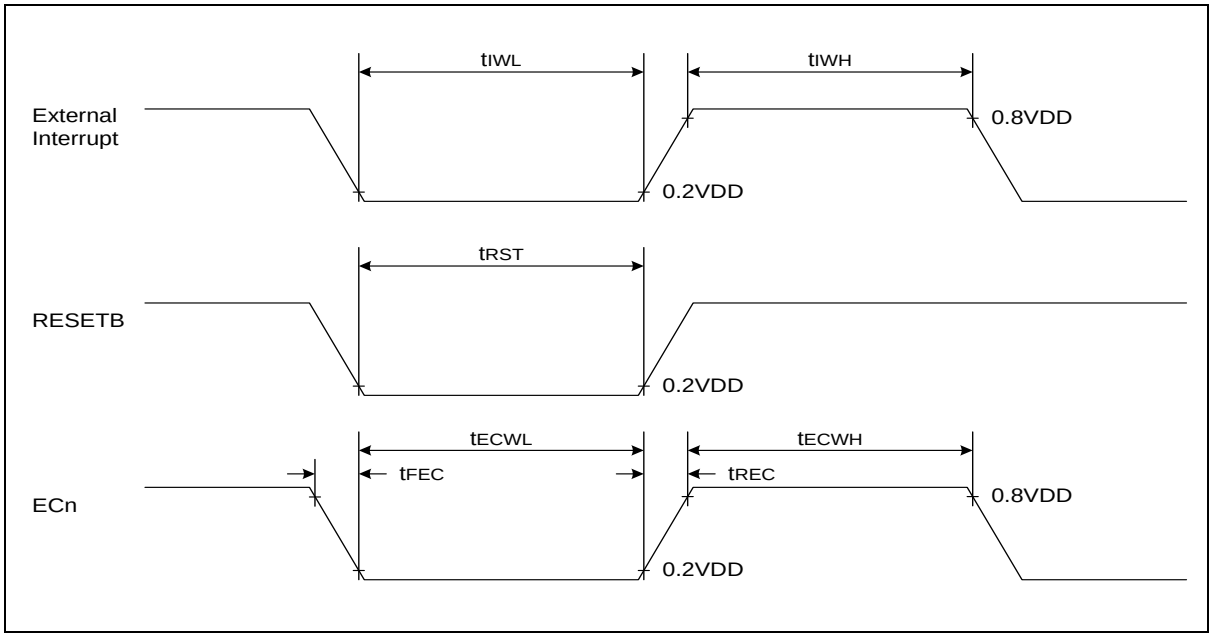


Figure 37. AC Timing

22.11 USART characteristics

The following table and figures show USART timing condition in SPI or Synchronous mode operation.

Table 29. USART Timing Characteristics in SYNC. Or SPI Mode Operations

(T_A= -40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Parameter		Symbol	Min.	Max.	Unit
System clock period(0.5MHz~16MHz)		t_{SCLK}	62.5	2000	ns
Clock (XCK) period		t_{XCK}	4 x t_{SCLK}	1028 x t_{SCLK}	ns
Clock (XCK) high time		t_{XCKH}	2 x t_{SCLK}	514 x t_{SCLK}	ns
Clock (XCK) low time		t_{XCKL}	2 x t_{SCLK}	514 x t_{SCLK}	ns
Lead time	Master Slave	t_{LEAD} t_{LEAD}	0.5 x t_{XCK} 2 x t_{SCLK}	0.5 x t_{XCK} –	ns
Lag time	Master Slave	t_{LAG} t_{LAG}	0.5 x t_{XCK} 2 x t_{SCLK}	0.5 x t_{XCK} –	ns
Data setup time (inputs)	Master Slave	t_{SIM} t_{SIS}	2 x t_{SCLK} 2 x t_{SCLK}	2 x t_{SCLK} 2 x t_{SCLK}	ns
Data hold time (inputs)	Master Slave	t_{HIM} t_{HIS}	10 10	– –	ns
Data setup time (outputs)	Master Slave	t_{SOM} t_{SOS}	2 x t_{SCLK} 2 x t_{SCLK}	2 x t_{SCLK} 2 x t_{SCLK}	ns
Data hold time (outputs)	Master Slave	t_{HOM} t_{HOS}	-10 -10	– –	ns
Disable time		t_{DIS}	1 x t_{SCLK}	2 x t_{SCLK}	ns

NOTES:

1. In synchronous mode, Lead and Lag time for SS pin is ignored. And the case of “UCPHA=0” is also only applied to SPI mode
2. All timing is shown between 20% VDD and 80% VDD.

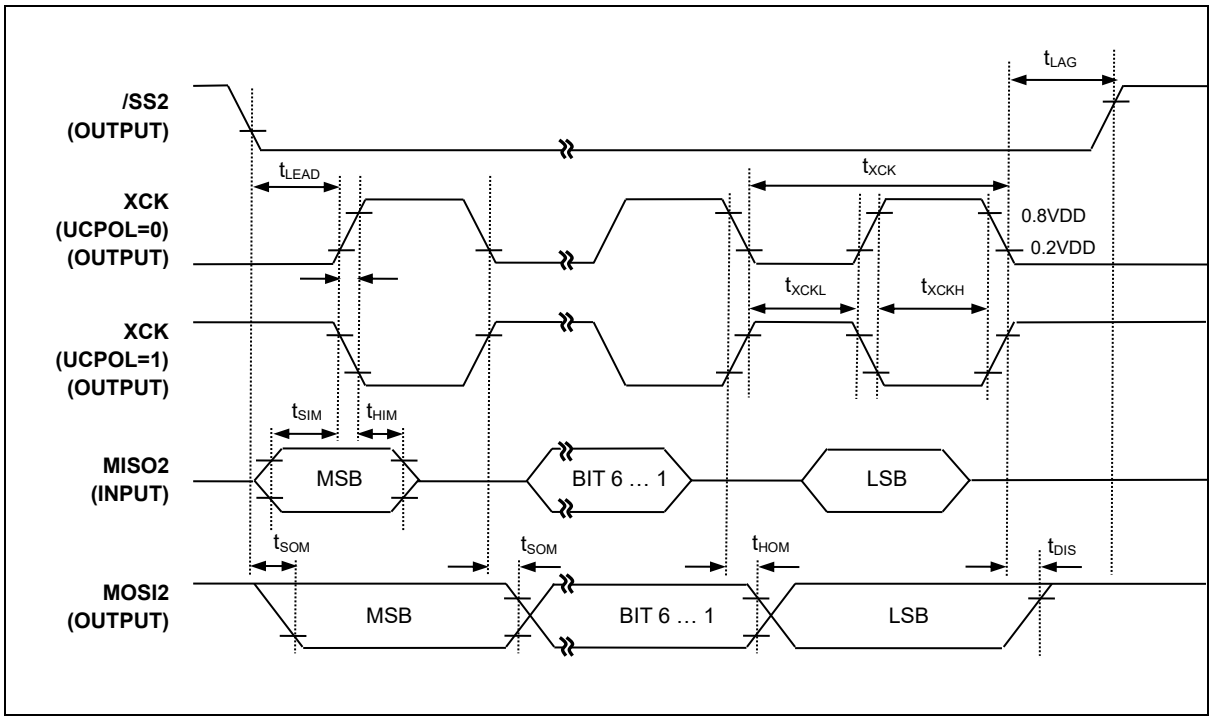
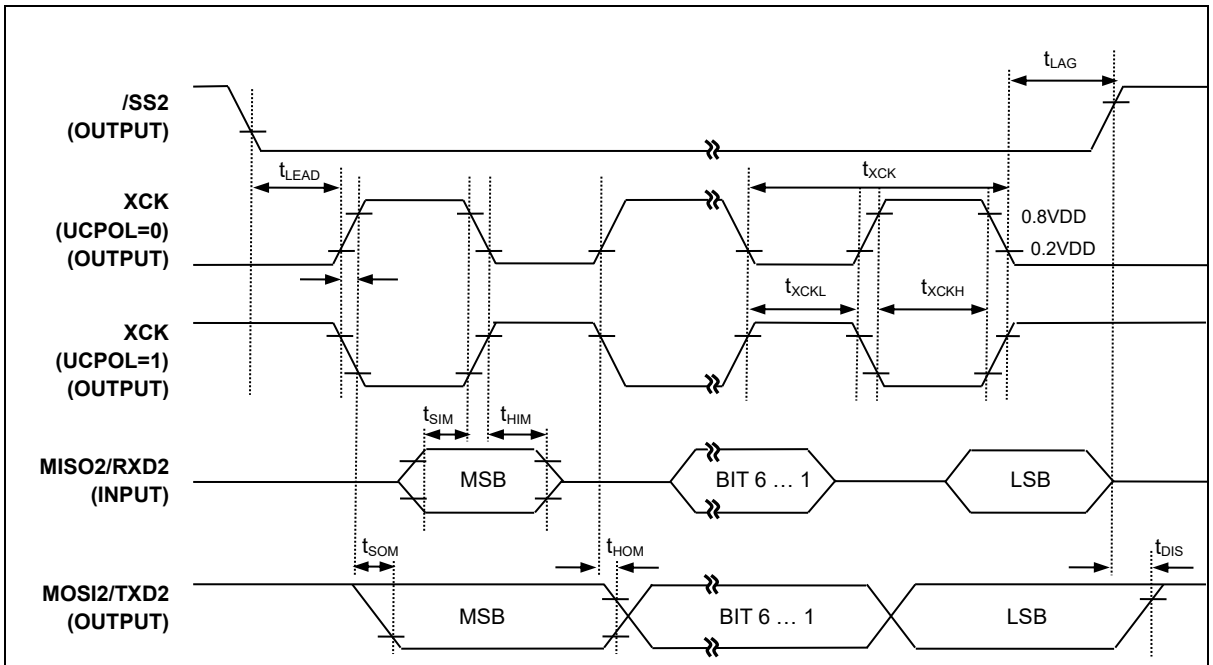


Figure 38. SPI Master Mode Timing (UCPHA = 0, MSB First)



NOTE: When in Synchronous mode, the START bit becomes MSB and the 1st or 2nd STOP bit becomes LSB.

Figure 39. SPI/Synchronous Master Mode Timing (UCPHA = 1, MSB First)

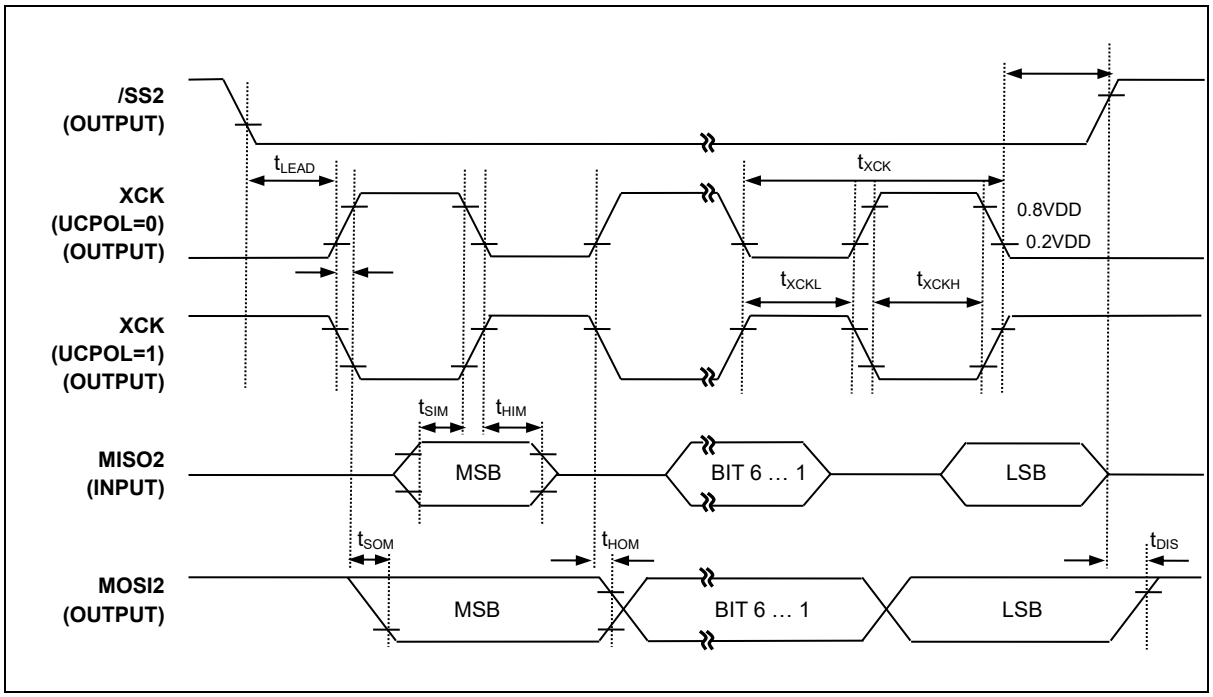
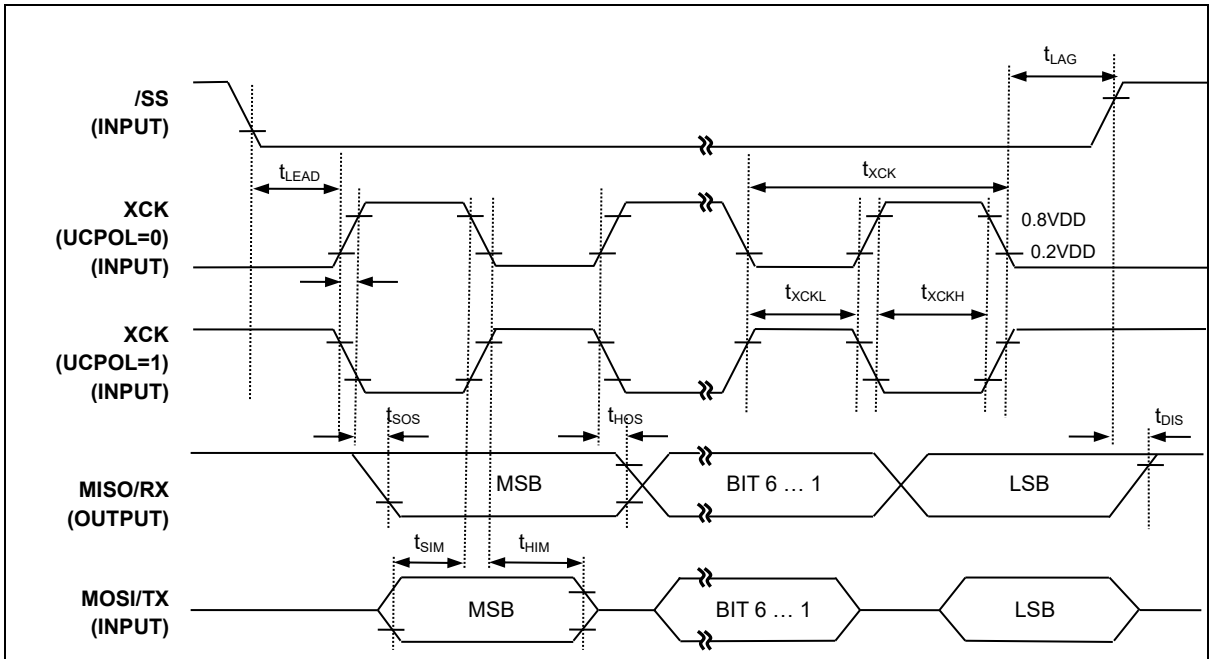


Figure 40. SPI Slave Mode Timing (UCPHA = 0, MSB First)



NOTE: When in Synchronous mode, the START bit becomes MSB and the 1st or 2nd STOP bit becomes LSB.

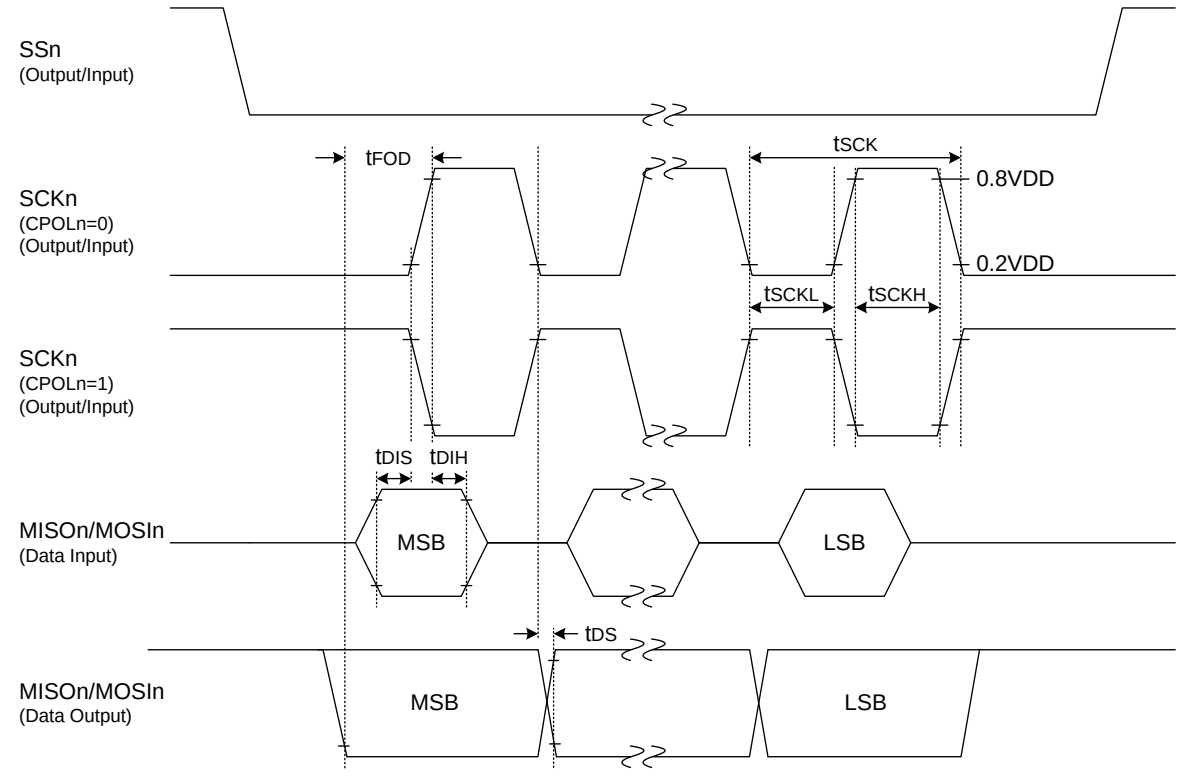
Figure 41. SPI/Synchronous Slave Mode Timing (UCPHA = 1, MSB First)

22.12 SPI0/1 characteristics

Table 30. SPI0/1/2 Characteristics

(T_A=-40°C– +85°C or T_A=-40°C ~ 105°C, VDD=1.8V – 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Clock Pulse Period	tSCK	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	tSCKH, tSCKL	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width		External SCK source	70	–	–	
First Output Clock Delay Time	tFOD	Internal/External SCK source	100	–	–	
Output Clock Delay Time	tDS	–	–	–	50	
Input Setup Time	tDIS	–	100	–	–	
Input Hold Time	tDIH	–	150	–	–	



NOTE: n =0, 1 and 2

Figure 42. SPI0/1/2 Timing

22.13 UART0/1 characteristics

Table 31. UART0/1 Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, f_{XIN}=8MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial port clock cycle time	t_{SCK}	1800	t_{CPU} x 16	2200	ns
Output data setup to clock rising edge	t_{S1}	810	t_{CPU} x 13	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	t_{CPU}- 50	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	720	t_{CPU} x 8	1280	

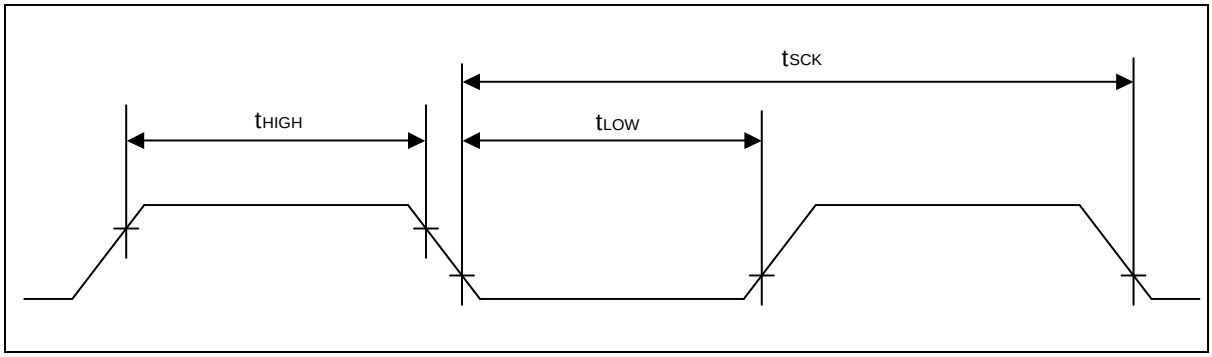


Figure 43. Waveform for UART0/1 Timing Characteristics

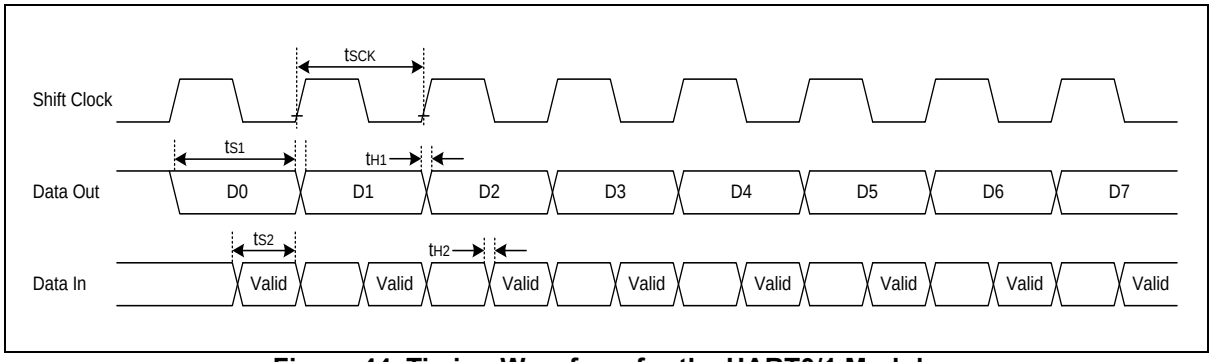


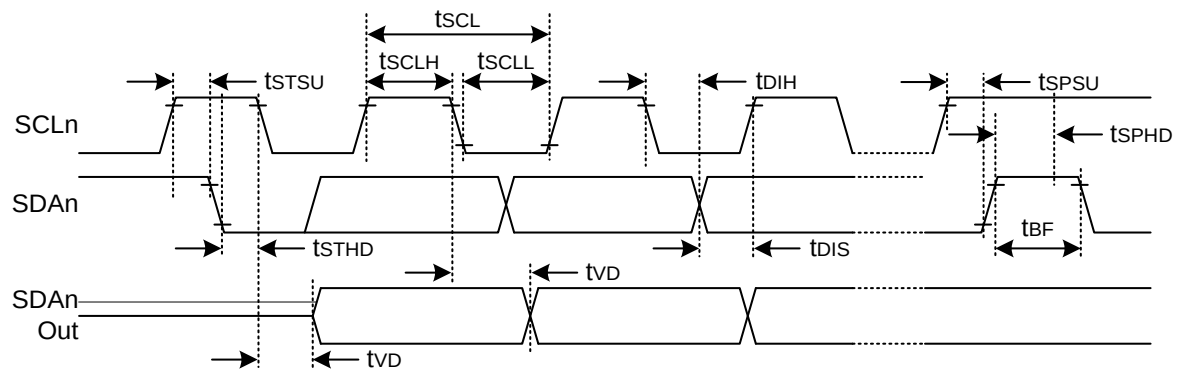
Figure 44. Timing Waveform for the UART0/1 Module

22.14 I2C0/1 characteristics

Table 32. I2C0/1 Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Parameter	Symbol	Standard mode		High-speed mode		Unit
		Min.	Max.	Min.	Max.	
Clock frequency	tSCL	0	100	0	400	kHz
Clock High Pulse Width	tSCLH	4.0	–	0.6	–	us
Clock Low Pulse Width	tSCLL	4.7	–	1.3	–	
Bus Free Time	tBF	4.7	–	1.3	–	
Start Condition Setup Time	tSTSU	4.7	–	0.6	–	
Start Condition Hold Time	tSTHD	4.0	–	0.6	–	
Stop Condition Setup Time	tSPSU	4.0	–	0.6	–	
Stop Condition Hold Time	tSPHD	4.0	–	0.6	–	
Output Valid from Clock	tVD	0	–	0	–	
Data Input Hold Time	tDIH	0	–	0	1.0	
Data Input Setup Time	tDIS	250	–	100	–	ns



NOTE: n= 0, and 1

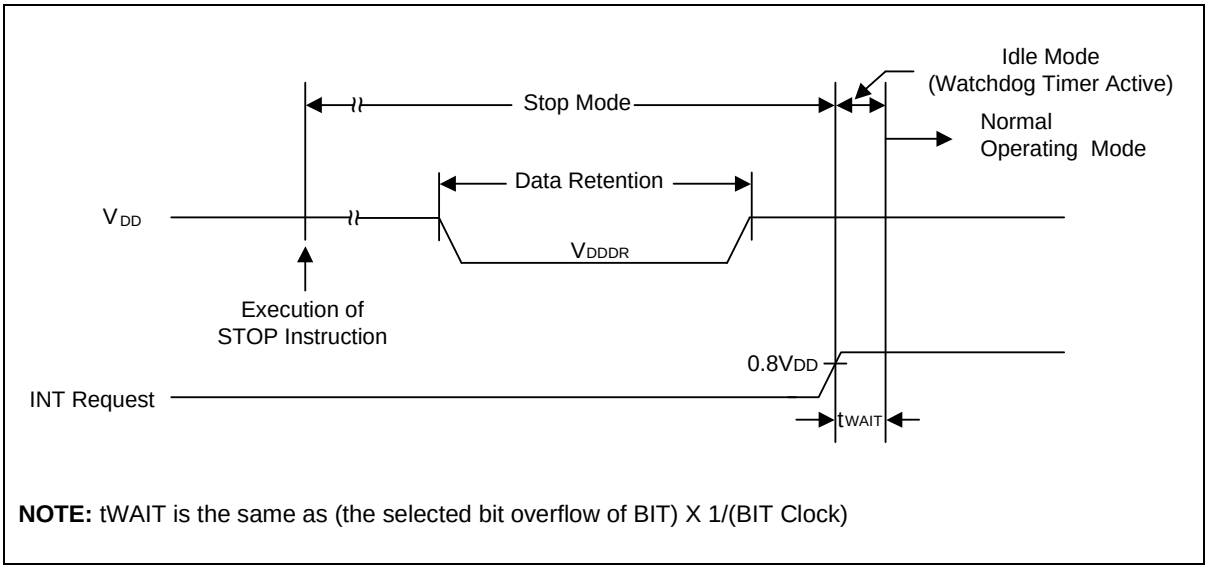
Figure 45. I2C0/1 Timing

22.15 Data retention voltage in Stop mode

Table 33. Data Retention Voltage in Stop Mode

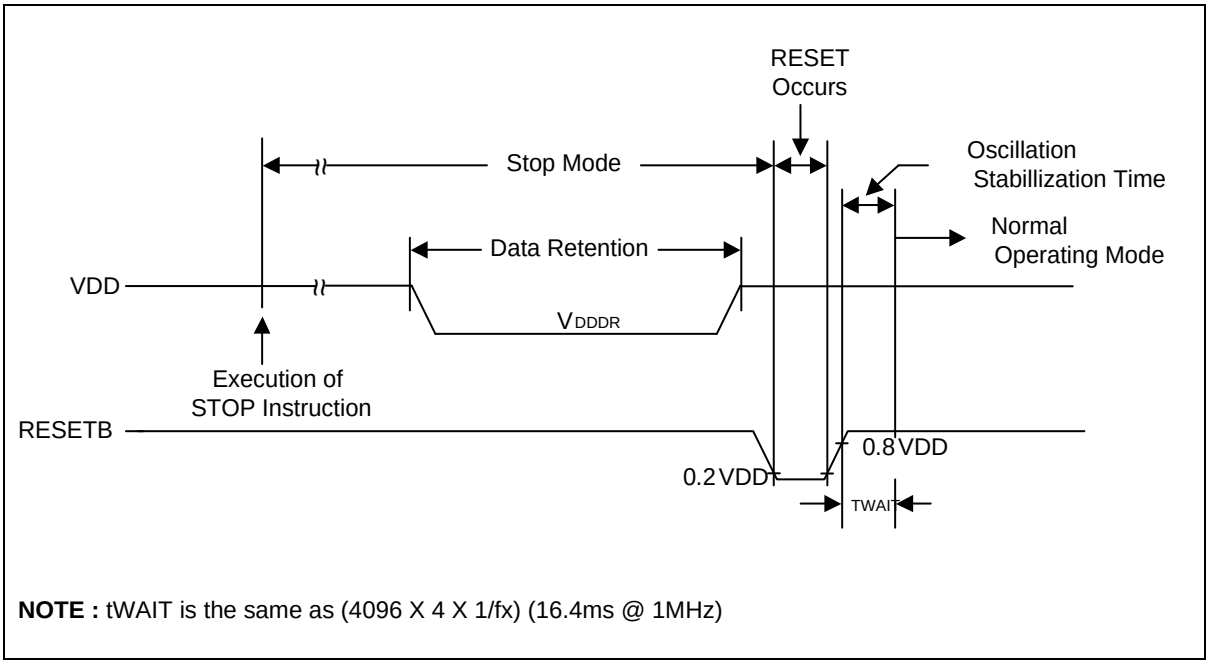
(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	VDDR= 1.8V, (TA= 25°C), Stop mode	–	–	1	uA



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 46. Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 1/fx) (16.4ms @ 1MHz)

Figure 47. Stop Mode Release Timing when Initiated by RESETB

22.16 Internal Flash ROM characteristics

Table 34. Internal Flash ROM Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE}	–	–	–	30,000	times

NOTE: During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

22.17 Input/output capacitance

Table 35. Input/Output Capacitance

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	fx= 1MHz	–	–	10	pF
Output Capacitance	C_{OUT}	Unmeasured pins are				
I/O Capacitance	C_{IO}	connected to VSS				

22.18 LCD Driver characteristics

Table 36. LCD Driver characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=2.7V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
LCD voltage	VLC0	LCD contrast = Disable, 1/4 bias	–	–	–	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 00H	Typ.x0.94	V_{DD} x 16/31	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 01H	Typ.x0.94	V_{DD} x 16/30	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 02H	Typ.x0.94	V_{DD} x 16/29	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 03H	Typ.x0.94	V_{DD} x 16/28	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 04H	Typ.x0.94	V_{DD} x 16/27	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 05H	Typ.x0.94	V_{DD} x 16/26	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 06H	Typ.x0.94	V_{DD} x 16/25	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 07H	Typ.x0.94	V_{DD} x 16/24	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 08H	Typ.x0.94	V_{DD} x 16/23	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 09H	Typ.x0.94	V_{DD} x 16/22	Typ.x1.06	V

Table 36. LCD Driver characteristics (continued)

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=2.7V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
LCD voltage	VLC0	LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 0AH	Typ.x0.94	V_{DD} x 16/21	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 0BH	Typ.x0.94	V_{DD} x 16/20	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 0CH	Typ.x0.94	V_{DD} x 16/19	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 0DH	Typ.x0.94	V_{DD} x 16/18	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 0EH	Typ.x0.94	V_{DD} x 16/17	Typ.x1.06	V
		LCD contrast = Enable, 1/4 bias, No panel load, VLCD[3:0] = 0FH	Typ.x0.94	V_{DD} x 16/16	Typ.x1.06	V
LCD mid bias voltage	VLC1	V_{DD} = 2.7V to 5.5V, LCD clock = 0Hz, 1/4 bias, No panel load	Typ – 0.2	3/4 x VLC0	Typ + 0.2	V
	VLC2		Typ – 0.2	2/4 x VLC0	Typ + 0.2	
	VLC3		Typ – 0.2	1/4 x VLC0	Typ + 0.2	
LCD Driver output impedance	R_{LO}	VLCD = 3.0V	–	5	10	kΩ
LCD bias dividing resistor	RLCD1	1/4 bias, T_A = 25°C	7.5	10	12.5	kΩ
	RLCD2		38	50	62	kΩ
	RLCD3		60	80	100	kΩ
	RLCD4		180	240	300	kΩ

NOTES:

1. The specifications of the parameters are guaranteed by design.
2. It is middle output voltage when the VDD and the VLC0 node are connected.

22.19 Main clock oscillator characteristics

Table 37. Main Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=2.4V ~ 5.5V)

Oscillator	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal	Main oscillation frequency	2.4V – 5.5V	4	–	12.0	MHz
Ceramic Oscillator	Main oscillation frequency	2.4V – 5.5V	4	–	12.0	MHz
External Clock	XIN input frequency	2.4V – 5.5V	4	–	10.0	MHz
		2.4V – 5.5V	4	–	12.0	MHz

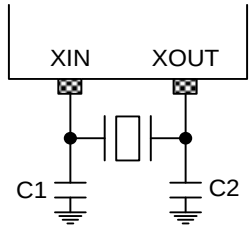


Figure 48. Crystal/Ceramic Oscillator

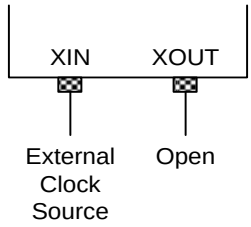


Figure 49. External Clock

22.20 Sub-clock oscillator characteristics

Table 38. Sub Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal	Sub oscillation frequency	1.8V – 5.5V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	kHz

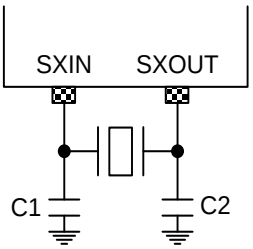


Figure 50. Crystal Oscillator

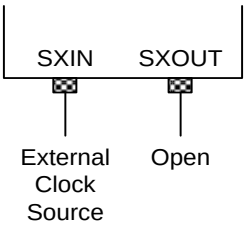


Figure 51. External Clock

22.21 Main oscillation stabilization characteristics

Table 39. Main Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	Min.	Typ.	Max.	Unit
Crystal	fx > 4MHz, VDD = 2.7V ~ 5.5V,	–	–	15	ms
	fx > 1MHz, VDD = 1.8V, T_A=-40°C	–	–	60	ms
Ceramic	–	–	–	10	ms
External Clock	f_{XIN} = 4 to 12MHz XIN input high and low width (t_{XH}, t_{XL})	42	–	1250	ms

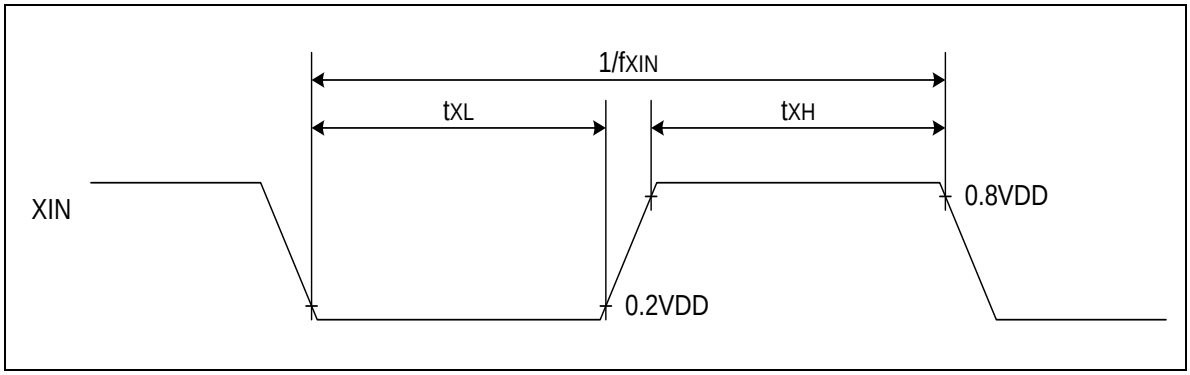


Figure 52. Clock Timing Measurement at XIN

22.22 Sub-oscillation characteristics

Table 40. Sub Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	Min.	Typ.	Max.	Unit
Crystal	T_A=-40°C ~+85°C	–	–	10	s
	T_A= 25°C		500		ms
External Clock	SXIN input high and low width (t_{XH}, t_{XL})	5	–	15	us

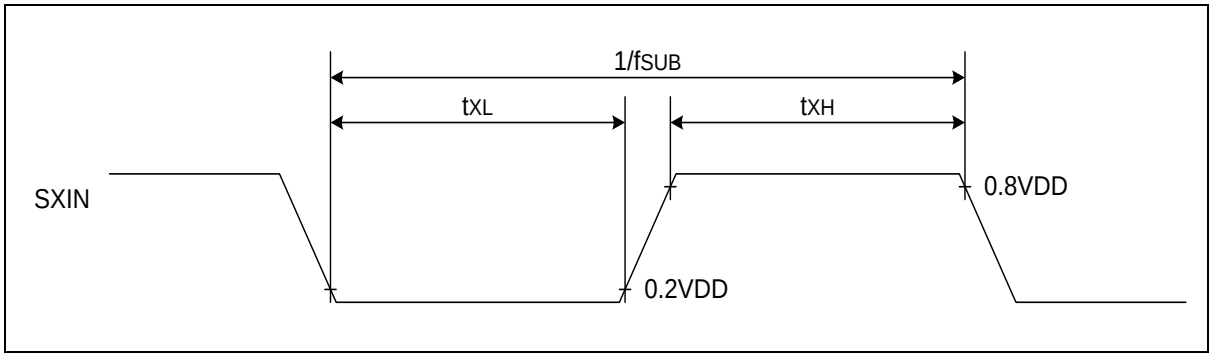


Figure 53. Clock Timing Measurement at SXIN

22.23 Operating voltage range

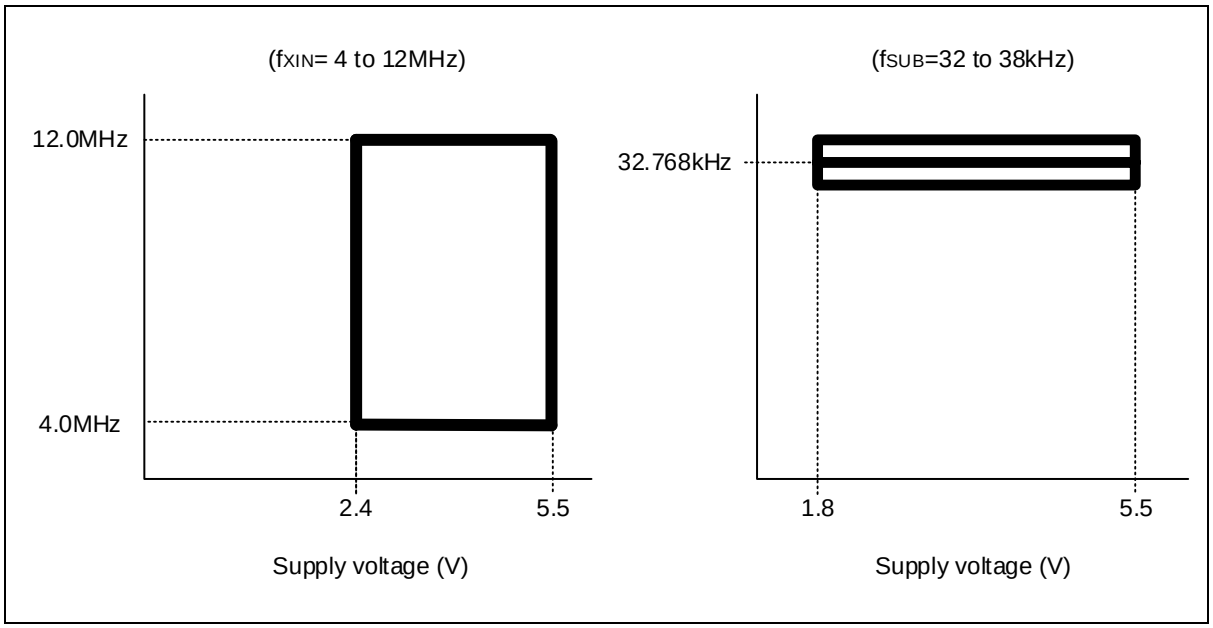


Figure 54. Operating Voltage Range

22.24 Recommended circuit and layout

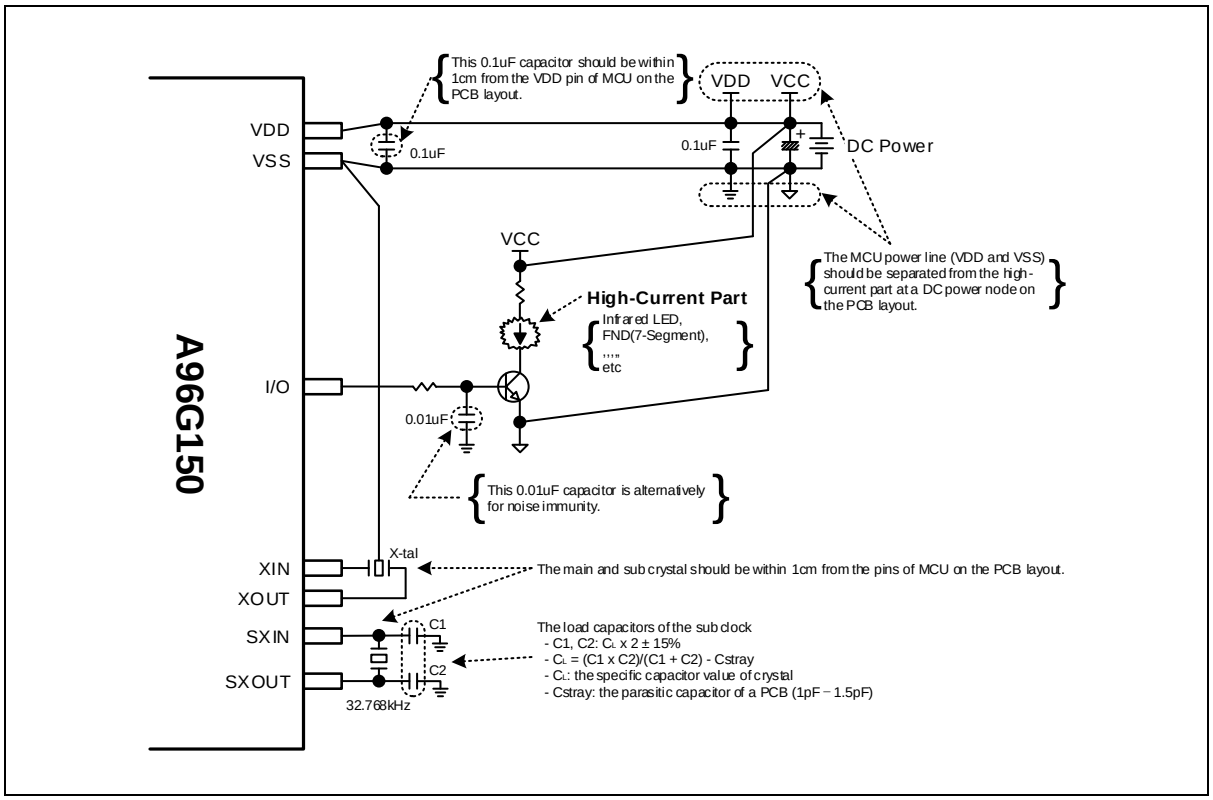


Figure 55. Recommended Voltage Range

22.25 Typical characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean – 3σ) respectively where σ is standard deviation.

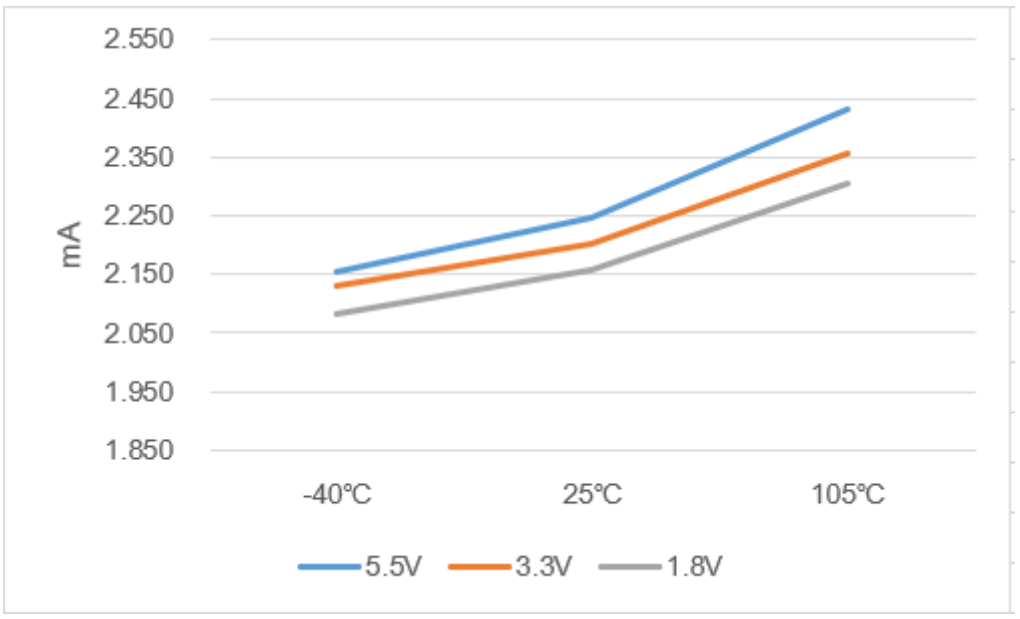


Figure 56. RUN (IDD1) Current

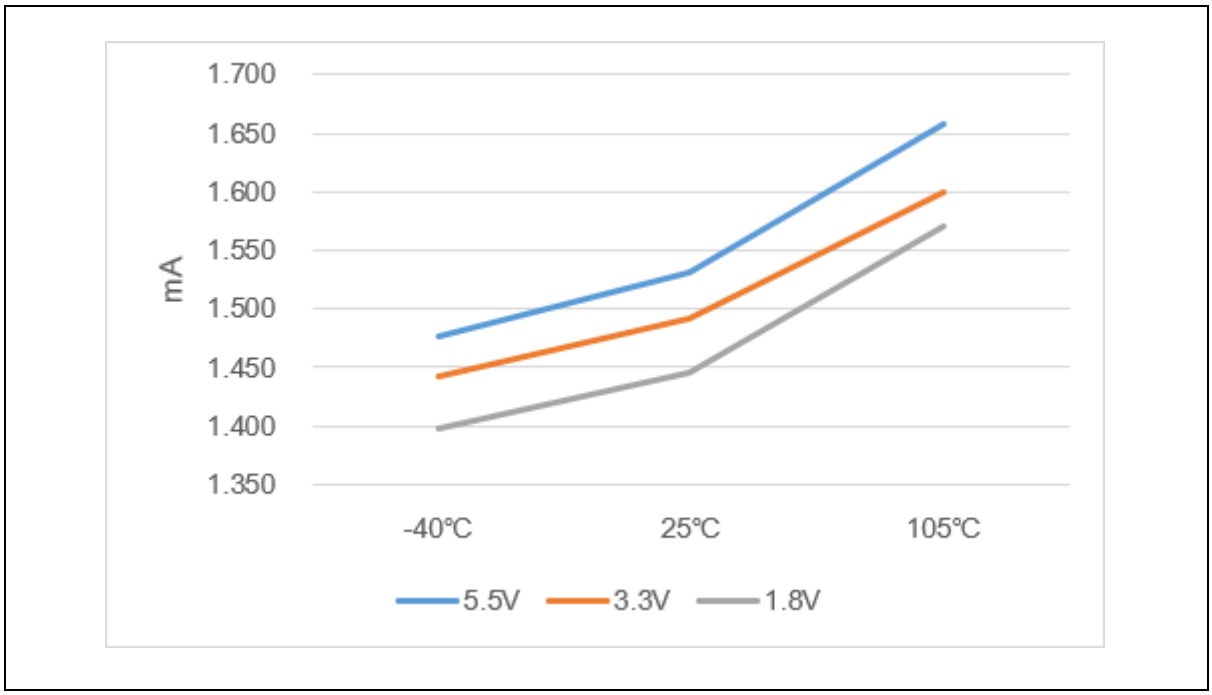


Figure 57. IDLE (IDD2) Current

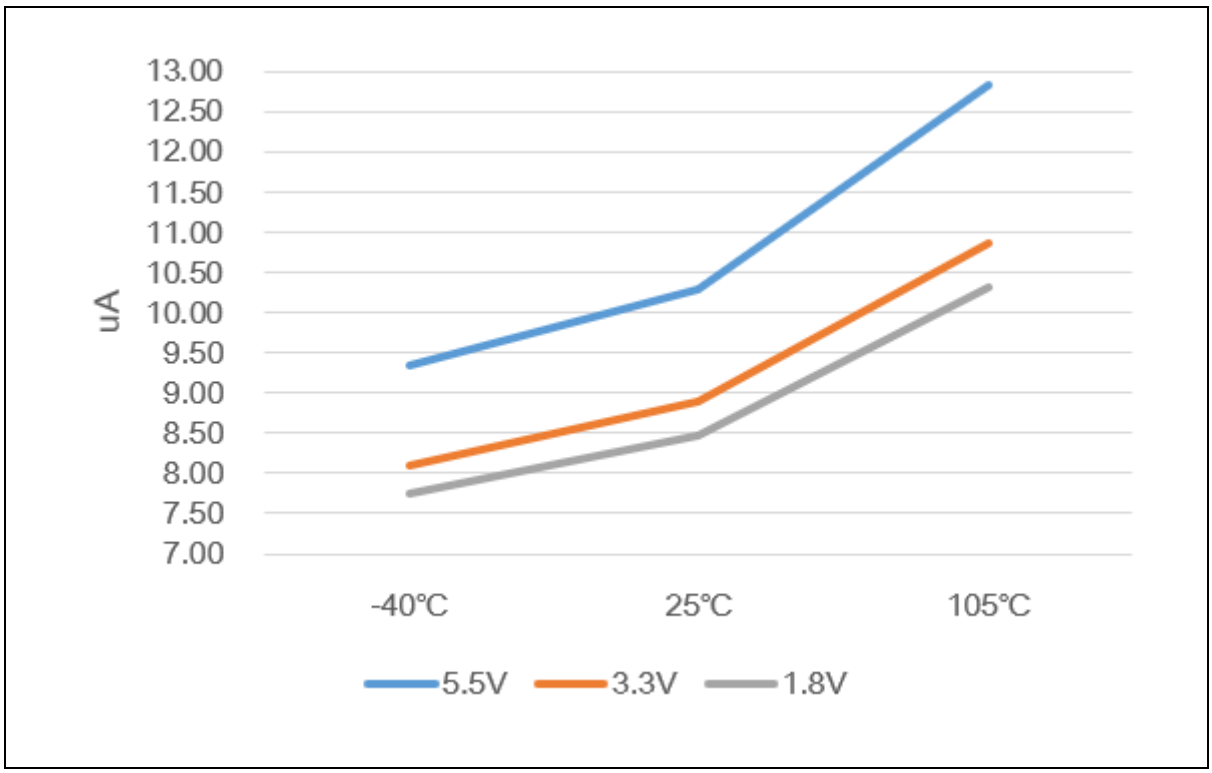


Figure 58. STOP1 (IDD3) Current

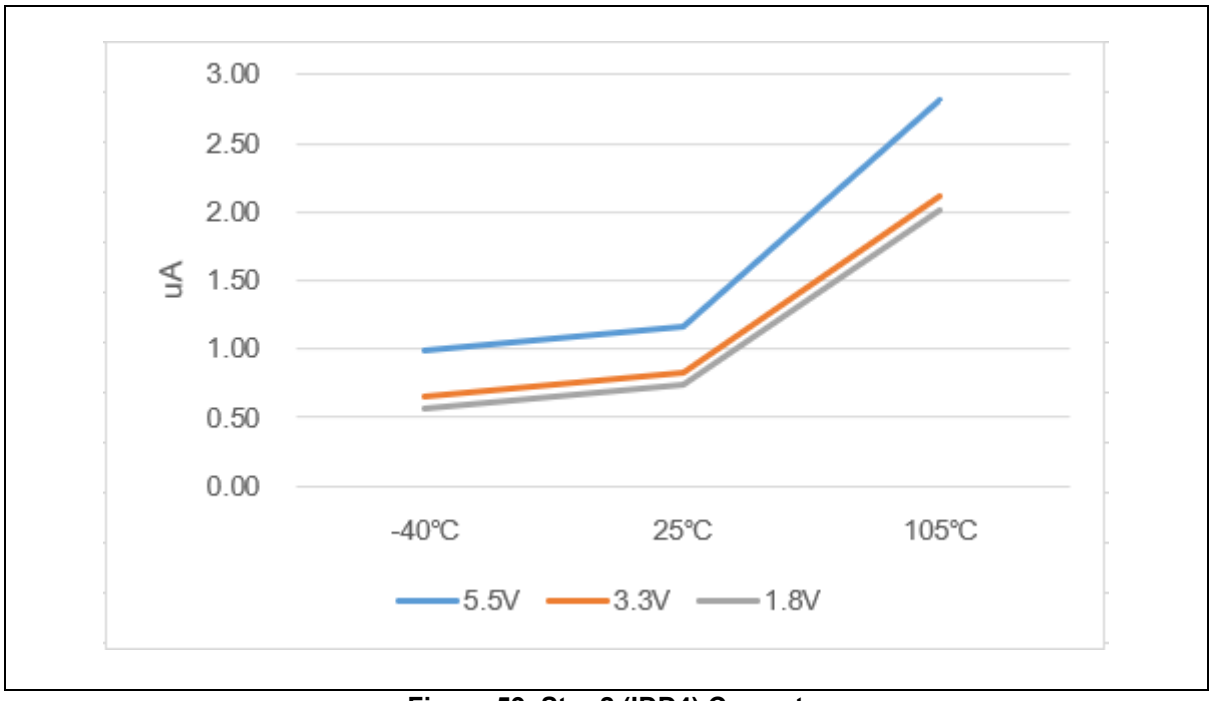


Figure 59. Stop2 (IDD4) Current

23 Development tools

This chapter introduces a wide range of development tools for microcontrollers. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

23.1 Compiler

ABOV semiconductor does not provide any compiler for A96G150. It is recommended to consult a compiler provider.

Since A96G150 has Mentor 8051 as its core, and ROM is smaller than 64Kbytes in size, a developer can use any standard 8051 compilers of other providers.

23.2 Core and debug tool information

ABOV's microcontroller uses OCD (On-Chip Debugger) interface for debugging, which is ABOV's own interface. The OCD monitors and controls the core and supports the read and write operations of external memory and devices. In addition, it supports memory monitoring and break functions.

Debug interfaces such as an OCD interface enable a microcontroller to write on internal programmable memory, thereby, allow it to support ISP (In-system Program) which making possible to write as a single chip or as an embedded chip in the system.

Table 41 provides information of the core and debug emulation interface.

Table 41. Core and Debug Information

	Value	Description
Device name	A9xXxxx	
Series	94/ 95/ 96/ 97 series	
Core	M8051/ CM8051	
Extended Stack Pointer	Yes/ no	94, 97 series only
Debug interface	OCD 1/ OCD 2	
Number of break point	4/ 8	
Real-time monitoring	Yes/ no	OCD 2 only
Run flag port	Yes/ no	OCD 2 option

NOTES:

1. A96G150 has 96 Series core and OCD 1 interface.
2. Also, A96G150 can be operated with OCD II dongle because OCD II dongle includes all of OCD1 function.
3. 95 series core is the old version of 96 Series core.

23.2.1 Feature of 94/96/97 Series core

ABOV's microcontroller contains an M8051/CM8051 core that was made by improving the 8051. The M8051/ CM8051 core is compatible with the 8051. It reduces time of operation cycles and makes development easy by providing the OCD debug function.

ABOV's 8-bit microcontroller has a core of 94 Series, 96 Series, or 97 Series, that is basically compatible with the 8051 series at the instruction set level. A core of each series uses different Debug Interface respectively as shown in Table 42.

Table 42. Core and Debug Interface by Series

	Core	Debug interface
96 Series	M8051	OCD 1
97 Series	M8051	OCD 2
94 Series	CM8051	OCD 2

Features of each series are compared in Table 43.

Table 43. Feature Comparison Chart by Series and Cores

	96 Series	97 Series	94 Series
CPU Core	M8051	M8051	CM8051
Cycle Compatible with MCS51	1/6	1/6	No
OCD Function	OCD 1	OCD 2	OCD 2
Program BUS	8-bit		
Data Bus	8-bit IRAM/ XRAM separated		8-bit single SRAM
EA Auto Clear NOTE1	Yes	Yes	Yes
EA=0, Idle/ Stope Mode Wake up	Yes	Yes	Yes
Interrupt Priority NOTE2	6 group x 4 level	Interrupt x 4 level	Interrupt x 2 level
Nested Interrupt Priority	4 level	4 level	Interrupt x 2 level (max. 4 times)
SFR BUS (read/ write)	Two ports	Two ports	Single port
Stack Extension	X	O	O
Register	SRAM		
Register Bank	4		
CPU/ Flash Clock Ratio	x 1		
Pipeline	No	No	2-stage (IF + ID/ EX)
DHRY Stone Score (I8051: 1.00)	6.0	6.0	8.4
Average Instruction Set Exe. Cycle Compare with i8051	x 6.0	x 6.0	x 6.4
Power Consumption/ DHRY (@synthesis)	52.27uA/ MHz	52.27uA/ MHz	30.19 uA/ MHz

NOTES:

1. A96G150 has 96 Series core and OCD 1 interface. In addition, A96G150 can be operated with OCD II dongle because OCD II dongle includes all of OCD1 function.
2. EA means that All Interrupt Enable bit or Disable bit (Standard 8051).
3. Group: When a programmer selects a specific interrupt (e.g. Interrupt1), the whole interrupts: 0, 6, 12, and 18 have higher priorities.

ABOV's 8-bit microcontrollers maintain the compatibility of binary levels with 8051 cores; however, the cores and series have differences in performances, functions of the core, and debug interfaces.

Through the following sections, you can see the differences of each series.

23.2.2 OCD type of 94/96/97 Series core

96 Series core uses OCD 1 for a debug interface, while the cores of 94 Series and 97 Series use OCD 2 for debug interfaces. The OCD 1 and OCD 2 use the same method in Hardware, but protocols are not compatible each other.

In the OCD 2, it is able to measure the emulation time through the “Run Flag” pin.

Table 44. OCD Type of Each Series

Series	**96 Series**	**97 Series**	**94 Series**	**Remark**
OCD type	OCD 1	OCD 2	OCD 2	

In Table 45, debug interfaces of the OCD 1 and OCD 2 are compared.

Table 45. Comparison of OCD 1 and OCD 2

	Value	**Description**
OCD 1	Break point MAX.8	PC break only
OCD 2	Break point MAX.12	With RAM break Code, XDATA, IDATA 1/8/16/32bit compare
	Real-time monitoring	Code, XDATA, IDATA
	Frequency output	Examine CPU frequency
	Run Flag port	Option for run time measurement

96 Series – OCD 1

This series supports basic operations such as Run, Stop, Step, Break point, register reading/ writing, Memory reading/ writing, and SFR reading/ writing.

94 Series and 97 Series – OCD 2

This series supports the features of the OCD 1 and the features listed below (however, the protocol is not compatible with the OCD1).:

- RTM support: CODE, XDATA, IDATA are updated during the Run Time (Real Time Monitoring available).
- Run Flag support: Emulation Time can be measured in OCD mode (using the Run Flag port).
- RAM Break support: IDATA, SFR, and XDATA break are added.

23.2.3 Interrupt priority of 94/96/97 Series core

In the M8051, users can set interrupt priorities by group. Thus, the 96 Series microcontroller with the basic M8051 core only supports interrupt priorities in group units.

In the 94 Series or 97 Series microcontroller, users can set interrupt priorities to have more functions than the existing functions, and set individual priority over each interrupt source.

Table 46. Interrupt Priorities in Groups and Levels

Series	96 Series	97 Series	94 Series	Remark
Interrupt Priority	6 Grouped 4 Level	Fully 4 Level	Fully 4 Level	96 Series: IP/IP (Interrupt Priority Register) 94, 97 Series: IPxL/IPxH (Interrupt Priority Register)

96 Series

- The priorities by group is available only with IP/IP1 settings.
  - With IP/IP1 settings, users can set interrupt priorities by group unit.
  - The interrupt priority of a group unit (4 interrupts in a group) can be changed to the level between 0 and 3 according to the value of IP/IP1.

94 Series and 97 Series

- The individual interrupt priority can be set by setting IPxL/IPxH(x=0~3).
- The individual interrupt priority can be changed to the level between 0 and 3 according to the value of IPxL/IPxH(x=0~3).

23.2.4 Extended Stack Pointer of 94/96/97 Series core

M8051 uses IRAM area for Stack Pointer. However, 94 Series and 97 Series microcontrollers use not only IRAM area but also XRAM area for Stack Pointer by configuring additional registers.

The setting procedure is as follows:

1. Using the XSP/XSPCR register, you can use XRAM area for Stack Pointer.
2. The XSPCR decides whether to use XRAM for Stack Pointer.
   - If XSPCR='0', IRAM is available for Stack Pointer.
   - If XSPCR='1', XRAM is available for Stack Pointer.
3. The XSP decides a position of XRAM Stack Pointer.
   - This is valid only if XSPCR='1'.

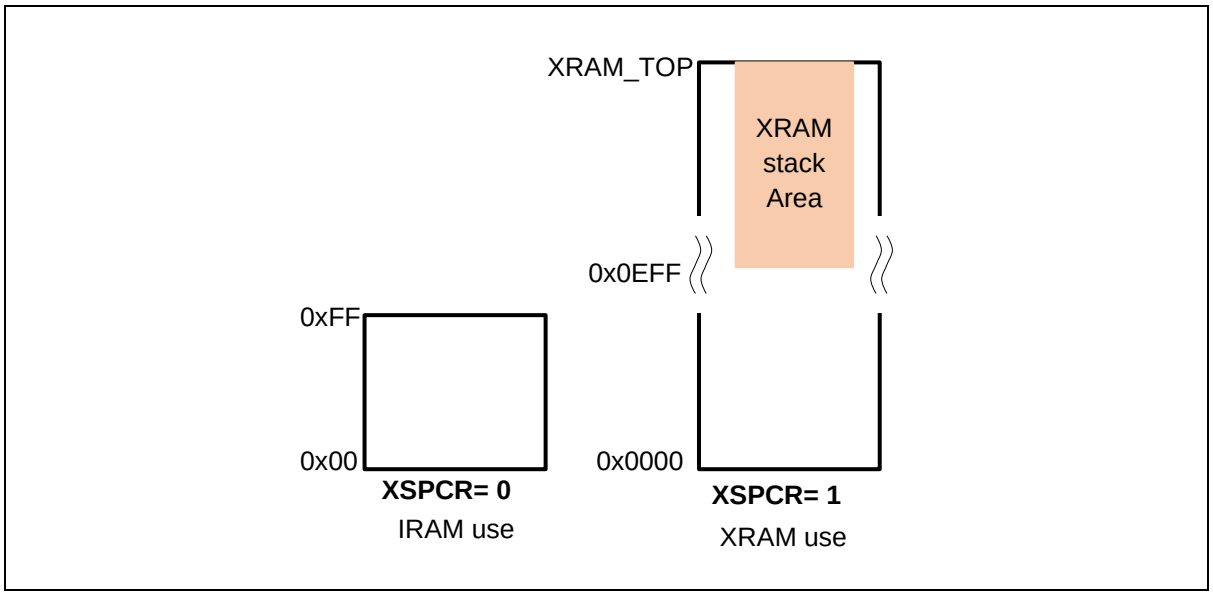


Figure 60. Configuration of the Extended Stack Pointer

STACK_POINTER = {XSP[7:0],SP[7:0]} = XRAM_TOP – STACK_SIZE

Ex) If only 256bytes of XRAM will be used for stack,

- XRAM_TOP = 4K(0x0FFF)
- STACK_SIZE = 256byte(0x0100)
- XSPCR= 1, XSP= 0x0E
- SP=0xFF setting
- Stack Pointer Position = 0x0FFF - 0x0100= 0x0EFF

23.3 OCD (On-chip debugger) emulator and debugger

Microcontroller series that uses an 8051 core has an OCD (On-Chip Debugger), a debug emulation block. The OCD is connected to a target microcontroller using two lines such as DSCL and DSDA. DSCL is for a clock signal and DSDA is for a bi-directional data.

The two lines work for the core management and control by doing register management and execution, step execution, break point and watch functions. In addition, they control and monitor the internal memory and the device by reading and writing.

Table 47. Debug Feature by Series

Series name	96 Series	97 Series	94 Series
OCD function	OCD 1	OCD 2	OCD 2
Max. number of breakpoints	8	8	4
Saving stack in XRAM	No	Yes	Yes
Real time monitoring	No	Yes	Yes
Run flag support	No	Yes	Yes

The OCD 2 applied to 94 Series and 97 Series provides the RTM (Real Time Monitoring) function that enables to monitor internal memory and I/O status without stopping the debugging. In addition, the OCD 2 provides the breakpoint function (RAM Break Function) for the IDATA, SFR, and XDATA.

The following is the functions that have been extended from the OCD 2:

- Emulation Time can be measured in OCD mode (using the Run Flag port)
- CODE, XDATA, IDATA are updated during the Run Time (Real Time Monitoring available).
- IDATA, SFR, XDATA break are added (RAM Break support).

Figure 61 shows the standard 10-pin connector of OCD 1 and OCD 2.

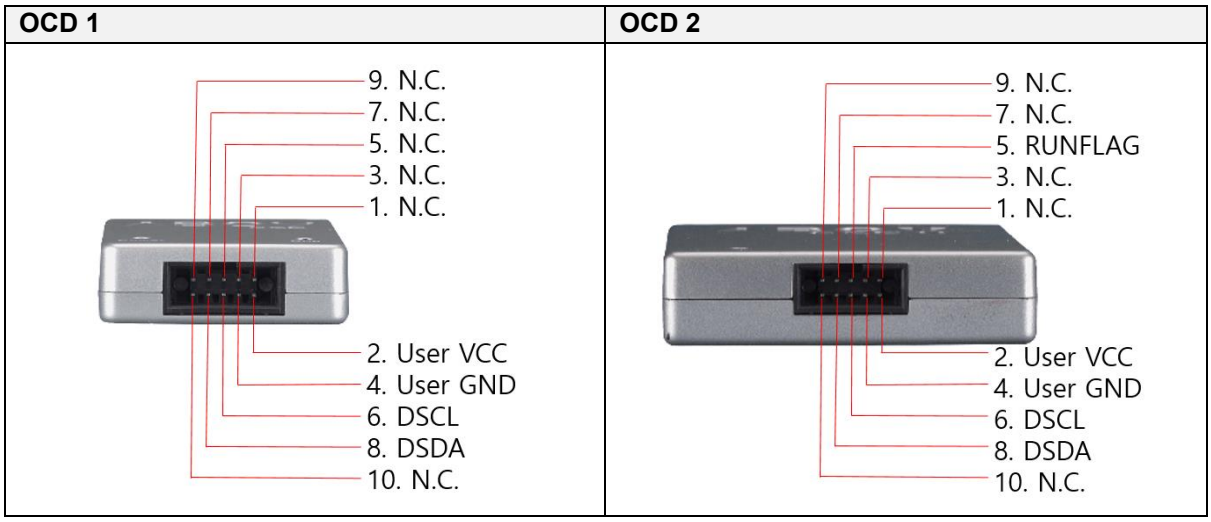


Figure 61. OCD 1 and OCD 2 Connector Pin Diagram

Table 48 introduces pins used for the OCD 1 and OCD 2.

Table 48. OCD 1 and OCD 2 Pin Description

Pin name	Microcontroller function in Debug mode	
	I/O	Description
DSCL	I	Serial clock pin. Input only pin.
DSDA	I/O	Serial data pin. Output port when reading and input port when programming. IT can be assigned as input/push-pull output port.
VDD,VSS	—	Logic power supply pin.

The OCD emulator supports ABOV's 8051 series MCU emulation. The OCD uses two wires interfacing between PC and MCU, which is attached to user's system. The OCD can read or change the value of MCU's internal memory and I/O peripherals. In addition, the OCD controls MCU's internal debugging logic. This means OCD controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD debugger program runs underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista (32-bit). If a user wants to see more details, it is recommended to refer to OCD debugger manual by visiting ABOV's website (http://www.abovsemi.com) and downloading debugger S/W and corresponding manuals.

- Connection:
  - DSCL (A96G150 P13 port)
  - DSDA (A96G150 P11 port)

Figure 62 shows pinouts of OCD connector.

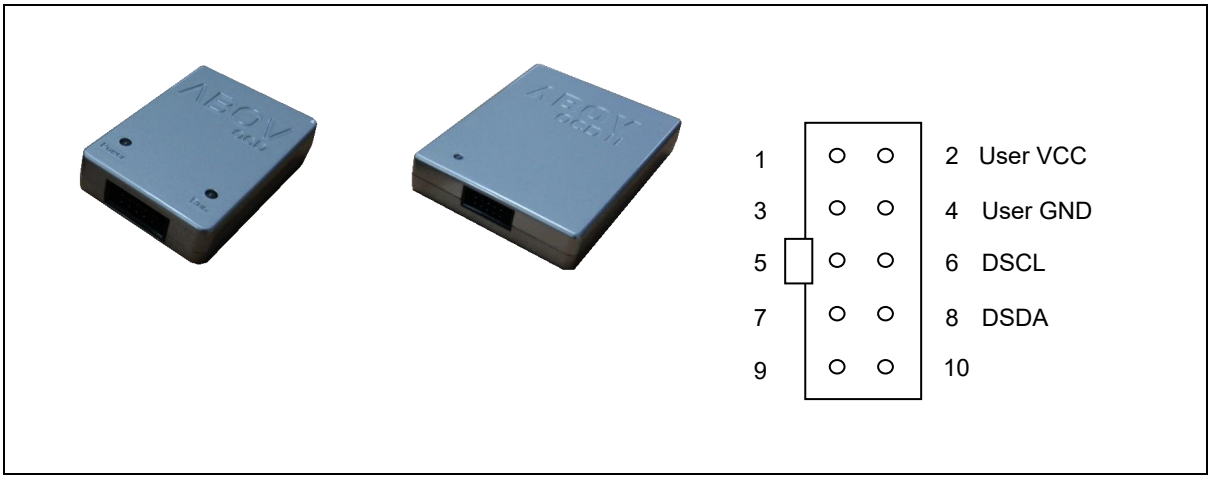


Figure 62. Debugger (OCD1/OCD2) and Pinouts

23.3.1 On-chip debug system

A96G150 supports On-chip debug (OCD) system. We recommend developing and debugging program with A96G1 series. On-chip debug system of A96G150 can be used for programming the non-volatile memories and on-chip debugging. Detail descriptions for programming via the OCD interface can be found in this section.

Table 49 introduces features of OCD.

Table 49. OCD Features

Two wire external interface	• 1 for serial clock input • 1 for bi-directional serial data bus
Debugger accesses	• All internal peripherals • Internal data RAM • Program Counter • Flash memory and data EEPROM memory
Extensive On-Chip Debugging supports for Break Conditions	• Break instruction • Single step break • Program memory break points on single address • Programming of Flash, EEPROM, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by Dr. Choice®
Operating frequency	The maximum frequency of a target MCU.

Figure 63 shows a block diagram of the OCD interface and the On-chip Debug system.

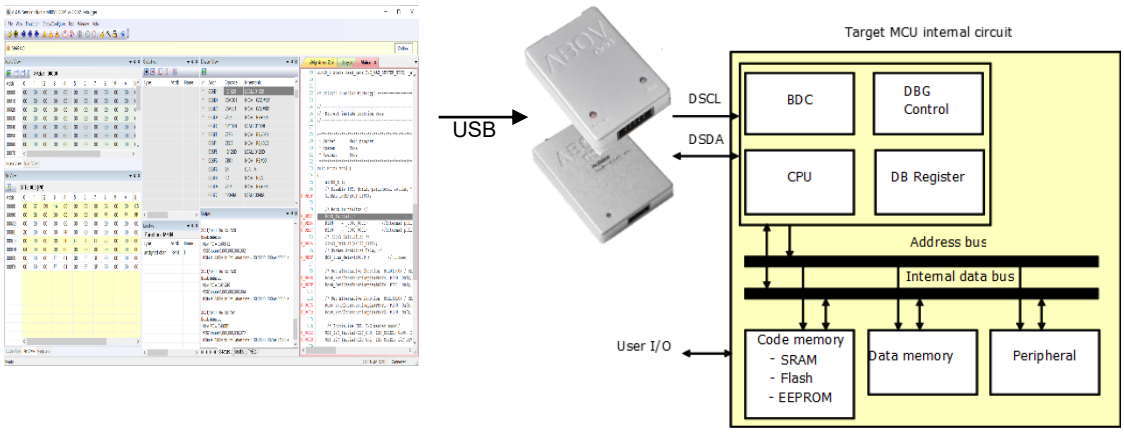


Figure 63. On-chip Debugging System in Block Diagram

23.3.2 Entering debug mode

While communicating through the OCD, users can enter the microcontroller into DEBUG mode by applying power to it. This means, the microcontroller enters DEBUG mode by placing specific signals to DSCL and DSDA at the moment of initialization when powering on the microcontroller. To do this, users should be able to control the power of the microcontroller (VCC or VDD) and need to be careful to place a capacitive load such as a large capacity condenser on a power pin.

Please remember that the microcontroller can enter DEBUG mode only when power is applied, and it cannot enter DEBUG mode once the OCD is run.

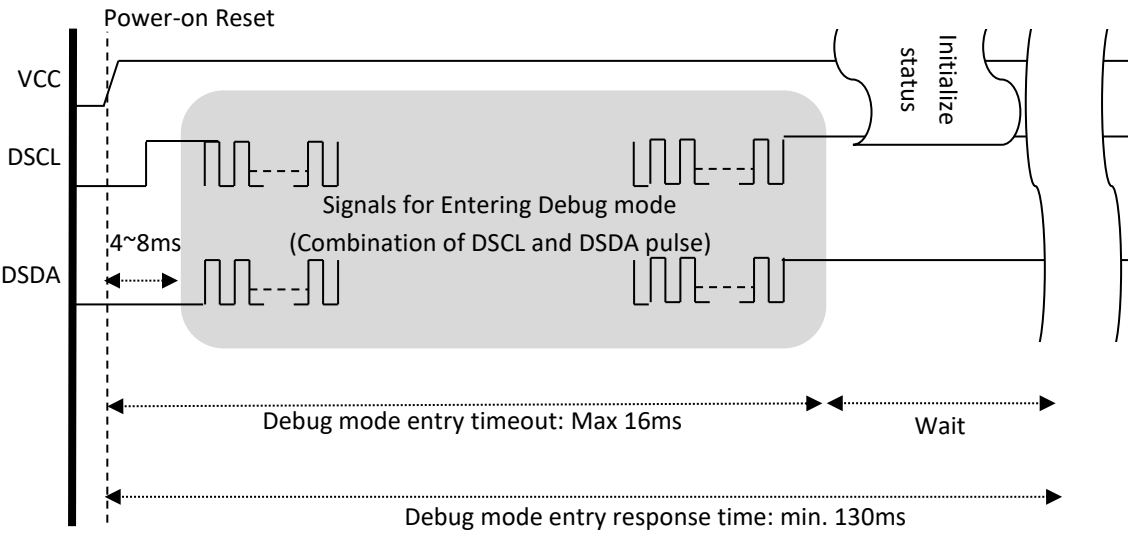


Figure 64. Timing Diagram of Debug Mode Entry

23.3.3 Two-wire communication protocol

For the OCD interface, the semi-duplex communication protocol is used through separate two wires such as DSCL and DSDA. The DSCL is a serial clock signal and the DSDA is a bi-directional serial address and data.

A unit packet of transmission data is 10-bit long and consists of a byte of data, 1-bit of parity, and 1-bit of acknowledge. A parity check bit and a receive acknowledge bit are transmitted to guarantee stability of the data communication. In addition, a communication packet includes a start bit and an end bit to indicate a start and an end of the communication.

More detailed information of this communication protocol is listed below:

Basic transmission packet

- A 10-bit packet transmission using two-pin interface.
- A packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

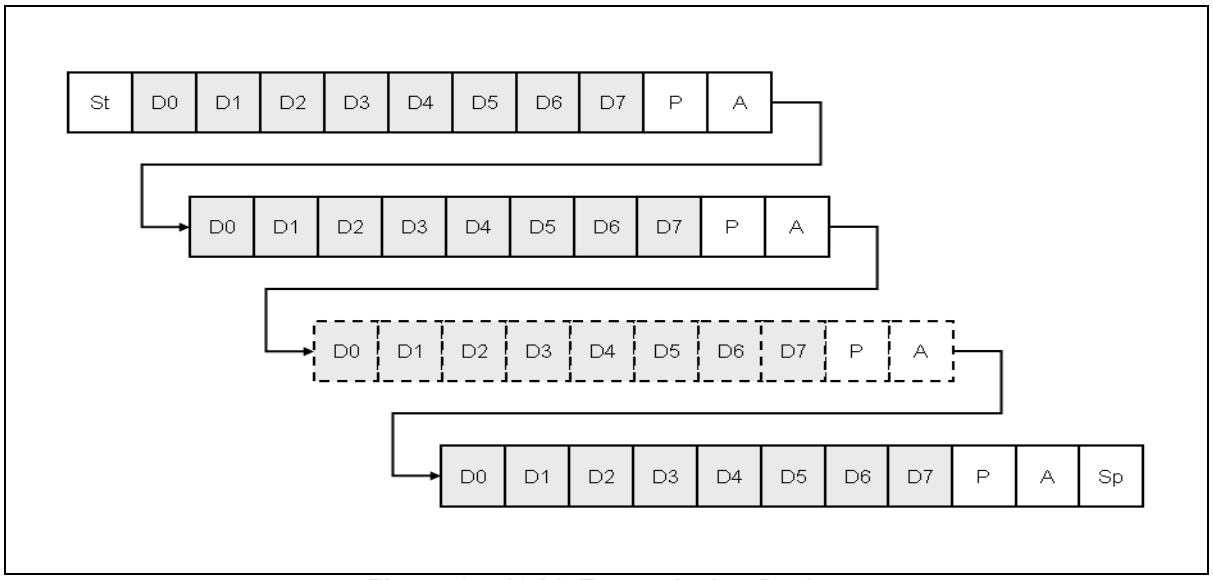


Figure 65. 10-bit Transmission Packet

Packet transmission timing

Figure 66 shows a timing diagram of a packet transmission using the OCD communication protocol. The start bit means a start of a packet and is valid when DSDA falls from ‘H’ to ‘L’ while External Host maintains DSCL to ‘H’. After this, communication data is transferred and received between a Host and a microcontroller. The end bit means an end of the data transmission and is valid when DSDA changes from ‘L’ to ‘H’ while a Debugger maintains DSCL to ‘H’. Next, the microcontroller places the bus in a wait state and processes the received data.

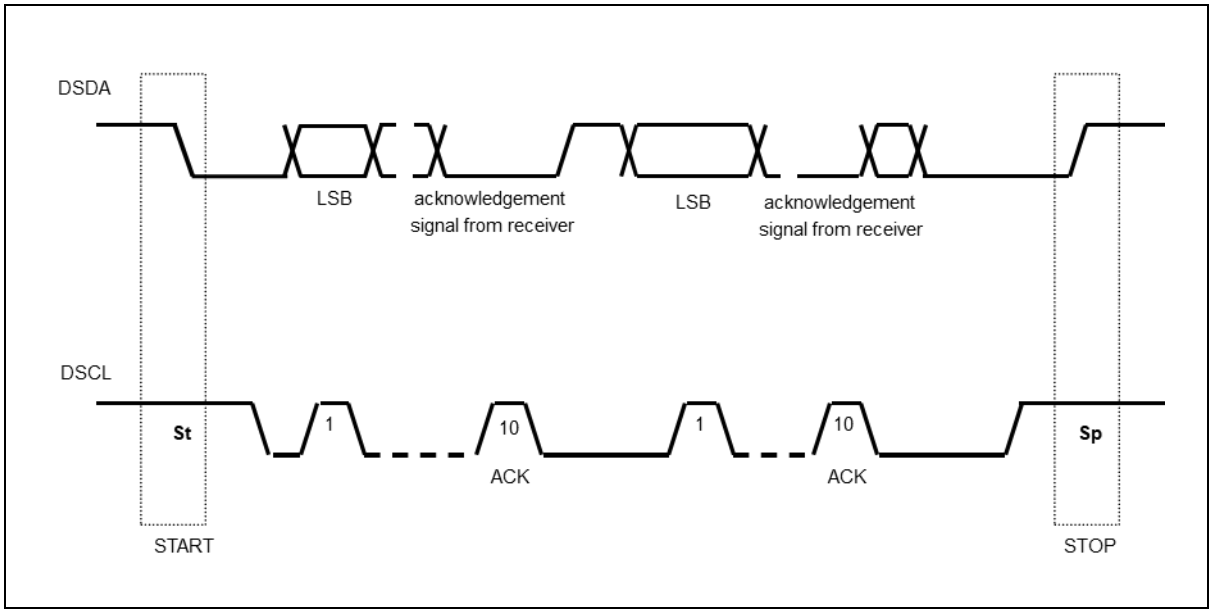


Figure 66. Data Transfer on OCD

Figure 67 shows a timing diagram of each bit based on the state of DSCL clock and DSDA data. Similar to I2C signal, DSDA data is allowed to change when DSCL is ‘L’. If the data changes when DSCL is ‘H’, the change means ‘START’ or ‘STOP’.

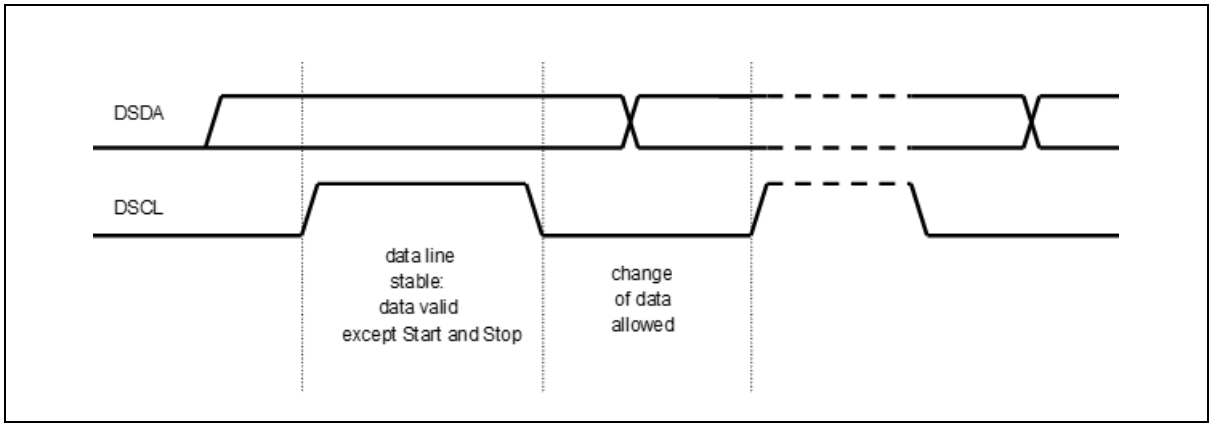


Figure 67. Bit Transfer on Serial Bus

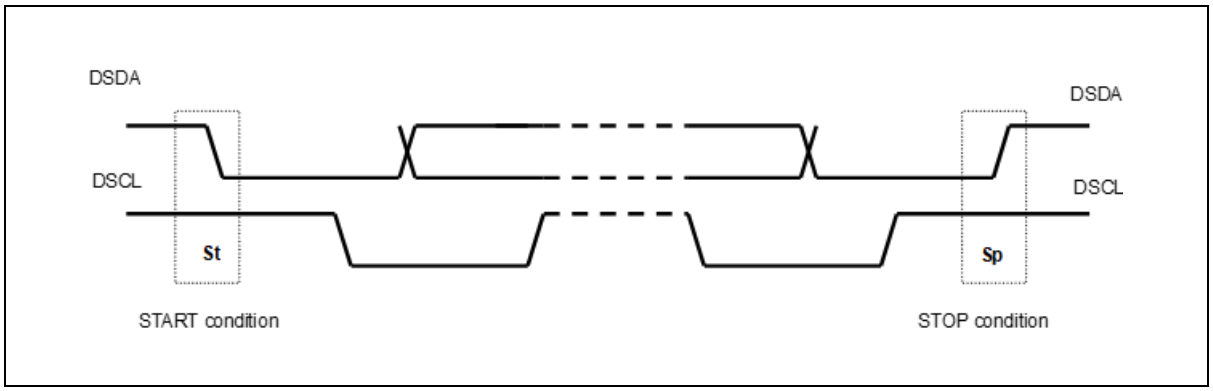


Figure 68. Start and Stop Condition

During the OCD communication, each data byte is transferred in accompany with a parity bit. When data is transferred in succession, a receiver returns the acknowledge bit to inform the reception.

As shown in Figure 69, when transferring data, a receiver outputs DSDA to ‘L’ to inform the normal reception of data. If a receiver outputs DSDA to ‘H’, it means error reception of data.

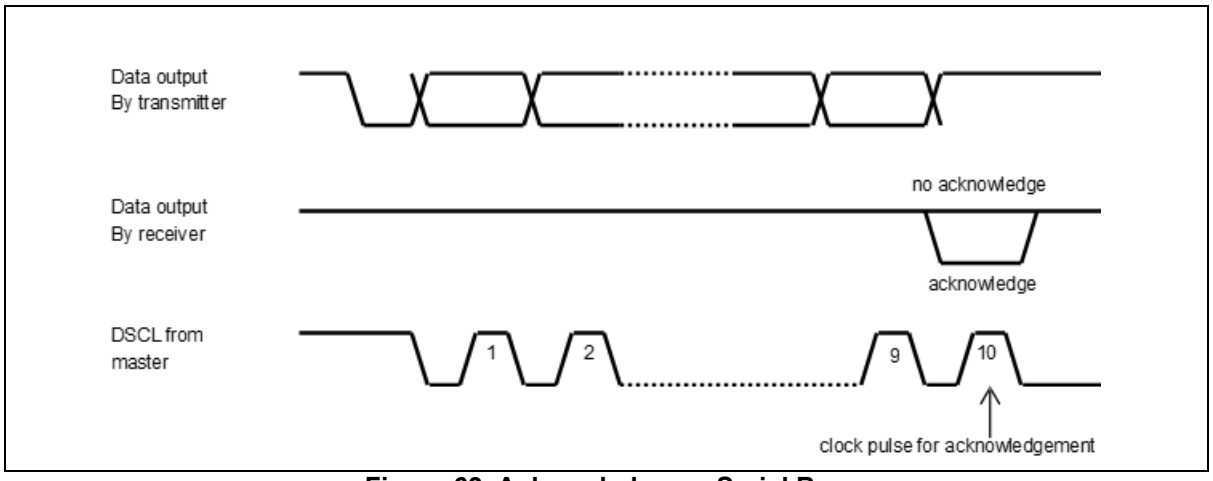


Figure 69. Acknowledge on Serial Bus

While the Host Debugger executes data communications, if a microcontroller needs communication delay or process delay, it can request communication delay to the Host Debugger.

Figure 70 shows timing diagrams where a microcontroller requests communication delay to the Host Debugger. If the microcontroller requests timing delay of the DSCL signal that the Host Debugger outputs, the microcontroller maintains the DSCL signal to ‘L’ to delay the clock change although the Host Debugger changes DSCL to ‘H’.

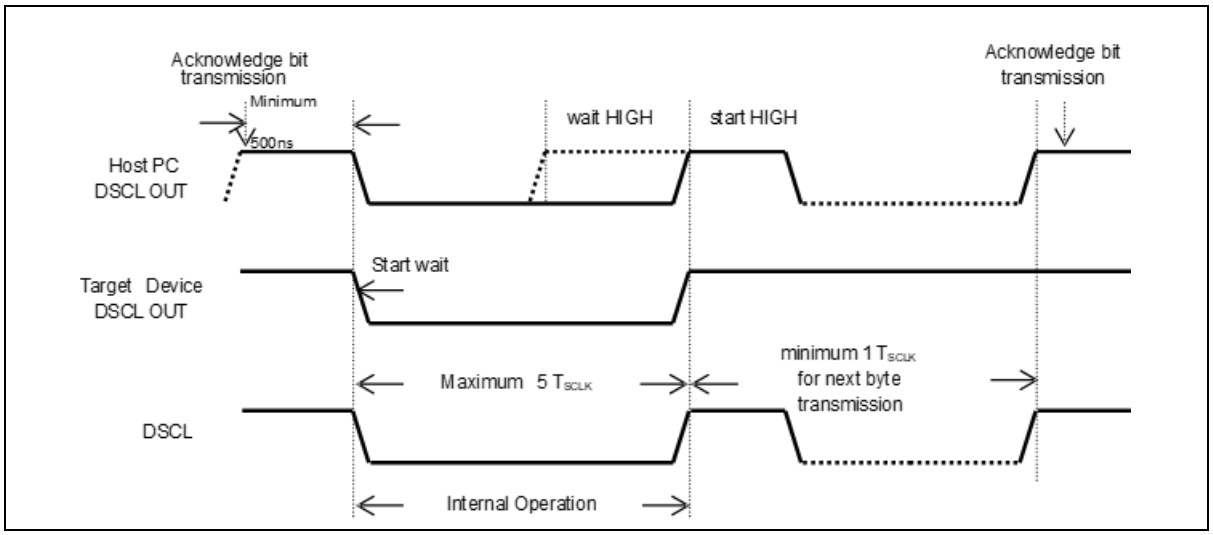


Figure 70. Clock Synchronization during Wait Procedure

23.4 Programmers

23.4.1 E-PGM+

E-PGM+ USB is a single programmer. A user can program A96G150 directly using the E-PGM+.

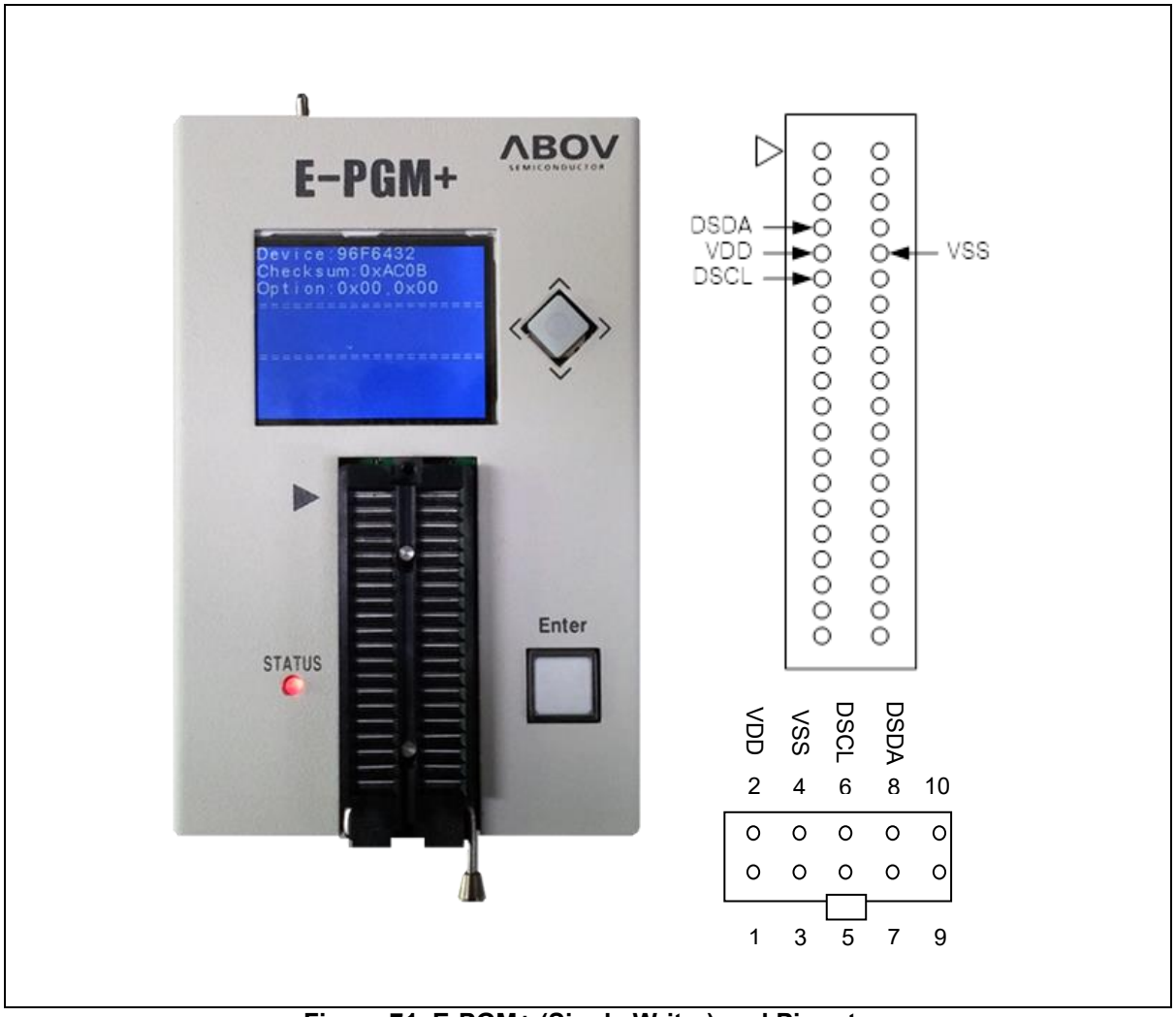


Figure 71. E-PGM+ (Single Writer) and Pinouts

23.4.2 OCD emulator

OCD emulator allows a user to write code on the device too, since OCD debugger supports ISP (In System Programming). It doesn't require additional H/W, except developer's target system.

23.4.3 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

Figure 72. E-Gang4 and E-Gang6 (for Mass Production)

23.5 Flash programming

Program memory of A96G150 is a flash type. This flash ROM is accessed through four pins such as DSCL, DSDA, VDD and VSS in serial data format. For more information about flash memory programming, please refer to Chapter 21. Memory programming

Table 50 introduces each pin and corresponding I/O status.

Table 50. Pins for Flash Programming

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P13	I	Serial clock pin. Input only pin.
DSDA	P11	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	—	Logic power supply pin.

23.5.1 On-board programming

Microcontroller need only four signal lines including VDD and VSS pins for programming flash ROM with serial protocol. Therefore, the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

23.6 Connection of transmission

OCD's two-wire communication interface uses Open-Drain Method (Wire-AND Bi-Directional I/O).

Normally, it is recommended to place a resister greater than 4.7kΩ for DSCL and DSDA respectively. The capacitive load is recommended to be less than 100pF. Outside these ranges, because the communication may not be accomplished, the connection to Debug mode is not guaranteed.

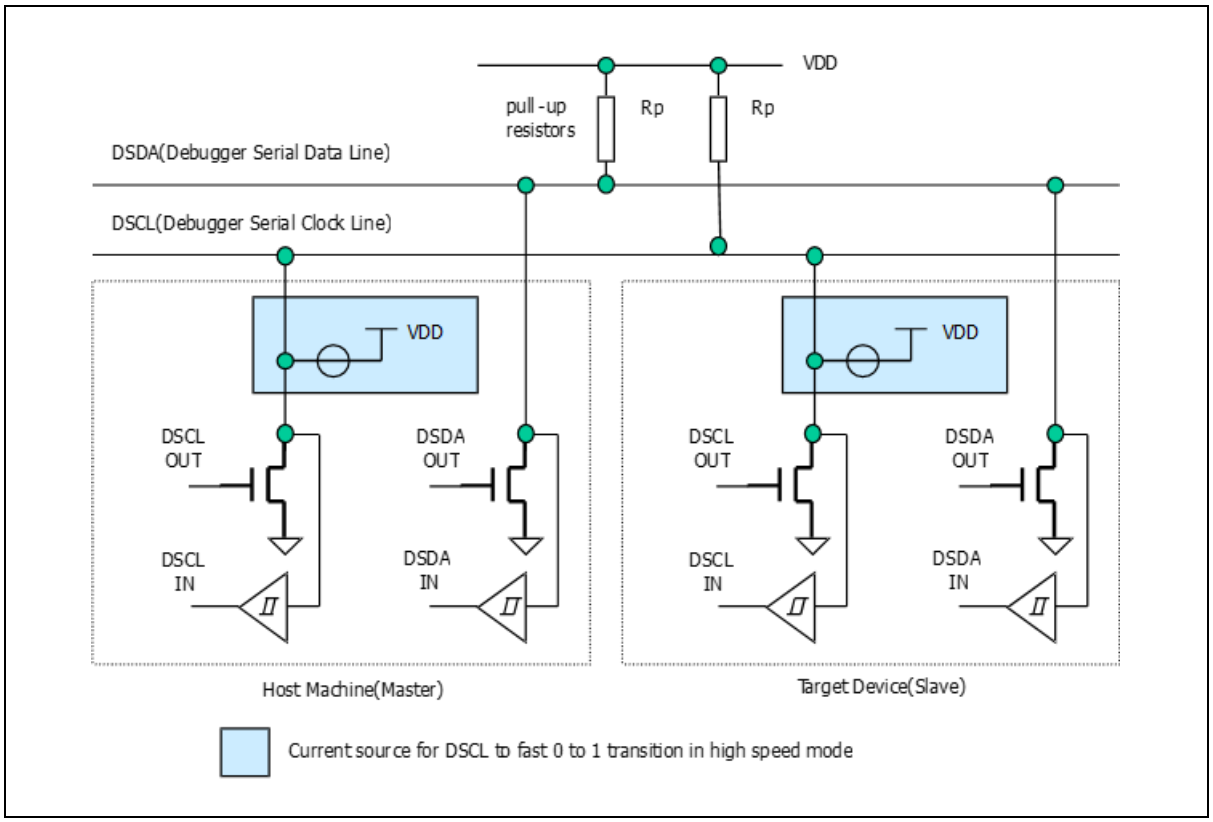


Figure 73. Connection of Transmission

23.7 Circuit design guide

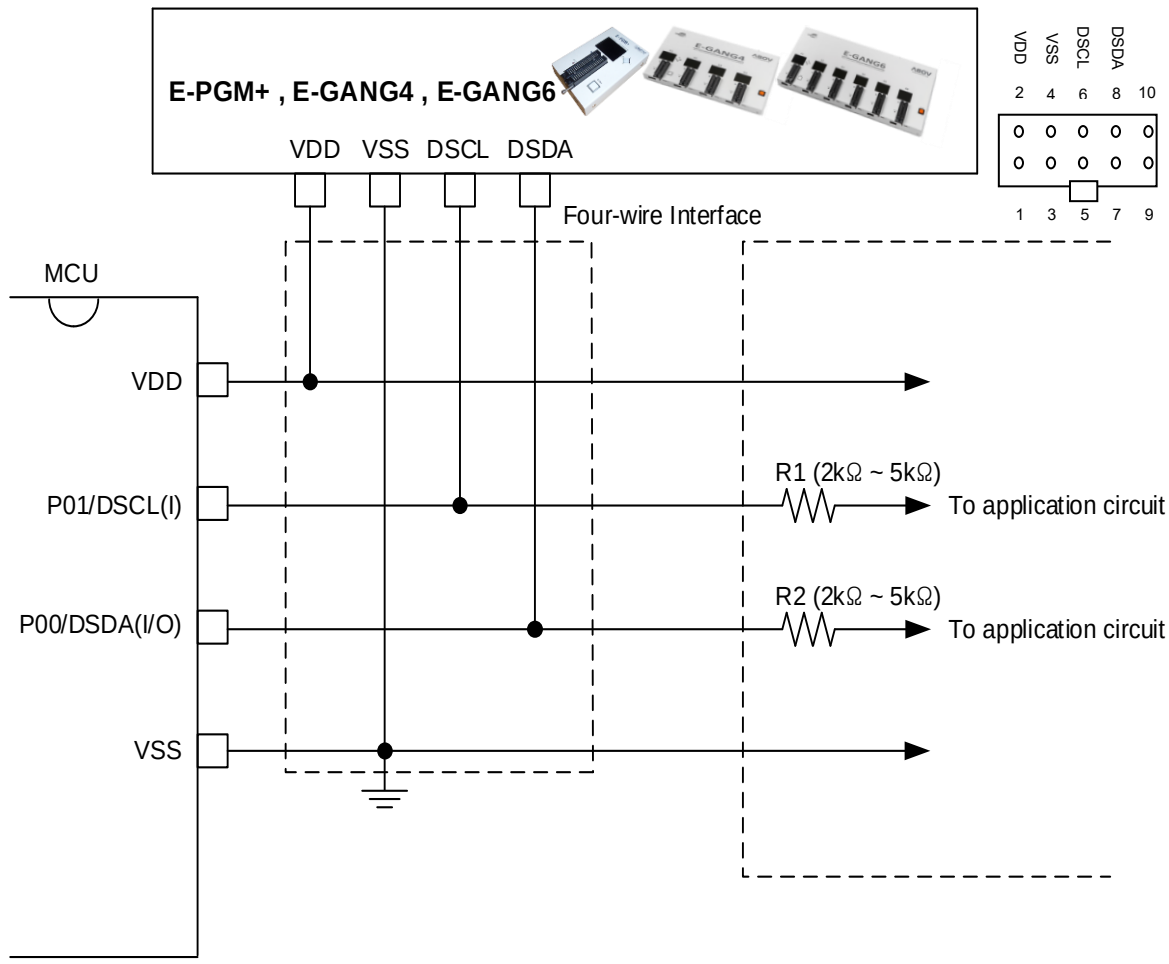
When programming flash memory, the programming tool needs 4 signal lines, DSCL, DSDA, VDD, and VSS. If a user designs a PCB circuit, the user should consider the usage of these 4 signal lines for the on-board programming.

Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.

When you use the OCD pins exclusively or share them with other functions, it needs to be careful.

Figure 74 shows an example circuit where the OCD pins (DSCL and DSDA) are shared with other functions. They are required to be connected when debugging or ISP (In System Program) is executed.

Normally, the OCD pins are connected to outside to execute the predefined functions. Even when they are connected for debugging or ISP directly, the OCD pins are shared with other functions by using resistors as shown in Figure 74. By doing this, the OCD pins process the normal external signals and execute the OCD functions first when they are shared.



NOTES:

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high-speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 74. PCB Design Guide for On-board Programming

24 Package information

This chapter provides A96G150 package information.

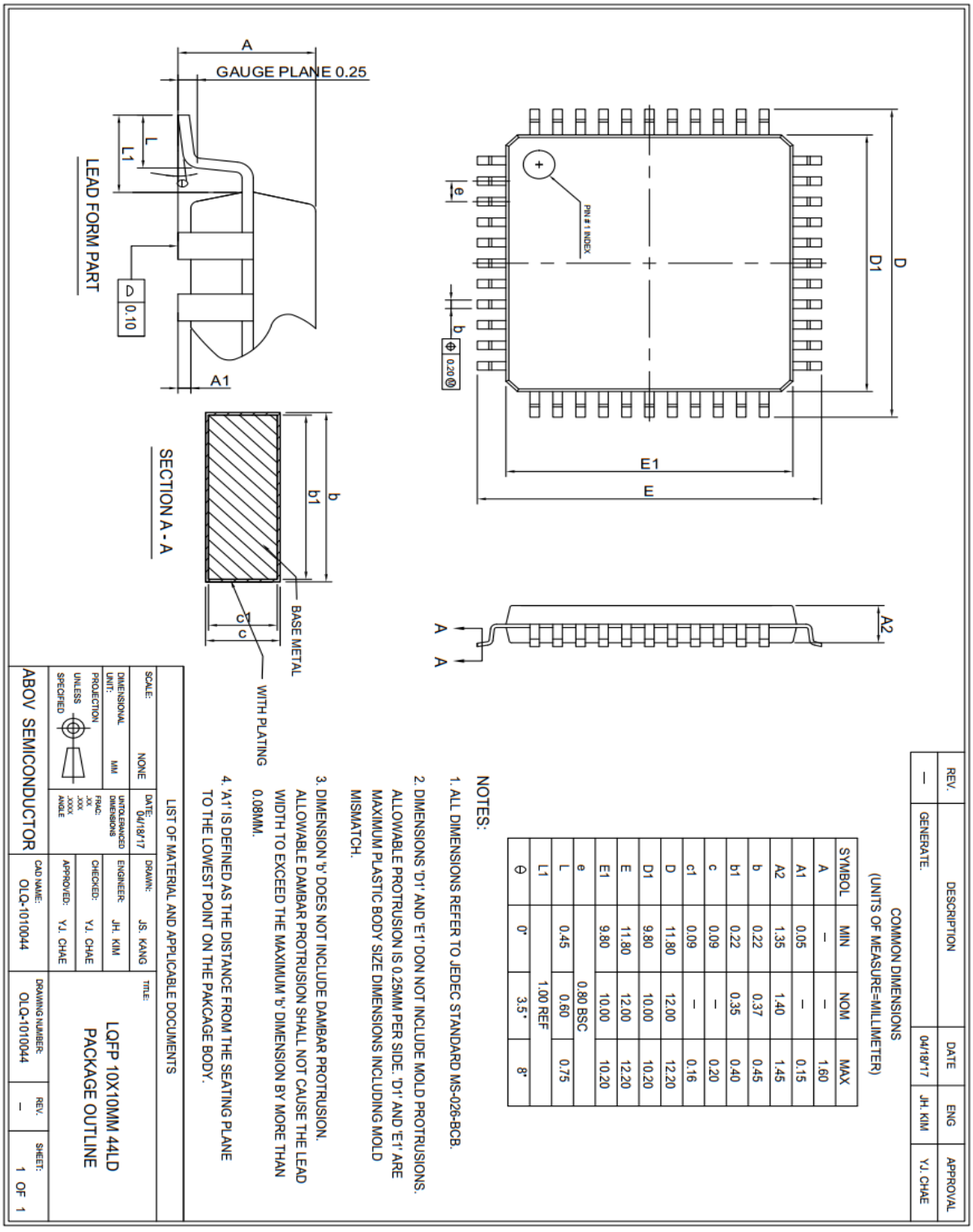


Figure 75. 44 LQFP Package Outline

25 Ordering information

Table 51. A96G150 Device Ordering Information

Device name	FLASH	EEPROM	XRAM	IRAM	ADC	I/O	Package	Temp. range
A96G150SN	64KB	2KB	2304 bytes	256 bytes	15 inputs	42	44 LQFP	-40°C ~ 85°C
A96G150SN2*	64KB	2KB	2304 bytes	256 bytes	15 inputs	42	44 LQFP	-40°C ~ 105°C

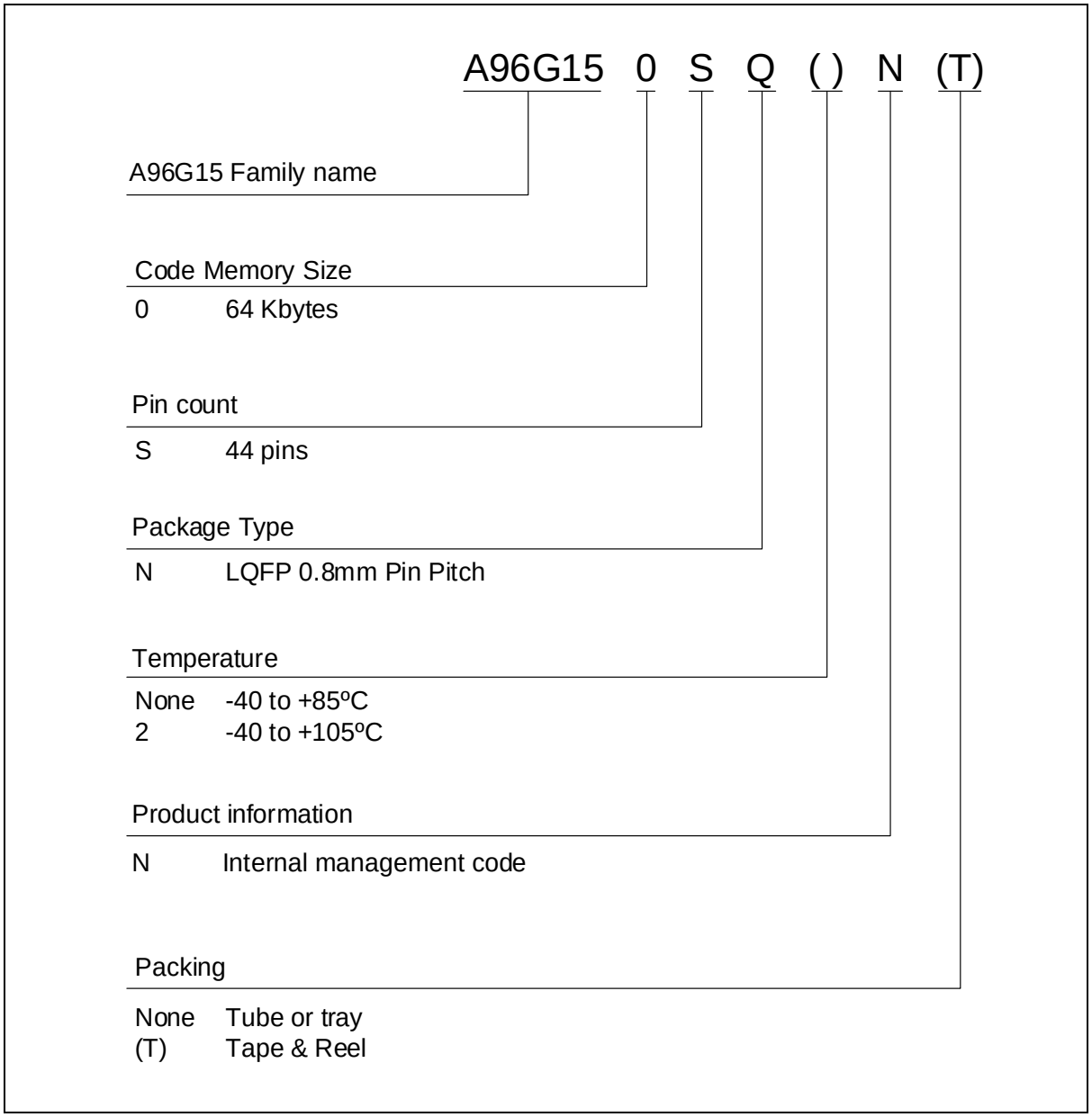


Figure 76. A96G150 Device Numbering Nomenclature

Appendix

Instruction table

Instructions are either1, 2 or 3bytes long as listed in the ‘Bytes’ column below. Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 system clock cycles.

Table 52. Instruction Table

ARITHMETIC				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

Table 52. Instruction Table (continued)

LOGICAL				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

Table 52. Instruction Table (continued)

DATA TRANSFER				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

Table 52. Instruction Table (continued)

BOOLEAN				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

Table 52. Instruction Table (continued)

BRANCHING				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

Table 52. Instruction Table (continued)

MISCELLANEOUS				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00
ADDITIONAL INSTRUCTIONS (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, entries such as E8-EF indicate continuous blocks of hex opcodes used for 8 different registers. Register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as ‘11→F1’ (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

CJNE instructions use abbreviation of #d for immediate data; other instructions use #data as an abbreviation.

Revision history

Revision	Date	Notes
1.00	2022. 06. 22	First creation
1.01	2022. 11. 01	Revision the font of this document

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