A96L523
Datasheet

General Purpose CMOS 8051 Flash 4KB Microcontroller Line interface and LDO 3V Logic

Datasheet Version 1.31

Features

CPU
- 8-bit CISC core (M8051, 2 clocks per cycle)

ROM (FLASH) capacity
- 4 Kbytes Flash with self-read/write capability
- On Chip debug and ISP
- 256bytes IRAM
- 128bytes Data EEPROM

Timer/counter
- Basic Interval Timer, Watch Dog Timer, Siren(by T1), Pulse generation (by T0/T1)

Line interface
- Three Rx Types and Five Tx modes

10-bit A/D converter
- 9 Input channels

Op-Amp
- 2 channels
- Rail-to-rail output

16-Bit CRC/checksum generator
- Auto and User CRC/Checksum mode

Reset
- Reset release level (1.4V)
- Low Voltage Reset

Constant sink current generator
- 2 channels
  - 16-step selectable
  - Max. 274mA sink current

USART (UART + SPI)
- 8bit UART x 1ch
- 8bit SPI x 1ch

Power-down mode
- STOP mode and IDLE mode

Operating Temperature
- -40 ~ +85℃

Package Type
- 24 TSSOP
- Pb-free package

VIN voltage range (Logic)
- Power Supply : 8.5V to 42V
- Signal Input : 0.0V to 42V

Low power consumption (Logic)
- Max. 90uA(@24V, Room Temp)

Low Dropout (Logic)
- 3V ± 3% (@24V, -10 C to +60 C)

LDO Drive ability (Logic)
- 20mA(@VOUT =24v)

Under Voltage Lock Out (Logic)
- Internal UVLO function

Line interface (Logic)
- Comparator for line interface Rx
- TR for line interface TX

Product selection table

Table 1. Device Summary

Part number	Flash	iRAM	USART / SPI	Timer	Line interface	LDO	Constant current	Op-Amp	ADC	I/O	Package
A96L523LRN	4KB	256B	1	2	Tx/Rx	3V	2	2	9ch	14	24TSSOP

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1 Description

A96L523 is an advanced CMOS 8-bit microcontroller with 4Kbytes of FLASH. This is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications.

1.1 Device overview

In this section, features of A96L523 and peripheral counts are introduced.

Table 2. A96L523 Device Features and Peripheral Counts

Peripherals (MCU)		**Description**
Core	CPU	8-bit CISC core (M8051, 2 clocks per cycle)
	Interrupt	Up to 16 peripheral interrupts supported. • EINT0 to 3, EINT10, EINT11(6) • Timer (0/1) (2) • WDT (1) • BIT (1) • USART Rx/Tx (2) • Line interface Rx/Tx(2) • ADC (1) • Siren (1)
Memory	ROM (FLASH) capacity	• 4Kbytes FLASH with self-read and write capability • In-system programming (ISP) • Endurance: 10,000 times(sector 0~123)/ 100,000 times(sector 124~127)
	IRAM	256Bytes
	XRAM	-
Programmable pulse generation		• Pulse generation (by T0/T1) • 8-bit PWM (by T0/T1)
Siren		16-bit × 1-ch (by T1)
Minimum instruction execution time		• 2us (@ 1MHz main clock)
Power down mode		• STOP mode • IDLE mode
General Purpose I/O (GPIO)		• Normal I/O: 14 ports • High sink current port: 2 ports P0[6:7]

Table 2. A96L523 Device Features and Peripheral Counts (continued)

Peripherals (MCU)		**Description**
Reset	Power on reset	Reset release level: 1.2V
	Low voltage reset	• levels detect • 1.60/2.20/2.70V
Low voltage indicator		-
Watch Timer (WT)		-
Timer/counter		• Basic interval timer (BIT) 8-bit x 1-ch. • Watchdog timer (WDT) 8-bit x 1-ch. • 16-bit x 2-ch (T0/T1)
Communication function	USART0	• 8-bit USART x 1-ch or 8-bit SPI x 1-ch
	USI0/1	-
10-bit A/D converter		9 input channels
OpAmp		2 ch.
Oscillator type		-
Internal RC oscillator		• 1MHz ±3.0% (T_A=-40~ +85°C)
Operating voltage and frequency		• 2.0V to 3.6V @ 0.125MHz to 1MHz with crystal
Function (Logic)		**Description**
VIN voltage range		• Power supply 8.5V to 42V • Signal input 0.0V to 42V
Low power consumption		Max. 90uA (@24V, room temperature)
Low Dropout (LDO) voltage		3V ± 3% (@24V, -10℃ to 60℃)
LDO drive ability		20mA (@VOUT = 24V)
Under Voltage Lockout (UVLO)		Internal UVLO function
Line interface		• Comparator for line interface Rx • TR for line interface Tx
ESD performance		• 2000V human body model • 200V machine model
RF-EMS(IEC 61000-4-3)		• LV3(10V/m)
Common		**Description**
Operating temperature		-40℃ to 85℃ ambient temperature
Package type		24 TSSOP

1.2 A96L523 block diagram

In this section, A96L523 device with peripherals are described in a block diagram.

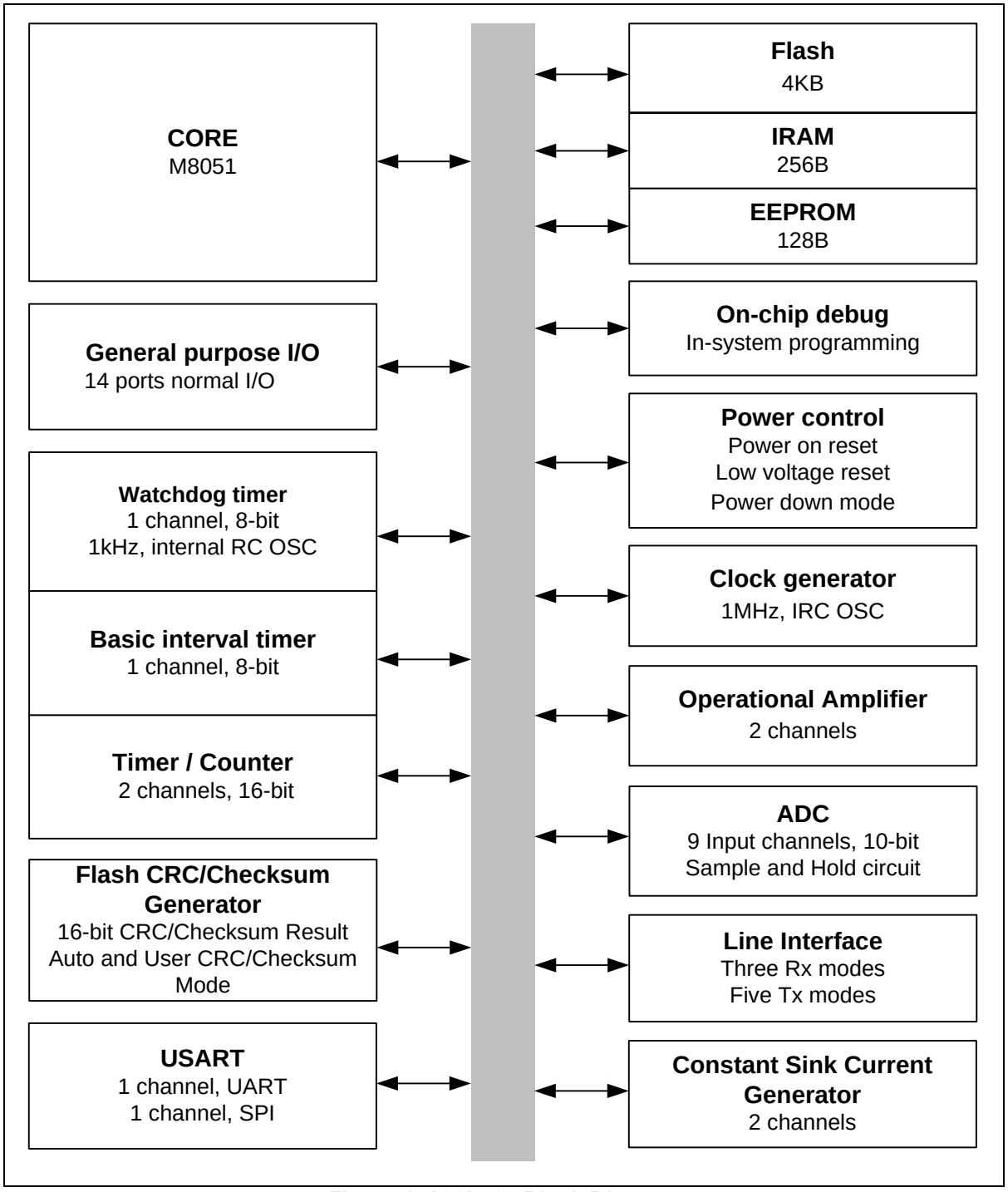


Figure 1. A96L523 Block Diagram

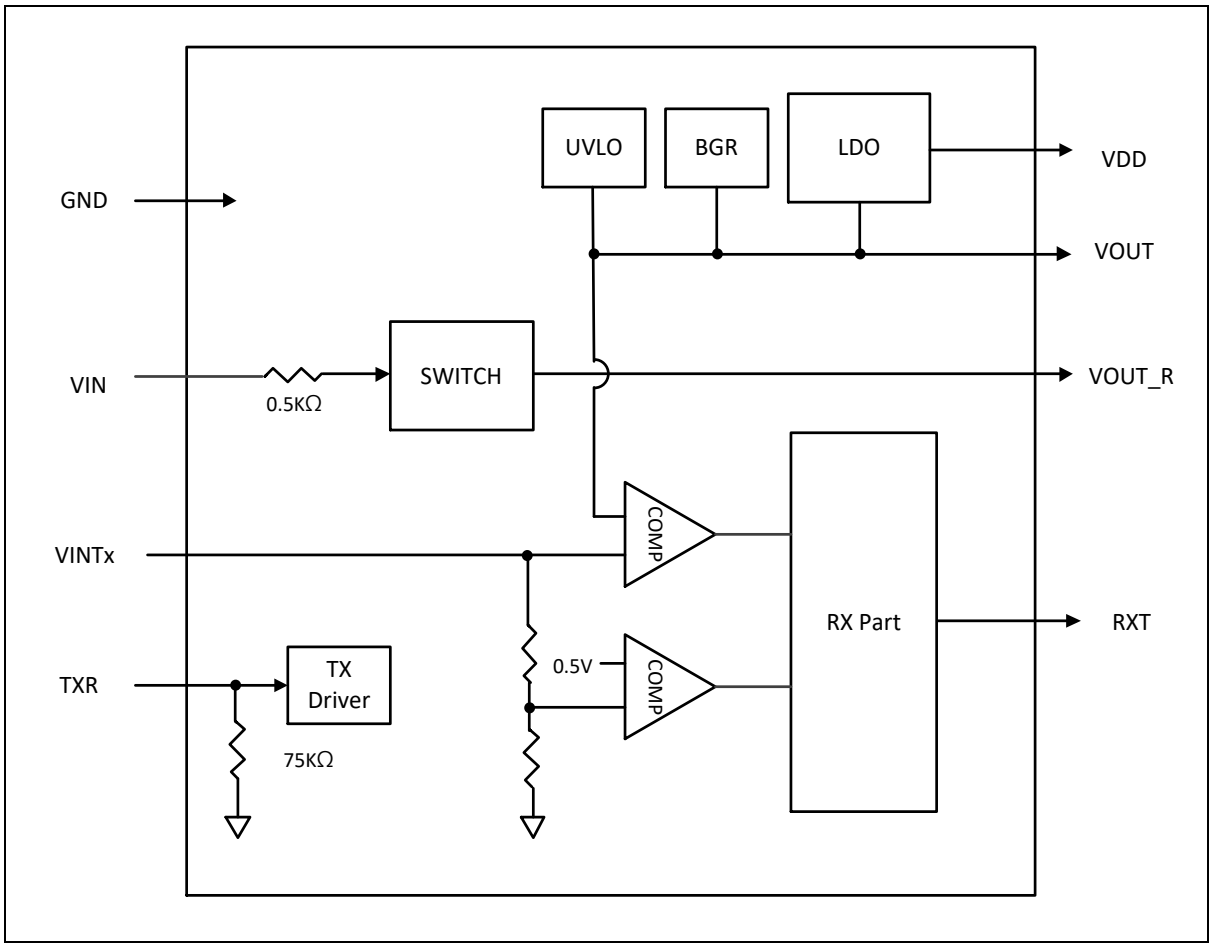


Figure 2. A96L523 Block diagram (logic part)

1.3 Functional description

The following section provides an overview of the features of the A96L523 series microcontroller.

1.3.1 CMOS 8051 core

A96L523 is an advanced CMOS 8-bit microcontroller with 4Kbytes of FLASH. This is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. Since A96L523 has Mentor 8051 as its core, and ROM is smaller than 4Kbytes in size, a developer can use any standard 8051 compiler of other providers.

1.3.2 4KB internal code flash memory

A 16-bit program counter is capable of addressing up to 64Kbytes, but this device has just 4Kbytes program memory space.

1.3.3 256 internal SRAM

The internal data memory space is divided into three blocks, which are generally referred to as the lower 128 bytes, upper 128 bytes, and SFR space.

1.3.4 EEPROM

The write/erase cycles of the internal EEPROM can be increased significantly if it is divided into smaller and used in turn. If 128bytes are divided into 4 areas with 32bytes and the each area from 1st to 4th is used up to 100,000 cycles, the total erase/write is for 400,000 cycles

1.3.5 I/O ports

The A96L523 has two groups of I/O ports (P0~P1). Each can be easily configured by software as I/O pin, internal pull up and open-drain pin to meet various system configurations and design requirements. Also P0/P1 include function that can generate interrupt according to change of state of the pin.

1.3.6 Interrupt controller

The A96L523 supports up to 16 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. They can also have four levels of priority assigned to them. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt source, and is not controllable by software

1.3.7 Clock generator

The default system clock is 1MHz INT-RC Oscillator and the default division rate is one. In order to stabilize system internally, it is used 1MHz INT-RC oscillator on POR.

1.3.8 Basic interval timer

The A96L523 has one 8-bit basic interval timer that is free-run and can't stop. Block diagram is shown in Figure 1. In addition, the basic interval timer generates the time base for watchdog timer counting. It also provides a basic interval timer interrupt (BITIFR).

1.3.9 Watchdog timer

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or something like that, and resumes the CPU to the normal state

1.3.10 Multi-purpose 16-bit timer

Four-channel 16-bit timers and one-channel low power general-purposed 16-bit timers support the functions introduced below:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

1.3.11 Line interface

The line Interface has two operating modes:

- Receive mode (RX Types 0~2)
- Transmit mode (TX Mode 0~4)

1.3.12 10-bit Analog-to-Digital Converter (ADC)

The analog-to-digital converter (A/D) allows conversion of an analog input signal to corresponding 10-bit digital value.

1.3.13 Operational amplifier

There is operational amplifier (OP-AMP) two channel in A96L523. The operational amplifier (OP-AMP) has three registers which are OP-AMP control register 0(AMPCR0) and OP-AMP control register 1(AMPCR1) and Chopper control register (CHPCR).

1.3.14 USART (UART and SPI)

USART supports UART and SPI mode. Only one of them can be used.

1.3.15 Constant sink current generator

Constant Sink Current Generator could provide constant current while I_{CS} voltage ranges from 1.8V to 3.6V. The constant current value is controlled by configuring ICSDR0/ICSDR1 registers, and the sink current will be between 50mA and 290mA.

1.3.16 Flash CRC/checksum generator

The Flash CRC (cyclic redundancy check) generator is used to get a 16-bit CRC code from Flash ROM and a generator polynomial.

1.3.17 Power down operation

The A96L523 has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides two kinds of power saving functions, IDLE and STOP mode. In two modes, program is stopped.

1.3.18 Reset

The A96L523 has five types of reset sources as shown in the followings:

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset (In the case of LVREN = `0 `)
- OCD Reset

1.4 Logic functional description

1.4.1 Initial function

The VDD voltage is increasing by the external power VIN voltage increasing. If the VDD voltage is 2.4V then the UVLO signal go to high. By this signal, the internal reset is release.

1.4.2 Power charging

The A96L523 includes the inrush current limit by PMOS transistor. If the VIN voltage level is higher than the VOUT voltage level, the switch turns on via the comparator. At this time, capacitor C0 of VOUT becomes charged state, and if VOUT voltage is higher than or equal to VIN, the switch turns off.

1.4.3 RXT, TXR function

In case of line interface communication, data can be transferred by changing the VIN voltage. In the previous method, external comparator and resistor components were required. The A96L523 supports this function inside the IC

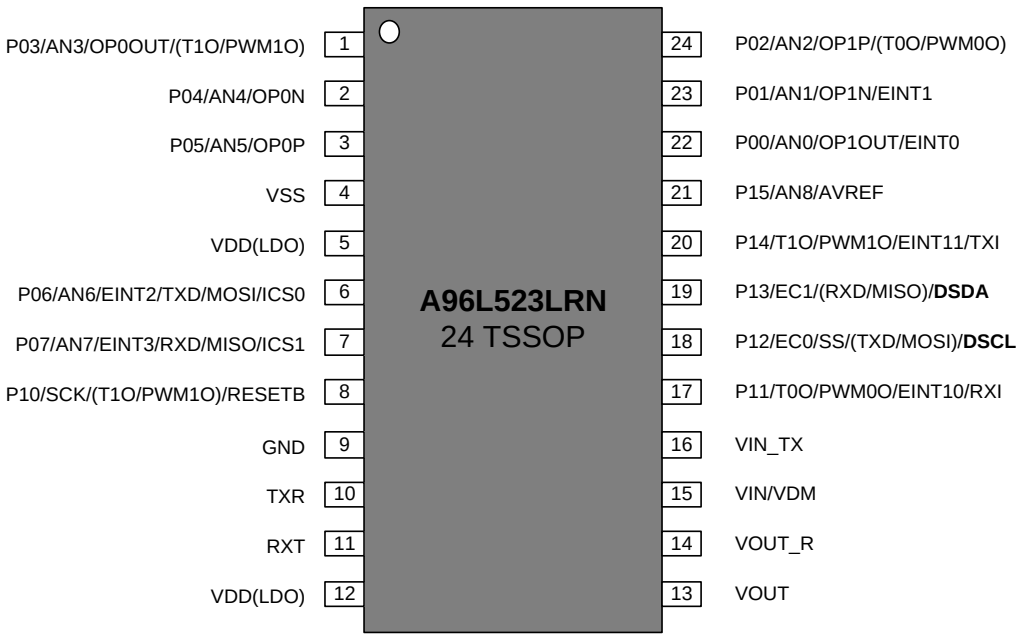
1.4.4 LDO description

The A96L523 includes one LDO (Low Drop Output voltage) for microcontroller and indicated LED driver power. In the initial operation phase, when the power/signal line is connecting to VIN pin, the C0 capacitor on pin VOUT is charged. The BGR circuit generates the VREF voltage. The LDO circuit can generate the LDO voltage by VREF voltage.

2 Pinouts and pin description

In this chapter, A96L523 device pinouts and pin descriptions are introduced.

2.1 Pinouts



NOTE: Programmer (E-PGM+, E-Gang4/6) uses P1[2:3] pin as DSCL, DSDA.

Figure 3. A96L523 24TSSOP Pin Assignment

2.2 Pin description

Table 3. Normal Pin Description

PIN name	I/O	Function	@RESET	Shared with
P00	I/O	The port 0 is a bit-programmable I/O port which can be configured as an input (P00/P01/P06/P07: Schmitt trigger input), a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	AN0/OP1OUT/EINT0
P01				AN1/OP1N/EINT1
P02				AN2/OP1P/(T0O/PWM0O)
P03				AN3/OP0OUT/(T1O/PWM1O)
P04				AN4/OP0N
P05				AN5/OP0P
P06				AN6/EINT2/TXD/MOSI/ICS0
P07				AN7/EINT3/RXD/MISO/ICS1
P10	I/O	The port 1 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SCK/(T1O/PWM1O)/RESETB
P11				T0O/PWM0O/EINT10/RXI
P12				EC0/SS/(TXD/MOSI)/DSCL
P13				EC1/(RXD/MISO)/DSDA
P14				T1O/PWM1O/EINT11/TXI
P15				AN8/AVREF
EINT0	I/O	External interrupt inputs	Input	P00/AN0/OP1OUT
EINT1				P01/AN1/OP1N
EINT2				P06/AN6/TXD/MOSI/ICS0
EINT3				P07/AN7/RXD/MISO/ICS1
EINT10	I/O	External interrupt input and Timer 0 capture input	Input	P11/T0O/PWM0O/RXI
EINT11	I/O	External interrupt input and Timer 1 capture input	Input	P14/T1O/PWM1O/TXI
T0O	I/O	Timer 0 interval output	Input	P11/PWM0O/EINT10/RXI (P02/AN2/OP1P/PWM0O)
T1O	I/O	Timer 1 interval output	Input	P14/PWM1O/EINT11/TXI (P03/AN3/OP0OUT/PWM1O) (P10/SCK/PWM1O/RESETB)
PWM0O	I/O	Timer 0 pulse output	Input	P11/T0O/EINT10/RXI(P02/AN2/ OP1P/T0O)
PWM1O	I/O	Timer 1 pulse output	Input	P14/T1O/EINT11/TXI (P03/AN3/OP0OUT/T1O) (P10/SCK/T1O/RESETB)

Table 3. Normal Pin Description (continued)

PIN name	I/O	Function	@RESET	Shared with
EC0	I/O	Timer 0 event count input	Input	P12/SS/DSCL
EC1	I/O	Timer 1 event count input	Input	P13/DSDA
RXI	I/O	Line interface receive input	Input	P11/T0O/PWM0O/EINT10
TXI	I/O	Line interface transmit output	Input	P14/T1O/PWM1O/EINT11
AN0	I/O	A/D converter analog input channels	Input	P00/OP1OUT/EINT0
AN1				P01/OP1N/EINT1
AN2				P02/OP1P/(T0O/PWM0O)
AN3				P03/OP0OUT/(T1O/PWM1O)
AN4				P04/OP0N
AN5				P05/OP0P
AN6				P06/EINT2/TXD/MOSI/ICS0
AN7				P07/EINT3/RXD/MISO/ICS1
AN8				P15/AVREF
AVREF	I/O	A/D converter reference voltage	Input	AN8/P15
OP0P	I/O	OP-AMP 0 positive input	Input	P05/AN5
OP0N	I/O	OP-AMP 0 negative input	Input	P04/AN4
OP0OUT	I/O	OP-AMP 0 output	Input	P03/AN3/(T1O/PWM1O)
OP1P	I/O	OP-AMP 1 positive input	Input	P02/AN2/(T0O/PWM0O)
OP1N	I/O	OP-AMP 1 negative input	Input	P01/AN1/EINT1
OP1OUT	I/O	OP-AMP 1 output	Input	P00/AN0/EINT0
TXD	I/O	UART data output	Input	P06/EINT2/AN6/MOSI/ICS0 (P12/EC0/SS/MOSI/DSCL)
RXD	I/O	UART data input	Input	P07/EINT3/AN7/MISO/ICS1 (P13/EC1/MISO/DSDA)
MOSI	I/O	SPI master output, slave input	Input	P06/EINT2/AN6/TXD/ICS0 (P12/EC0/SS/TXD/DSCL)
MISO	I/O	SPI master input, slave output	Input	P07/EINT3/AN7/RXD/ICS1 (P13/EC1/RXD/DSDA)
SCK	I/O	SPI clock input/output	Input	P10/(T1O/PWM1O)/RESETB
SS	I/O	SPI slave select input	Input	P12/EC0/DSCL
ICS0	I/O	Constant sink current pins	Input	P06/AN6/EINT2/TXD/MOSI
ICS1				P07/AN7/EINT3/RXD/MISO
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P10/SCK/(T1O/PWM1O)
DSCL	I/O	On chip debugger clock input	Input	EC0/P12/SS
DSDA	I/O	On chip debugger data input/output	Input	EC1/P13
VSS	–	Power input pin	–	–
VDD(LDO)	–	Power output pin (From Logic). LDO Power input pin(To MCU)	–	–

Table 3. Normal Pin Description (continued)

PIN name	I/O	Function	@RESET	Shared with
VOUT	O	Internal Power Pin. Connect to Capacitor	Output	–
VOUT_R	O	Switch Output Pin	Output	–
VIN	I	External Power Pin & Bridge Output Pin	Input	–
VINTx	O	Transmission Pin	Output	–
TXR	I	Input Pin for Power Signal Transmission	Input	–
RXT	O	Received Signal Output Pin	Output	–

NOTES:

1. The P10/RESETB pin is configured as one of the P10/SCK and the RESETB pin by the
2. “CONFIGURE OPTION”.
3. If the P13/DSDA and P12/DSCL pins are connected to an emulator during reset or power-on reset, the pins are automatically configured as the debugger pins.
4. The P13/DSDA and P12/DSCL pins are configured as inputs with an internal pull-up resistor only during the reset or power-on reset.
5. For VDD (LD) pin, Logic uses 3v output and MCU uses corresponding power as input

.

3 Port structures

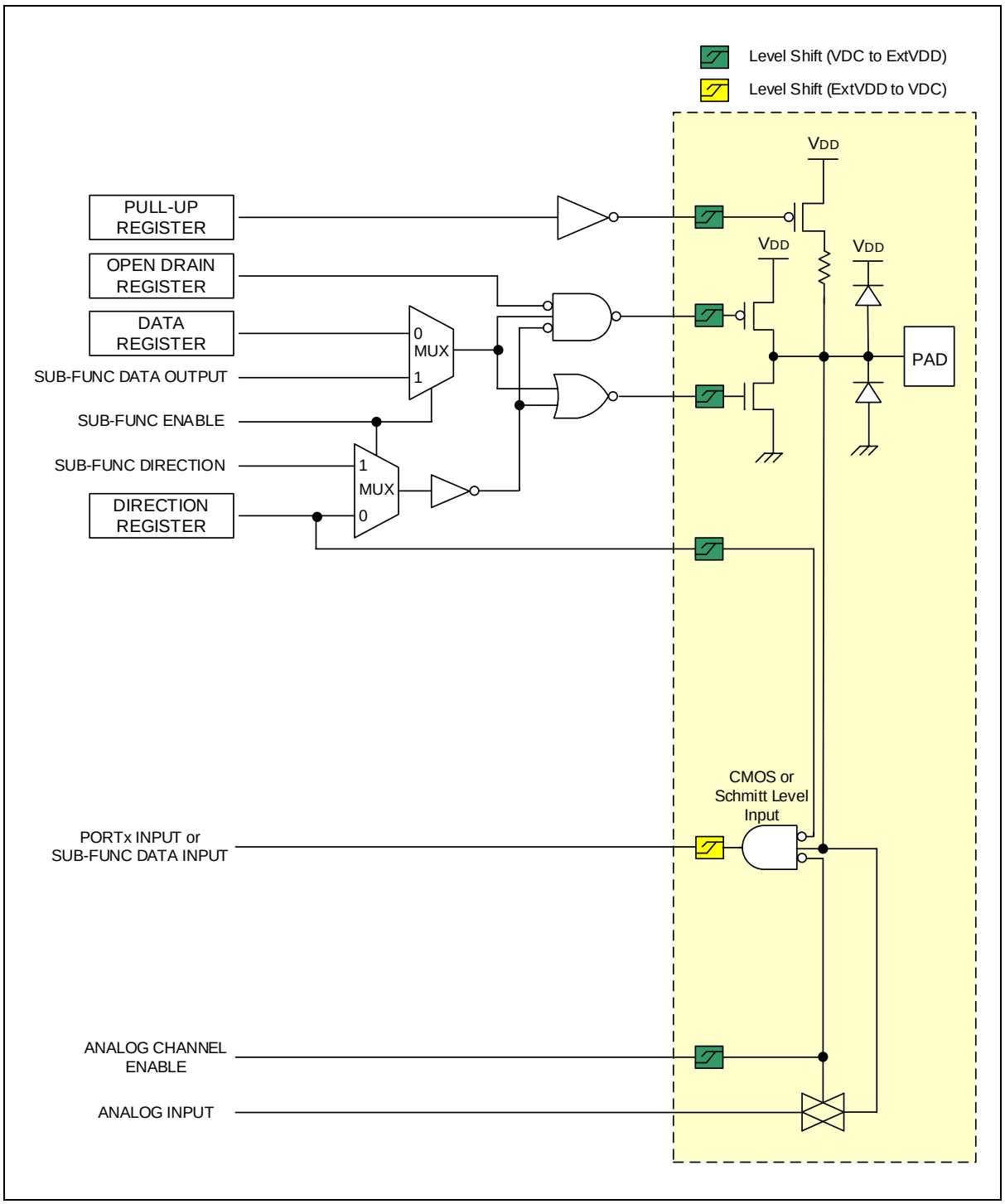


Figure 4. General Purpose I/O Port

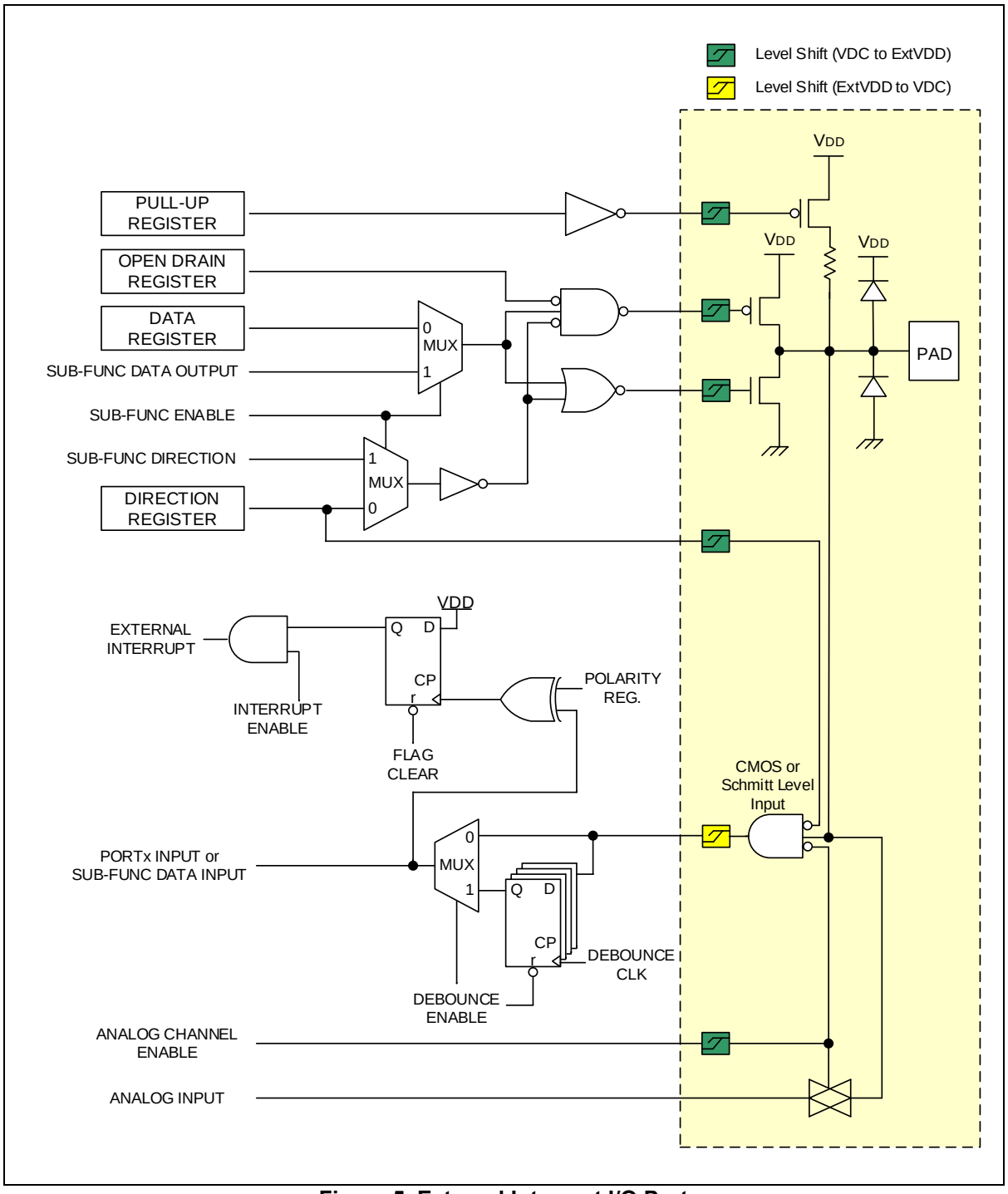


Figure 5. External Interrupt I/O Port

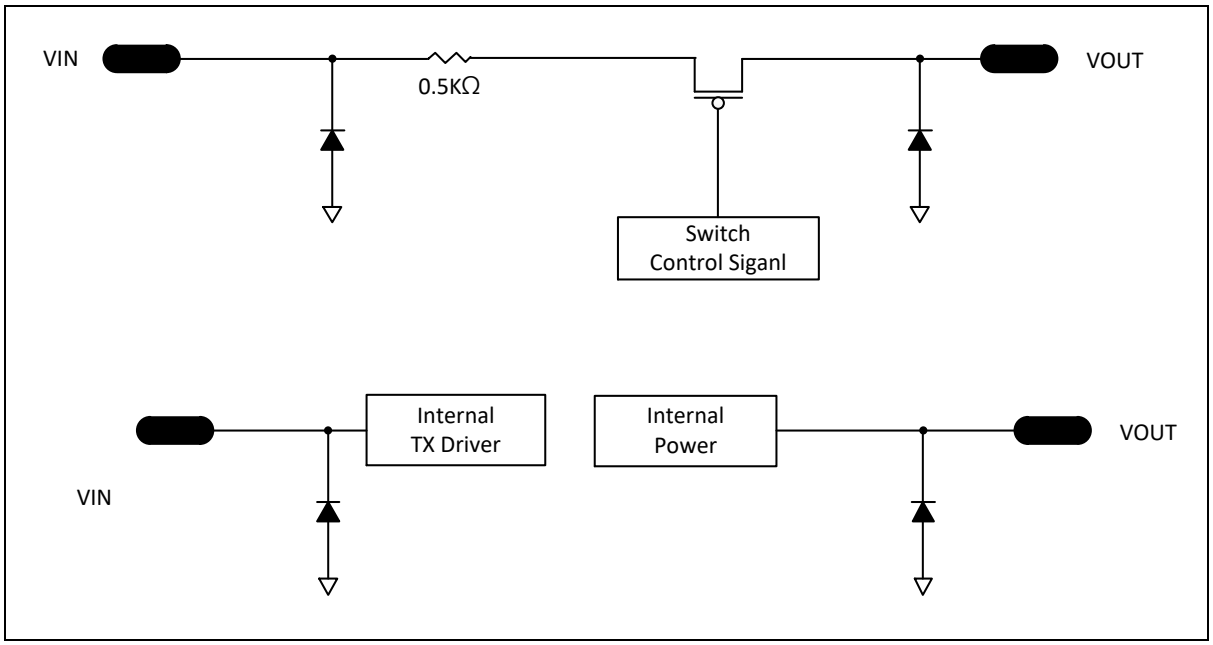


Figure 6. VOUT, VOUT_R and VIN Port

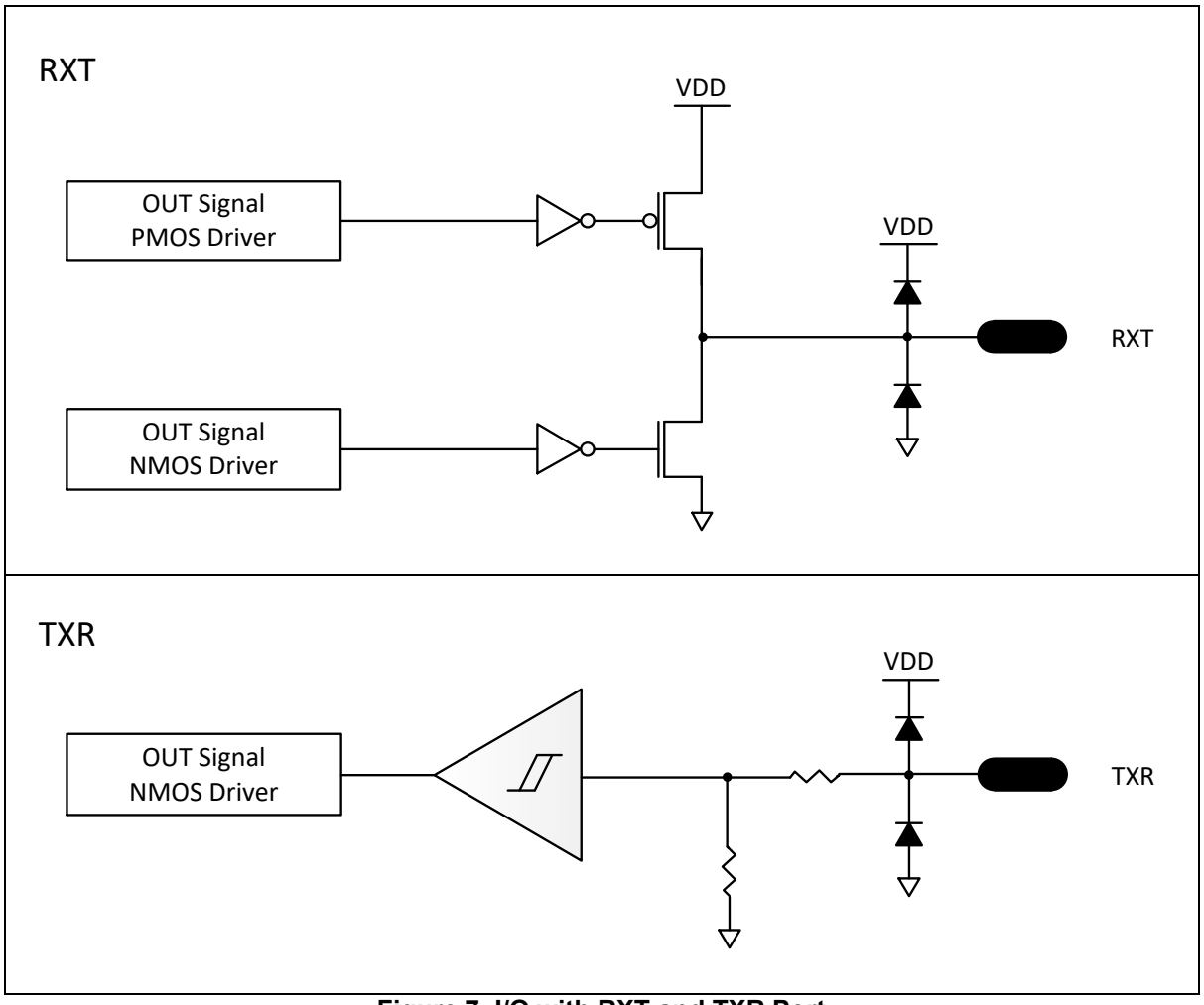


Figure 7. I/O with RXT and TXR Port

4 Memory organization

A96L523 addresses two separate address memory spaces:

- Program memory
- Data memory

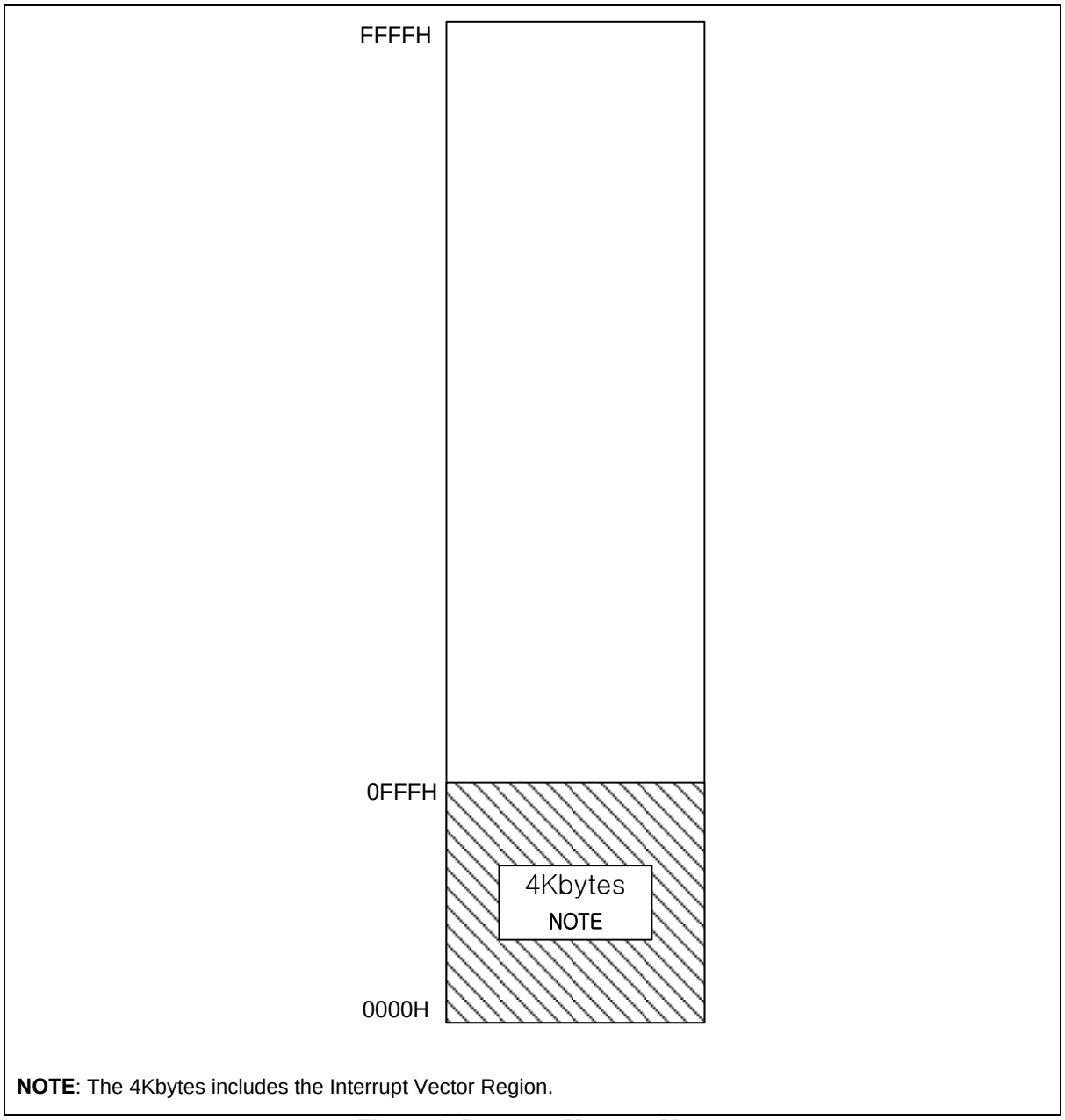
The A96L523 addresses two separate address memory stores: Program memory and Data memory. The logical separation of Program and Data memory allows Data memory to be accessed by 8-bit addresses, which makes the 8-bit CPU access the data memory more rapidly. Nevertheless, 16-bit Data memory addresses can also be generated through the DPTR register.

A96L523 provides on-chip 4k bytes of the ISP type flash program memory, which can be read and written to. Internal data memory (IRAM) is 256 bytes and it includes the stack area.

4.1 Program memory

A 16-bit program counter is capable of addressing up to 64Kbytes, but this device has just 4Kbytes program memory space.

Figure 8 shows the map of the lower part of the program memory. After reset, the CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. External interrupt 1, for example, is assigned to location 000BH. If external interrupt 1 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8 byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.



NOTE: The 4Kbytes includes the Interrupt Vector Region.

Figure 8. Program Memory Map

4.2 Data memory

The internal data memory space is divided into three blocks, which are generally referred to as the lower 128 bytes, upper 128 bytes, and SFR space.

Internal data memory addresses are always one byte wide, which implies an address space of only 256 bytes. However, in fact the addressing modes for internal RAM can accommodate up to 384 bytes by using a simple trick.

Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. Thus Figure 9 shows the upper 128 bytes and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128 bytes of RAM are present in all 8051 devices as mapped in Figure 10. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128 bytes can be accessed by either direct or indirect addressing. The upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

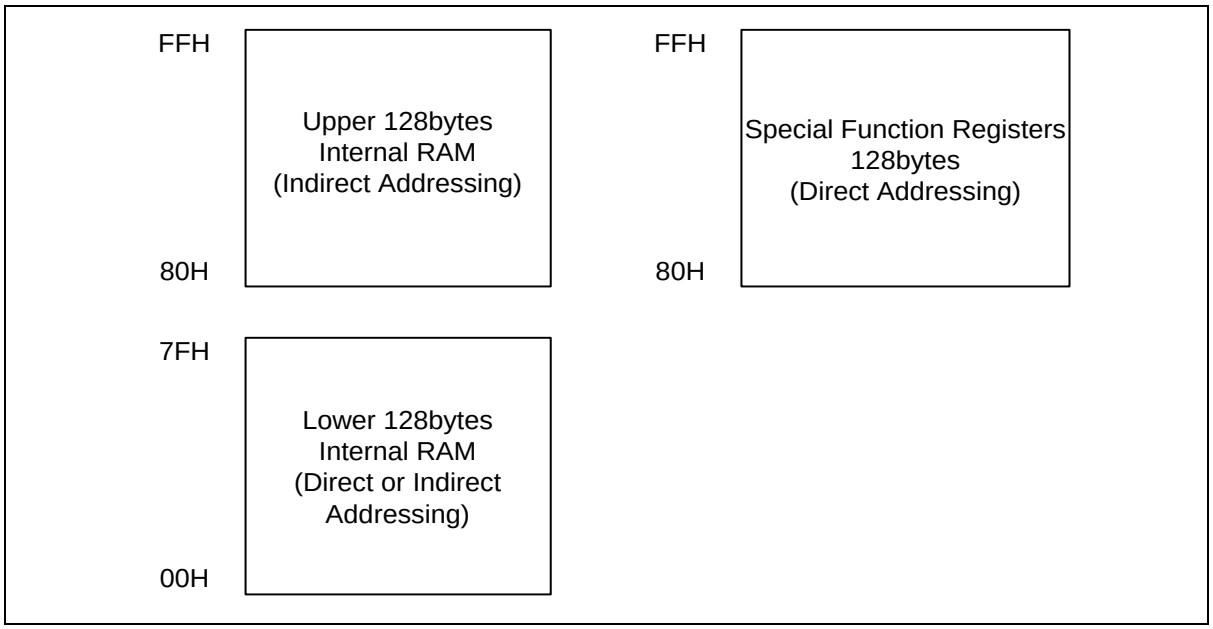


Figure 9. Data Memory Map

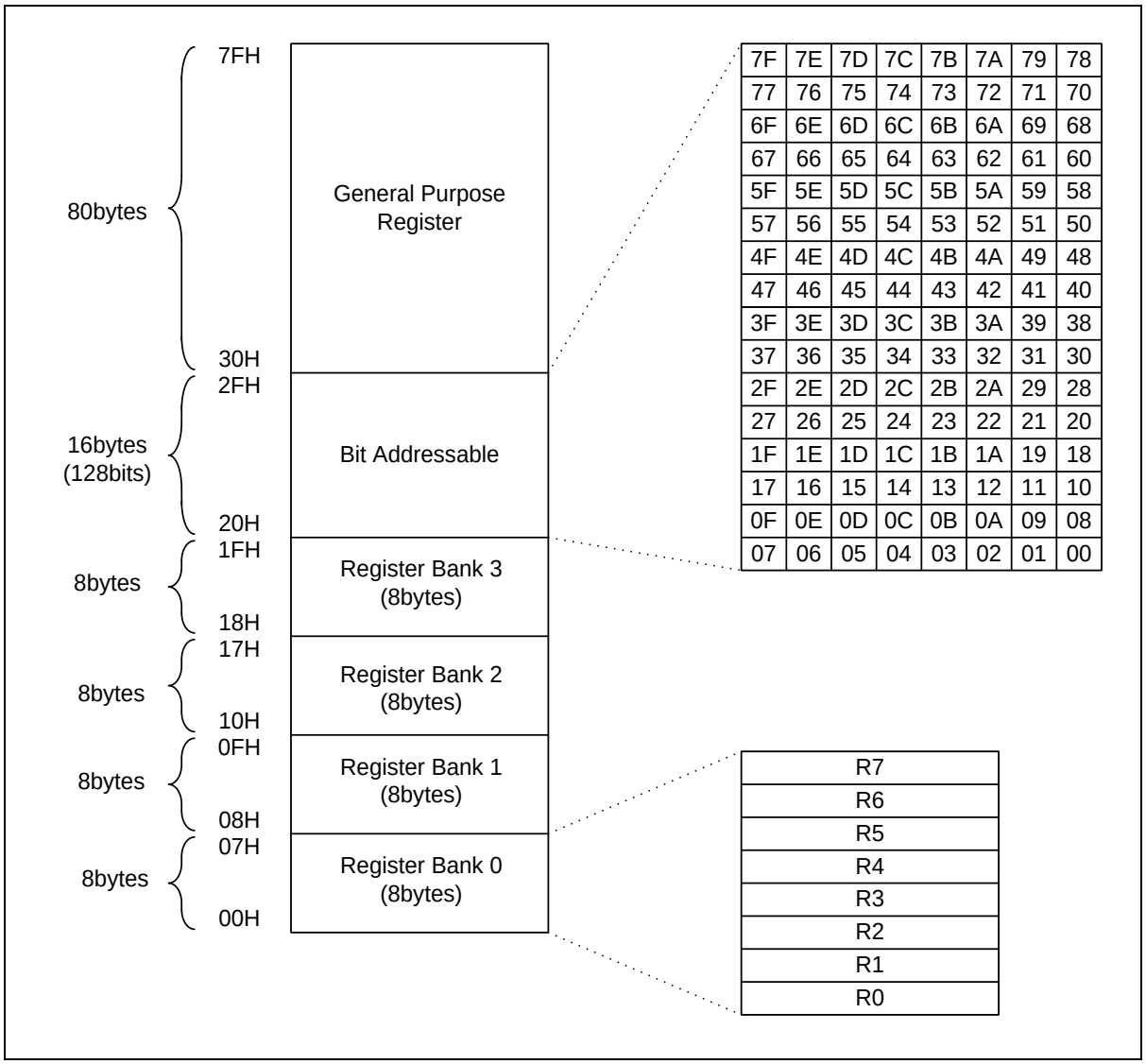


Figure 10. Lower 128Bytes of RAM

4.3 Extended SFR area

This area has no relation with RAM/FLASH. It can be read and written to through SFR with 8-bit unit.

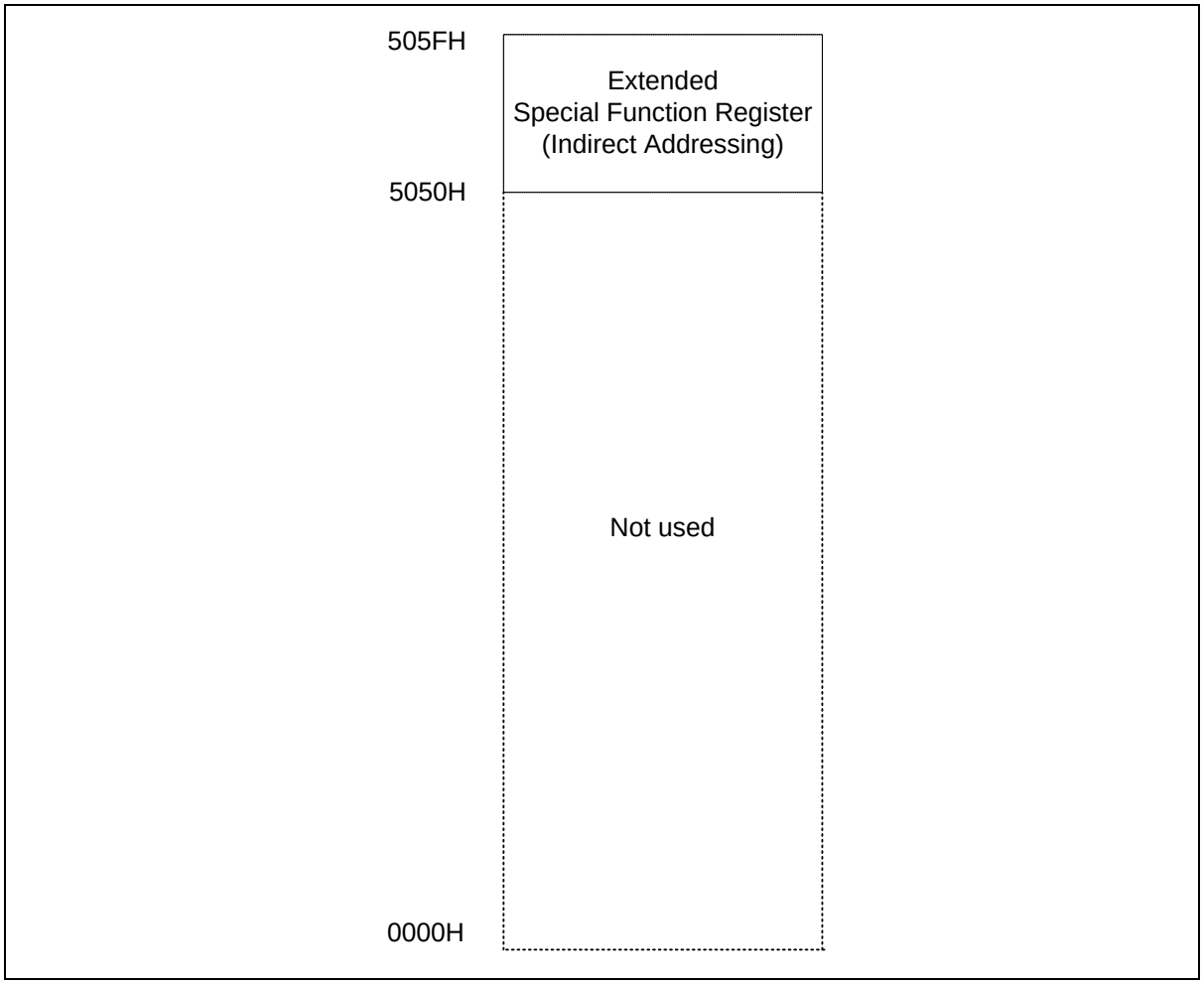


Figure 11. Extended SFR (XSFR) Area

4.4 EEPROM area

This area has no relation with RAM/FLASH. It can be read by DPTR and erased/written through buffer.

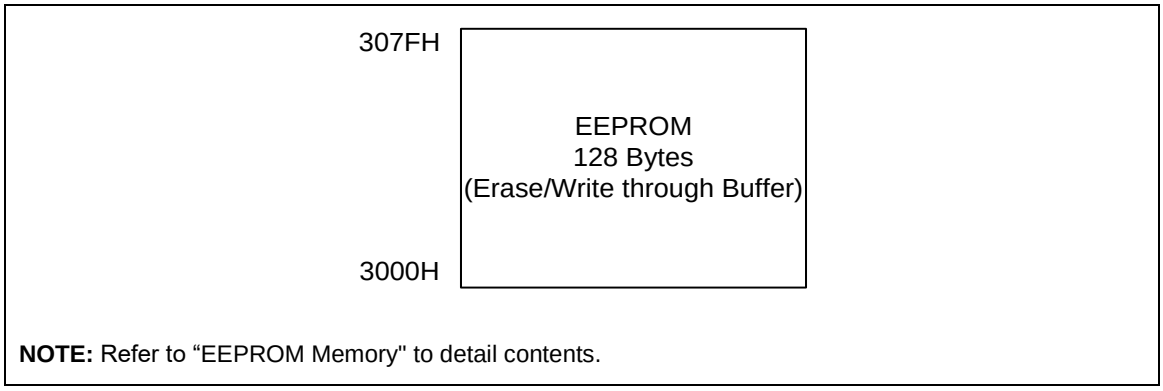


Figure 12. EEPROM Area

4.5 SFR map

4.5.1 SFR map summary

Table 4. SFR Map Summary

	Reserved
	M8051 compatible

	00H/8H(1)	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	–	FSADRH	FSADRM	FSADRL	FIDR	FMCR	–
0F0H	B	–	EESADRL	EESADRH	EEIDR	EEMCR	–	–
0E8H	RSTFR	RXBLEN	TMINRL	TMINRH	TMAXRL	TMAXRH	TENDRL	TENDRH
0E0H	ACC	LIRXDR	TRXARL	TRXARH	–	ICSCR	ICSDR0	ICSDR1
0D8H	LVRCR	TXBLEN	TTXCRL	TTXCRH	TTXDRL	TTXDRH	TTXRRL	TTXRRH
0D0H	PSW	LITXDR	TTXARL	TTXARH	TTXBRL	TTXBRH	–	FCDIN
0C8H	OSCCR	LITXTINF	ADCCRL	ADCCRH	ADCDRL	ADCDRH	–	–
0C0H	LISTATR	LICR0	LICR1	LICR2	LICAPL	LICAPH	TDLYRL	TDLYRH
0B8H	IP	–	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH
0B0H	–	–	T0CRL	T0CRH	T0ADRL	T0ADRH	T0BDRL	T0BDRH
0A8H	IE	IE1	IE2	IE3	–	CHPCR	AMP0CR	AMP1CR
0A0H	EIFLAG	–	EO	–	EIPOL0	EIPOL1	–	–
98H	–	P1IO	P1OD	P1PU	P1FSRL	P1FSRH	–	IRCIDR
90H	–	P0IO	P0OD	P0PU	P0FSRL	P0FSRH	P01DB	IRCTRM
88H	P1	–	SCCR	BITCR	BITCNT	WDTCR	WDTDR/	
080H	P0	SP	DPL	DPH	DPL1	DPH1	–	PCON

NOTE: 00H/8H, these registers are bit-addressable.

Table 5. XSFR Map Summary

	00H/8H	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
5058H	FCDRL	–	–	–	–	–	–	LVRIDR
5050H	FCSARH	FCEARH	FCSARM	FCEARM	FCSARL	FCEARL	FCCR	FCDRH
…	–	–	–	–	–	–	–	–
1010H	DWMAT	DWBNDL	DWDECD	DWINCM	UPMAT	UPBNDL	UPINCD	UPDECM
1008H	SIRENCR	–	–	–	MAXDRL	MAXDRH	MINDRL	MINDRH
1000H	USTCR1	USTCR2	USTCR3	USTST	USTBD	USTDR	–	–

5 I/O ports

The A96L523 has two groups of I/O ports (P0~P1). Each can be easily configured by software as I/O pin, internal pull up and open-drain pin to meet various system configurations and design requirements. Also P0/P1 include function that can generate interrupt according to change of state of the pin.

5.1 Port register

5.1.1 Data register (Px)

Data Register is a bidirectional I/O port. If ports are configured as output ports, data can be written to the corresponding bit of the Px. If ports are configured as input ports, the data can be read from the corresponding bit of the Px.

5.1.2 Direction register (PxIO)

Each I/O pin can be independently used as an input or an output through the PxIO register. Bits cleared in this register will make the corresponding pin of Px to input mode. Set bits of this register will make the pin to output mode. Almost bits are cleared by a system reset, but some bits are set by a system reset.

5.1.3 Pull-up register selection register (PxPU)

The on-chip pull-up resistor can be connected to I/O ports individually with a pull-up resistor selection register (PxPU). The pull-up register selection controls the pull-up resister enable/disable of each port. When the corresponding bit is 1, the pull-up resister of the pin is enabled. When 0, the pull-up resister is disabled. All bits are cleared by a system reset.

5.1.4 Open-drain selection register (PxOD)

There are internally open-drain selection registers (PxOD) for P0. The open-drain selection register controls the open-drain enable/disable of each port. Almost ports become push-pull by a system reset, but some ports become open-drain by a system reset..

5.1.5 De-bounce enable register (PxDB)

P00, P01, P06, P07, P11, and P14 support debounce function. Debounce clocks of each ports are fx/1, fx/4, fx/16, and fx/64.

5.1.6 Port Function selection register (PxFSR)

These registers define alternative functions of ports. Please remember that these registers should be set properly for alternative port function. A reset clears the P0FSRH, P0FSRL, P1FSRH and P1FSRL register to ‘00H’, which makes all pins to normal I/O ports.

5.2 P1 port

5.2.1 P1 port description

P1 is 6-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), P1 pull-up resistor selection register (P1PU), and P1 open-drain selection register (P1OD). Refer to the port function selection registers for the P1 function selection

6 Interrupt controller

The A96L523 supports up to 16 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. They can also have four levels of priority assigned to them. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt source, and is not controllable by software. The interrupt controller has following features:

Receive the request from 16 interrupt source

- group priority
- 4 priority levels
- Multi Interrupt possibility
- If the requests of different priority levels are received simultaneously, the request of higher priority level is served first.
- Each interrupt source can be controlled by EA bit and each IEx bit
- Interrupt latency: 3~9 machine cycles in single interrupt system

The non-maskable interrupt is always enabled. The maskable interrupts are enabled through four pair of interrupt enable registers (IE, IE1, IE2, and IE3). Each bit of IE, IE1, IE2, IE3 register individually enables/disables the corresponding interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to ‘0’, all interrupts are disabled: when EA is set to ‘1’, interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to ‘0’ jumping to an interrupt service vector and set to ‘1’ executing the [RETI] instruction. The A96L523 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP and IP1.

Figure 13 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority of a group is set by two bits of interrupt priority registers (one bit from IP, another one from IP1). Interrupt service routine serves higher priority interrupt first. If two requests of different priority levels are received simultaneously, the request of higher priority level is served prior to the lower one.

Interrupt Group	Highest → Lowest			
0 (Bit0)	Interrupt 0	Interrupt 6	Interrupt 12	Interrupt 18
1 (Bit1)	Interrupt 1	Interrupt 7	Interrupt 13	Interrupt 19
2 (Bit2)	Interrupt 2	Interrupt 8	Interrupt 14	Interrupt 20
3 (Bit3)	Interrupt 3	Interrupt 9	Interrupt 15	Interrupt 21
4 (Bit4)	Interrupt 4	Interrupt 10	Interrupt 16	Interrupt 22
5 (Bit5)	Interrupt 5	Interrupt 11	Interrupt 17	Interrupt 23

Highest

Lowest

Figure 13. Interrupt Group Priority Level

6.1 External interrupt

The external interrupt on INT0 ~ INT5 pins receive various interrupt request depending on the external interrupt polarity 0 register (EIPOL0) and external interrupt polarity 1 register (EIPOL1) as shown in Figure 14. Also each external interrupt source has enable/disable bits. The external interrupt flag register (EIFLAG) provides the status of external interrupts.

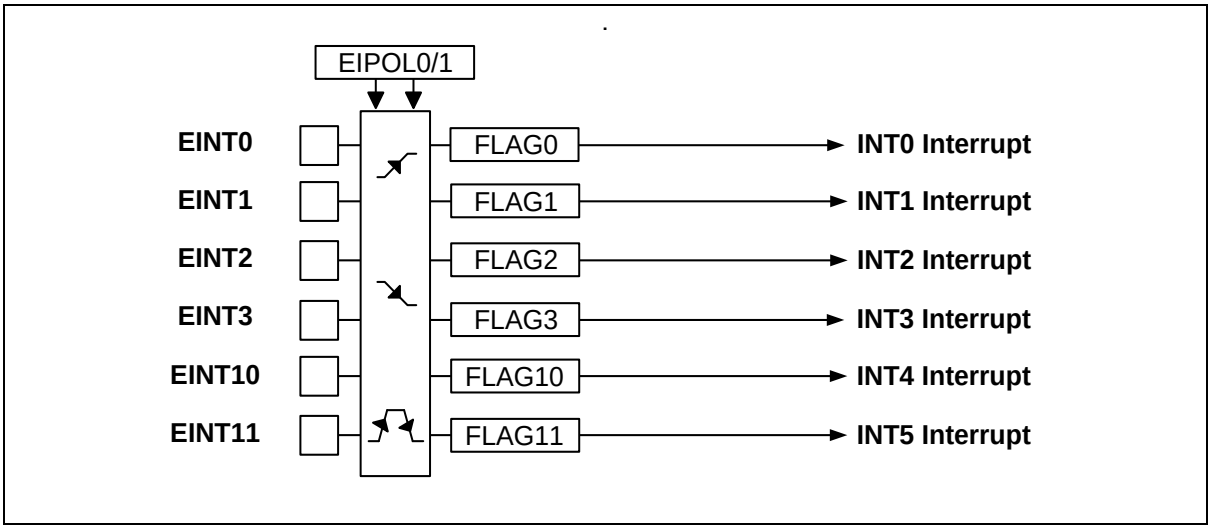
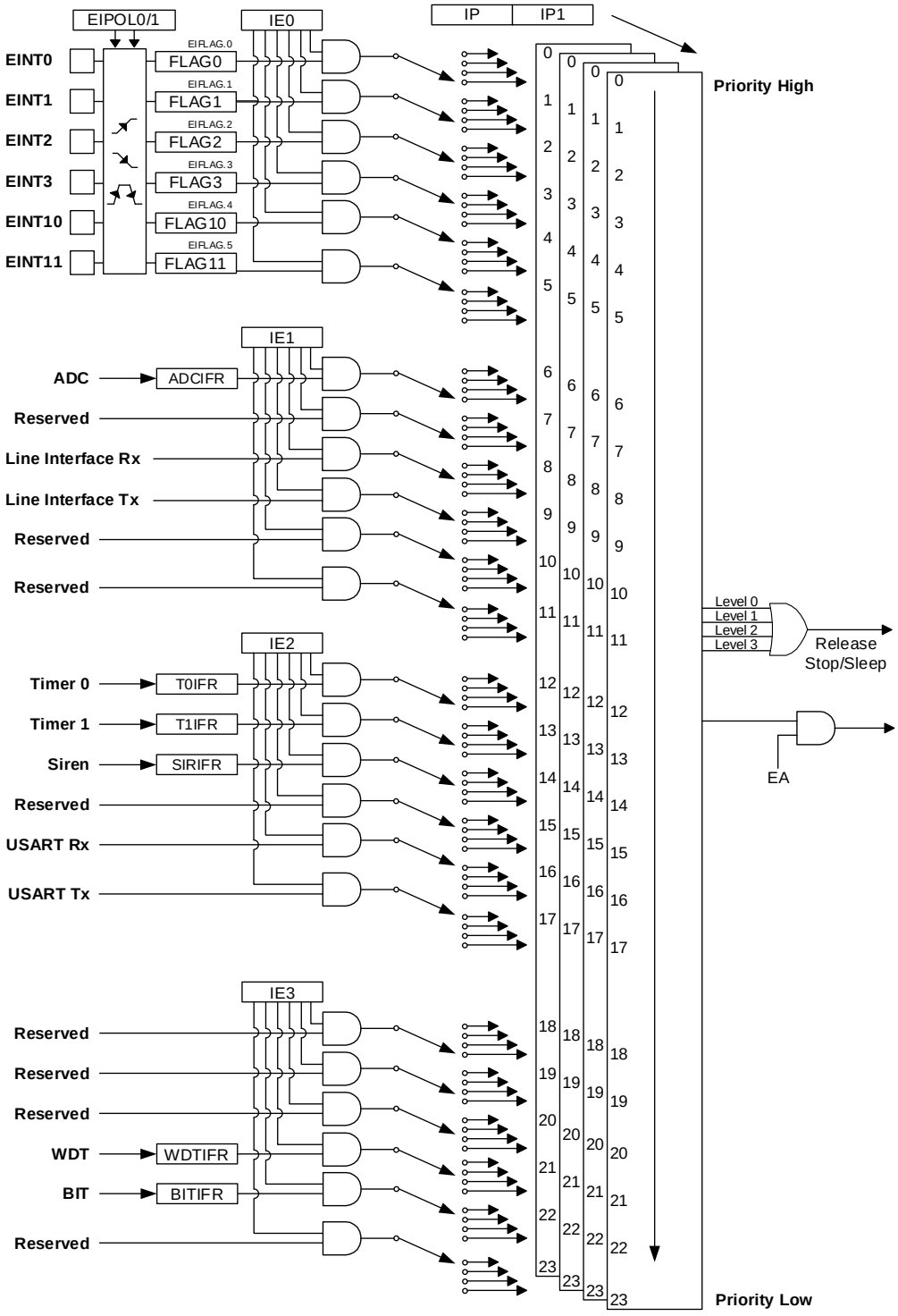


Figure 14. External Interrupt Description

6.2 Block diagram



NOTES:

1. The release signal for stop/idle mode may be generated by all interrupt sources which are enabled without reference to the priority level.
2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

Figure 15. Interrupt Controller Block Diagram

6.3 Interrupt vector table

The interrupt controller supports 24 interrupt sources as shown in the Table 6. When interrupt is served, Long Call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have their own priority order.

Table 6. Interrupt Vector Address Table

Interrupt source	Symbol	Interrupt enable bit	Priority	Mask	Vector addr.
Hardware RESET	RESETB	-	0	Non-Maskable	0000H
External Interrupt 0	INT0	IE.0	1	Maskable	0003H
External Interrupt 1	INT1	IE.1	2	Maskable	000BH
External Interrupt 2	INT2	IE.2	3	Maskable	0013H
External Interrupt 3	INT3	IE.3	4	Maskable	001BH
External Interrupt 10	INT4	IE.4	5	Maskable	0023H
External Interrupt 11	INT5	IE.5	6	Maskable	002BH
ADC Interrupt	INT6	IE1.0	7	Maskable	0033H
–	INT7	IE1.1	8	Maskable	003BH
Line Interface Rx	INT8	IE1.2	9	Maskable	0043H
Line Interface Tx	INT9	IE1.3	10	Maskable	004BH
–	INT10	IE1.4	11	Maskable	0053H
–	INT11	IE1.5	12	Maskable	005BH
T0 Interrupt	INT12	IE2.0	13	Maskable	0063H
T1 Interrupt	INT13	IE2.1	14	Maskable	006BH
Siren Interrupt	INT14	IE2.2	15	Maskable	0073H
–	INT15	IE2.3	16	Maskable	007BH
USART Rx Interrupt	INT16	IE2.4	17	Maskable	0083H
USART Tx Interrupt	INT17	IE2.5	18	Maskable	008BH
–	INT18	IE3.0	19	Maskable	0093H
–	INT19	IE3.1	20	Maskable	009BH
–	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
–	INT23	IE3.5	24	Maskable	00BBH

For maskable interrupt execution, EA bit must set ‘1’ and specific interrupt must be enabled by writing ‘1’ to associated bit in the IEx. If an interrupt request is received, the specific interrupt request flag is set to ‘1’. And it remains ‘1’ until CPU accepts interrupt. If the interrupt is served, the interrupt request flag will be cleared automatically.

7 Clock generator

As shown in Figure 16, the clock generator produces the basic clock pulses which provide the system clock to be supplied to the CPU and the peripheral hardware.

The default system clock is 1MHz INT-RC Oscillator and the default division rate is one. In order to stabilize system internally, it is used 1MHz INT-RC oscillator on POR.

- Calibrated Internal RC Oscillator (1 MHz)
  - INT-RC OSC/8 (0.125 MHz)
  - INT-RC OSC/4 (0.25 MHz)
  - INT-RC OSC/2 (0.5 MHz)
  - INT-RC OSC/1 (1 MHz, Default system clock)
- Internal WDTRC Oscillator (1 kHz)

7.1 Clock generator block diagram

In this section, a clock generator of A96L523 is described in a block diagram.

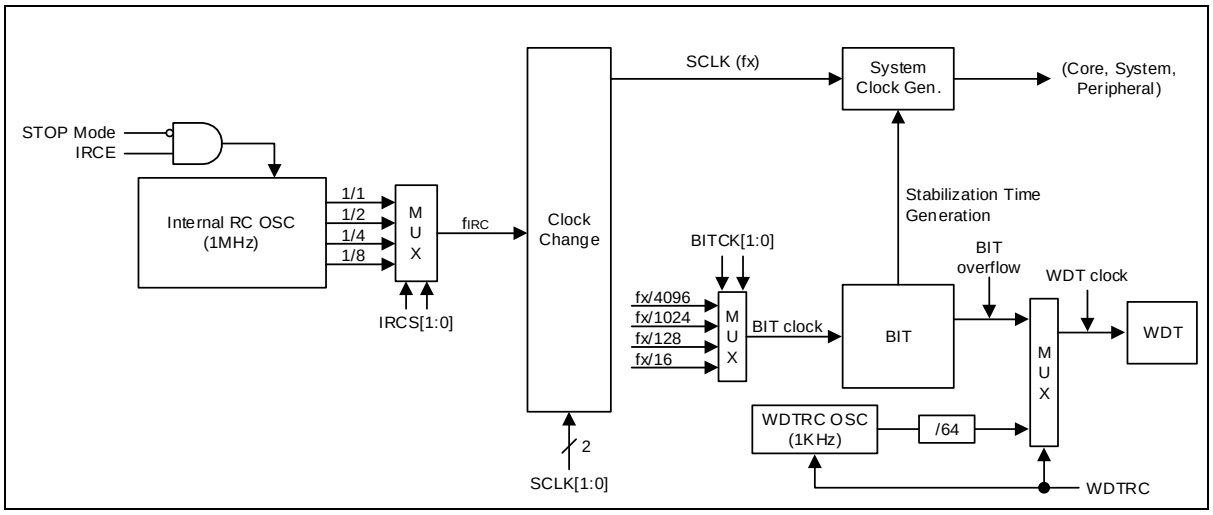


Figure 16. Clock Generator Block Diagram

8 Basic interval timer

The A96L523 has one 8-bit basic interval timer that is free-run and can't stop. Block diagram is shown in Figure 17. In addition, the basic interval timer generates the time base for watchdog timer counting. It also provides a basic interval timer interrupt (BITIFR).

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As a timer, BIT generates a timer interrupt.

8.1 BIT block diagram

In this section, basic interval timer of A96L523 is described in a block diagram.

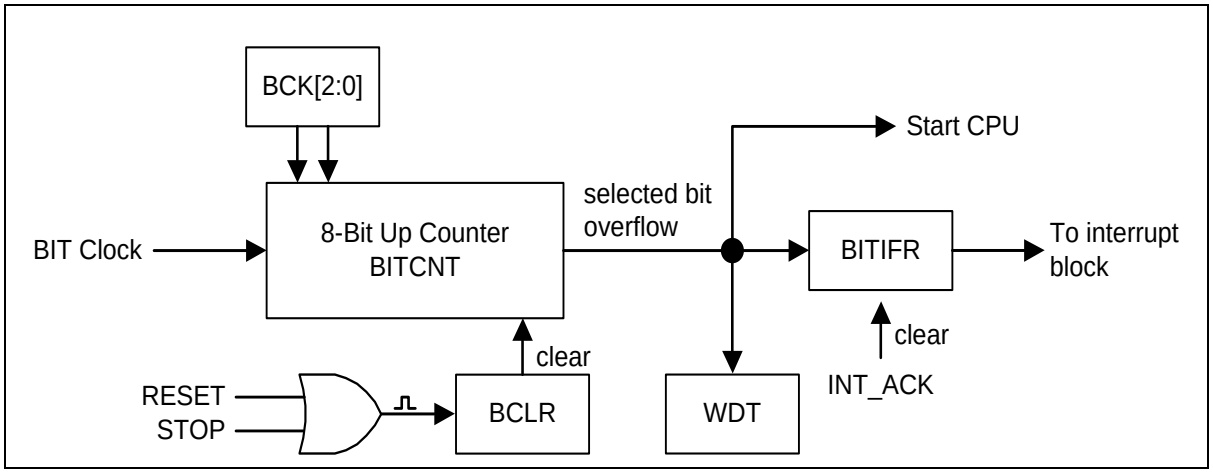


Figure 17. Basic Interval Timer Block Diagram

9 Watchdog timer

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or something like that, and resumes the CPU to the normal state. The watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. It is possible to use free running 8-bit timer mode (WDTRSON='0') or watch dog timer mode (WDTRSON='1') as setting WDTCR[6] bit. If WDTCR[5] is written to '1', WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically.

The watchdog timer consists of 8-bit binary counter and the watchdog timer data register. When the value of 8-bit binary counter is equal to the 8 bits of WDTCNT, the interrupt request flag is generated. This can be used as Watchdog timer interrupt or reset of CPU in accordance with the bit WDTRSON.

The input clock source of watch dog timer is the BIT overflow. The interval of watchdog timer interrupt is decided by BIT overflow period and WDTDR set value. The equation can be described as

WDT Interrupt Interval = (BIT Interrupt Interval) X (WDTDR Value+1)

9.1 WDT interrupt timing waveform

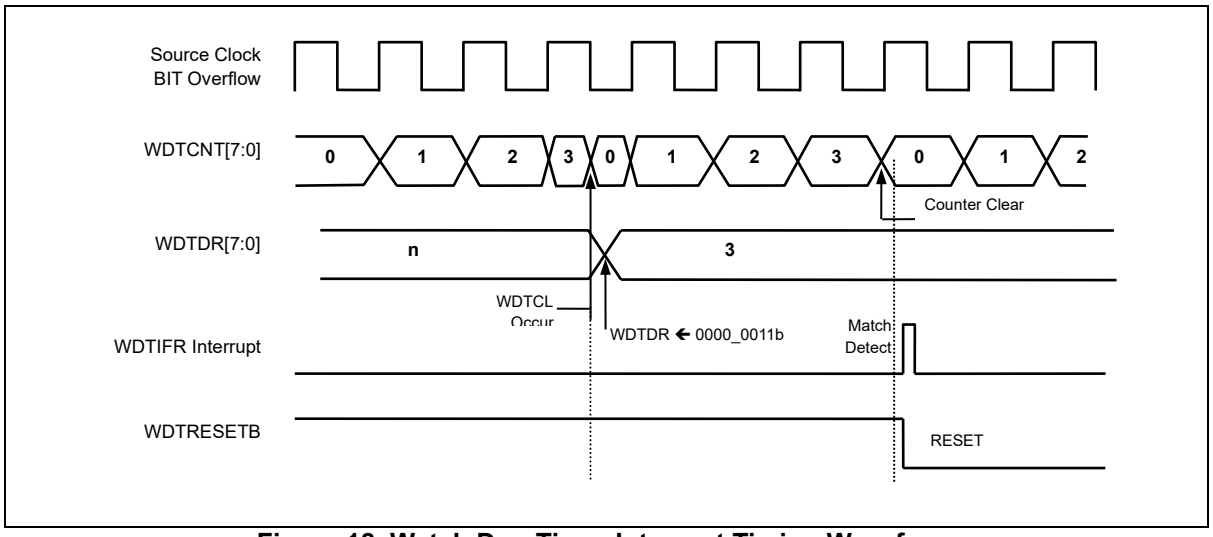
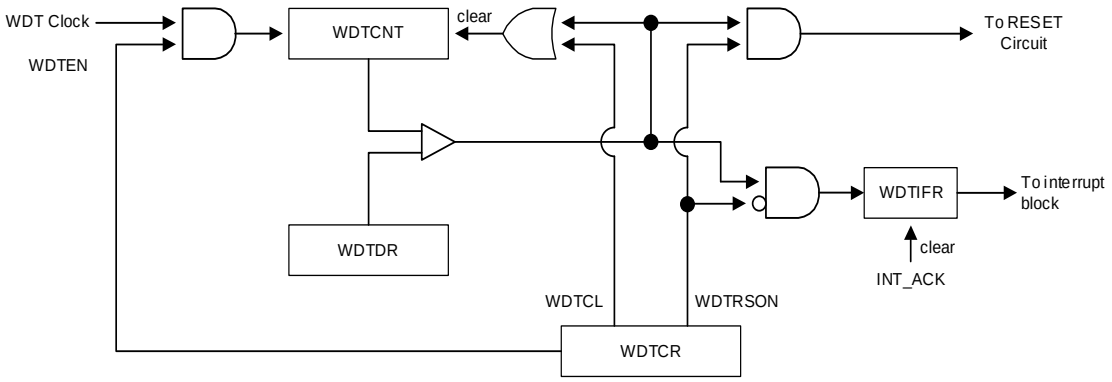


Figure 18. Watch Dog Timer Interrupt Timing Waveform

9.2 WDT block diagram



NOTE: The watch-dog timer clock depends on WDTCK bit of WDTCR register. Refer to the watch-dog timer control register.

Figure 19. Watch Dog Timer Block Diagram

10 Timer 0/1

10.1 Timer 0

The 16-bit timer 0 consists of multiplexer, timer 0 A data register high/low, timer 0 B data register high/low and timer 0 control register high/low (T0ADRH, T0ADRL, T0BDRH, T0BDRL, T0CRH, T0CRL).

It has four operating modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 0 can be clocked by an internal or an external clock source (EC0). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T0CK[2:0]).

TIMER 0 clock source: f_X/1, 2, 4, 8, 64, 512, 2048 and EC0

In the capture mode, by EINT10, the data is captured into input capture data register (T0BDRH/T0BDRL). Timer 0 outputs the comparison result between counter and data register through T0O port in timer/counter mode. Also Timer 0 outputs PWM wave form through PWM0O port in the PPG mode.

Table 7. Timer 0 Operating Modes

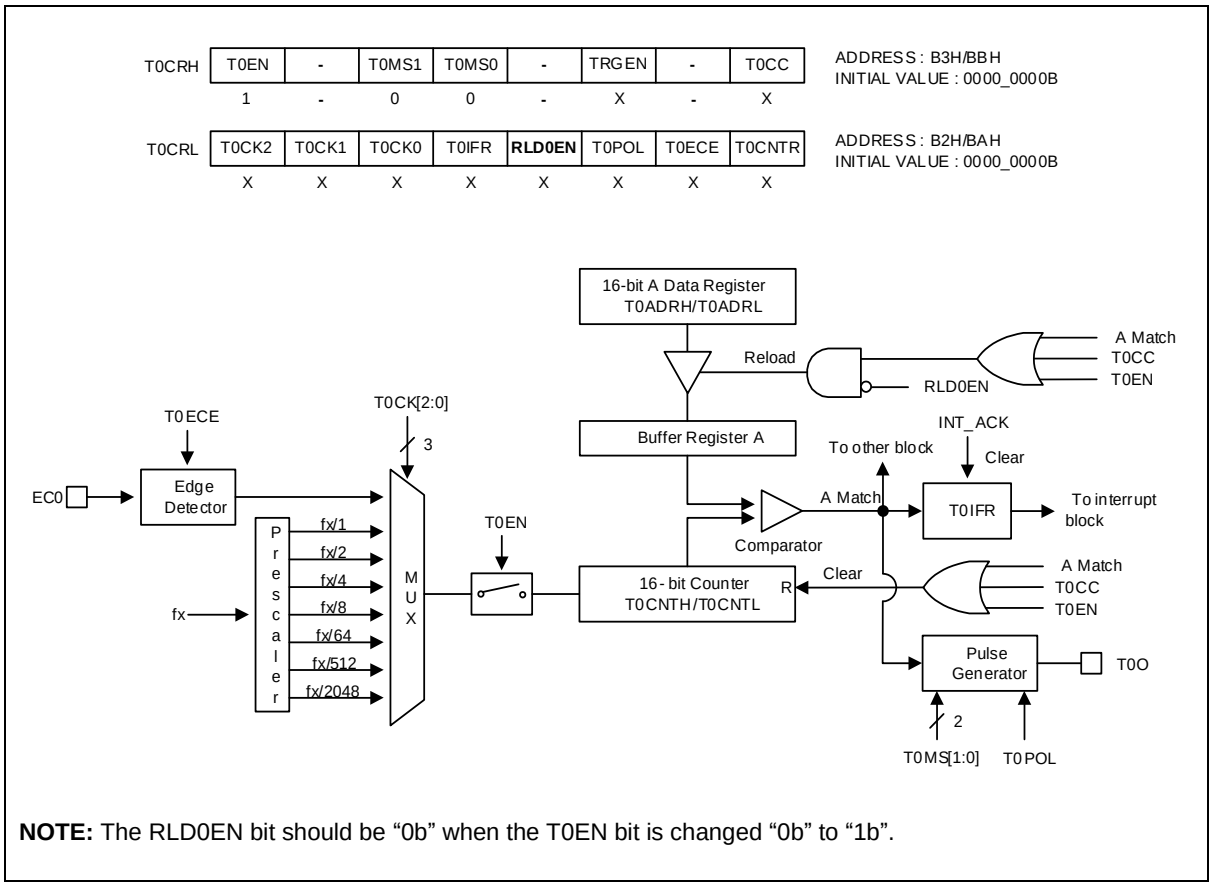
T0EN	P1FSRL[2](T0)	T0MS[1:0]	T0CK[2:0]	Timer 0
1	1	00	XXX	16 Bit Timer/Counter Mode
1	0	01	XXX	16 Bit Capture Mode
1	1	10	XXX	16 Bit PPG Mode(one-shot mode)
1	1	11	XXX	16 Bit PPG Mode(repeat mode)

10.1.1 16-bit timer/counter mode

The 16-bit timer/counter mode is selected by control register as shown in Figure 20.

The 16-bit timer have counter and data register. The counter register is increased by internal or external clock input. Timer 0 can use the input clock with one of 1, 2, 4, 8, 64, 512 and 2048 prescaler division rates (T0CK[2:0]). When the value of T0CNTH, T0CNTL and the value of T0ADRH, T0ADRL are identical in Timer 0 respectively, a match signal is generated and the interrupt of Timer 0 occurs. The T0CNTH, T0CNTL value is automatically cleared by match signal. It can be also cleared by software (T0CC).

The external clock (EC0) counts up the timer at the rising edge. If the EC0 is selected as a clock source by T0CK[2:0], EC0 port should be set to the input port by P12IO bit.



NOTE: The RLD0EN bit should be “0b” when the T0EN bit is changed “0b” to “1b”.

Figure 20. 16-bit Timer/Counter Mode for Timer 0

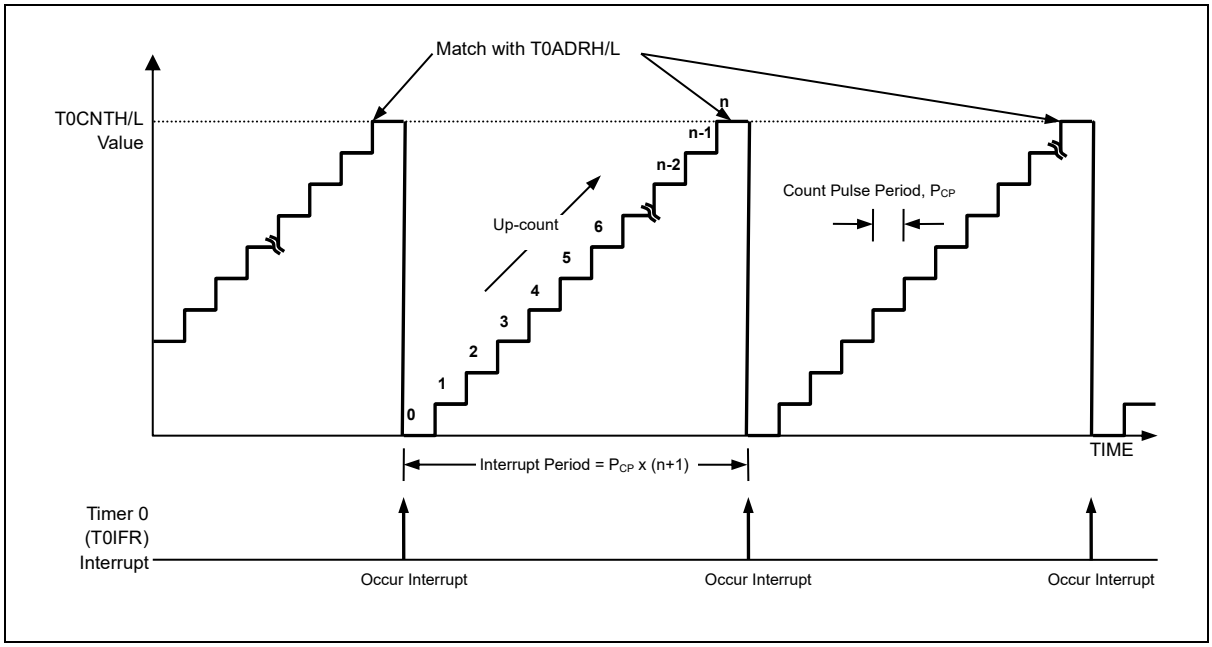


Figure 21. 16-bit Timer/Counter 0 Example

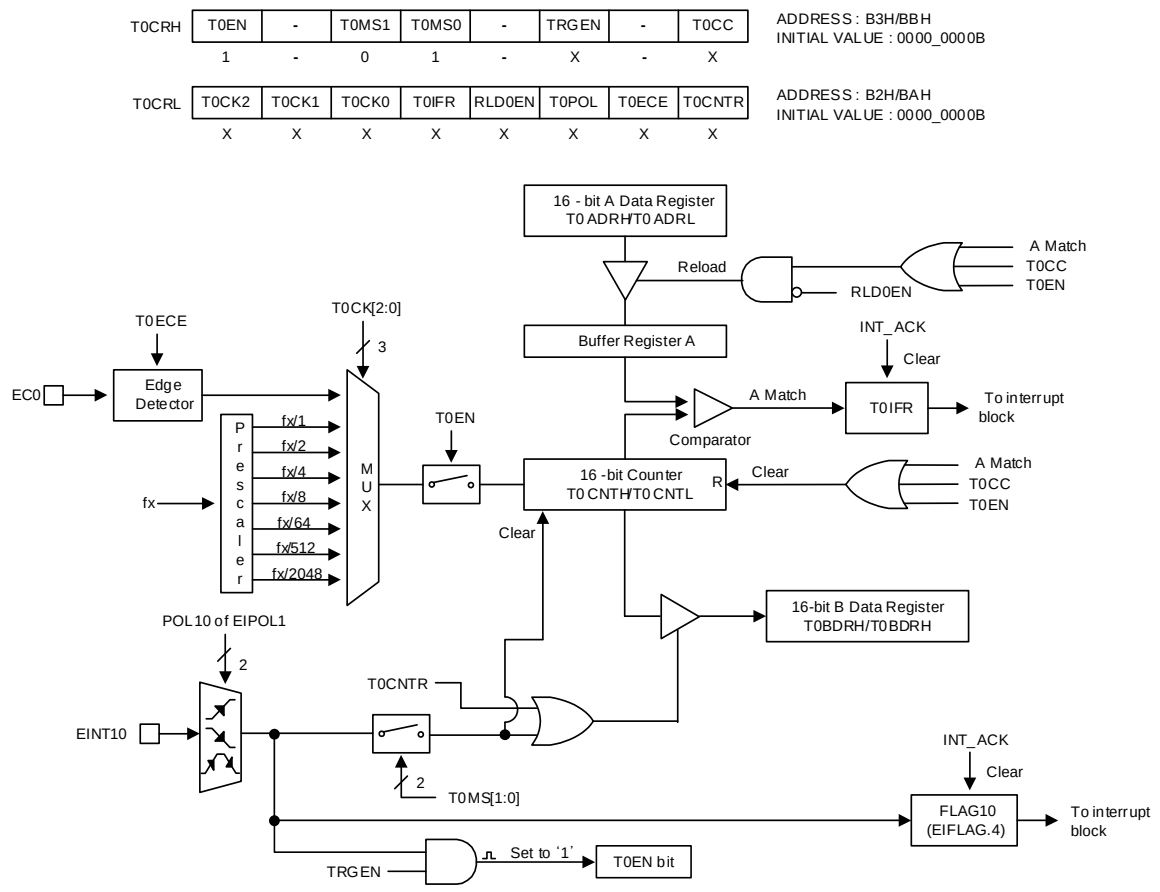
10.1.2 16-bit capture mode

The 16-bit timer 0 capture mode is set by T0MS[1:0] as '01'. The clock source can use the internal/external clock. Basically, it has the same function as the 16-bit timer/counter mode and the interrupt occurs when T0CNTH/T0CNTL is equal to T0ADRH/T0ADRL. The T0CNTH, T0CNTL values are automatically cleared by match signal. It can be also cleared by software (T0CC).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T0BDRH/T0BDRL.

According to EIPOL1 registers setting, the external interrupt EINT10 function is chosen. Of course, the EINT10 pin must be set as an input port.



NOTE: The RLD0EN bit should be "0b" when the T0EN bit is changed "0b" to "1b".

Figure 22. 16-bit Capture Mode for Timer 0

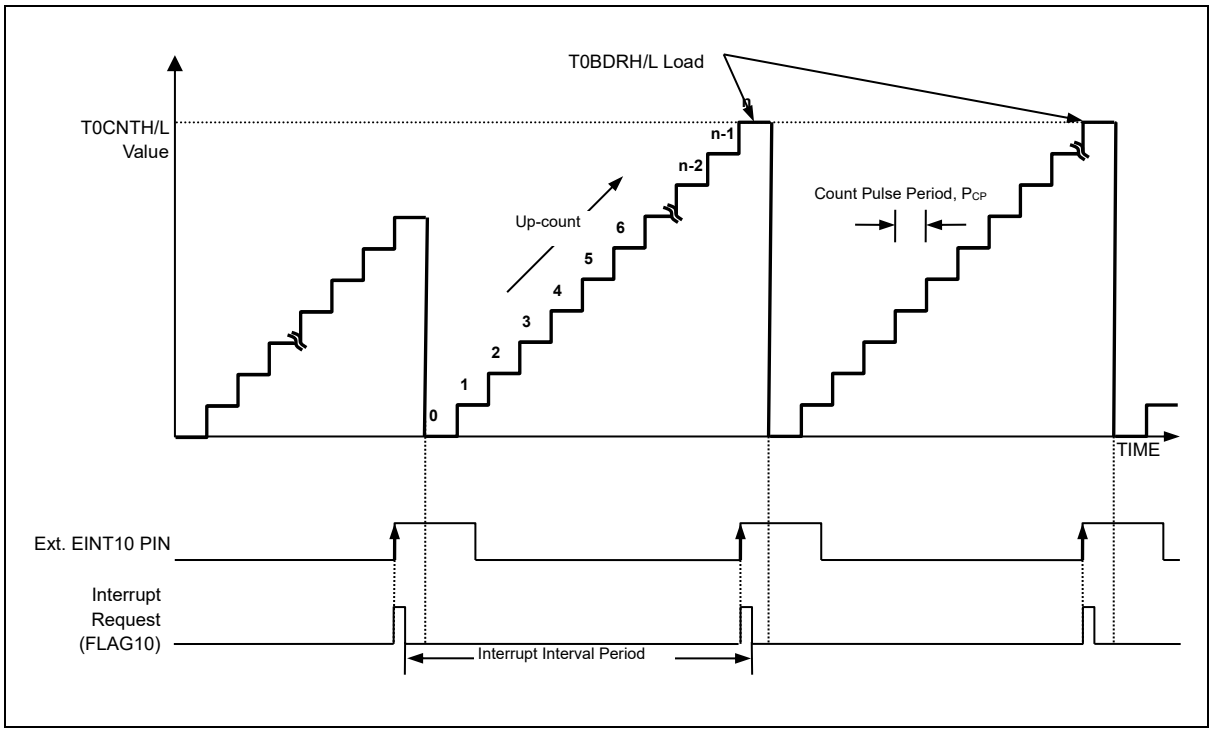


Figure 23. Input Capture Mode Operation for Timer 0

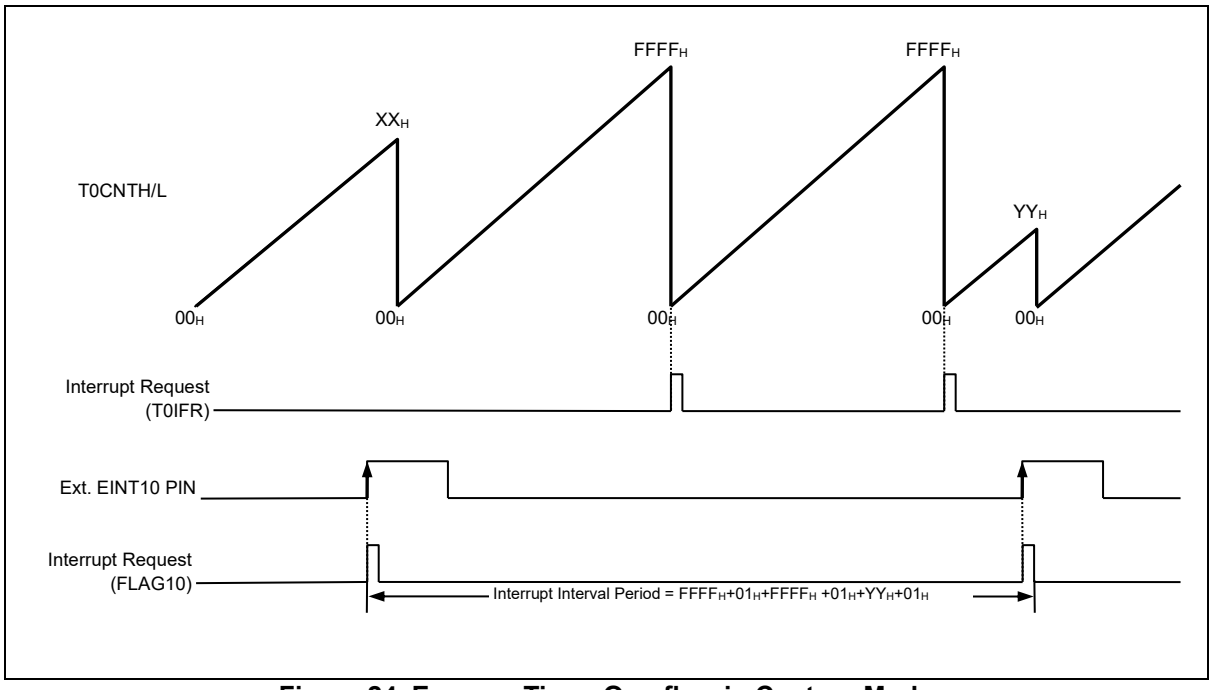
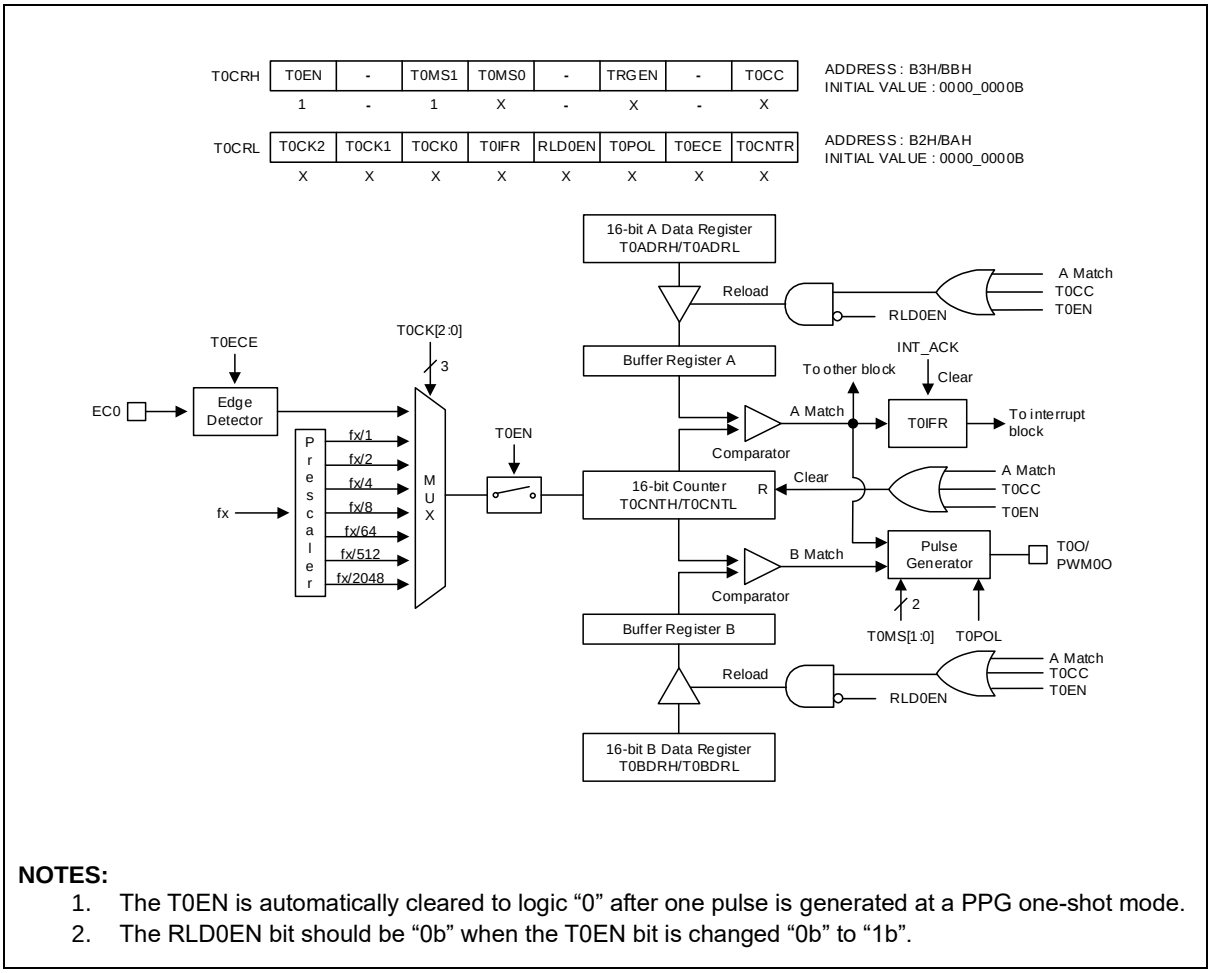


Figure 24. Express Timer Overflow in Capture Mode

10.1.3 16-bit PPG mode

The timer 0 has a PPG (Programmable Pulse Generation) function. In PPG mode, T0O/PWM0O pin outputs up to 16-bit resolution PWM output. This pin should be configured as a PWM output by setting P1FSRL[2] to '1' (T0). The period of the PWM output is determined by the T0ADRH/T0ADRL. And the duty of the PWM output is determined by the T0BDRH/T0BDRL.



NOTES:

1. The T0EN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.
2. The RLD0EN bit should be "0b" when the T0EN bit is changed "0b" to "1b".

Figure 25. 16-bit PPG Mode for Timer 0

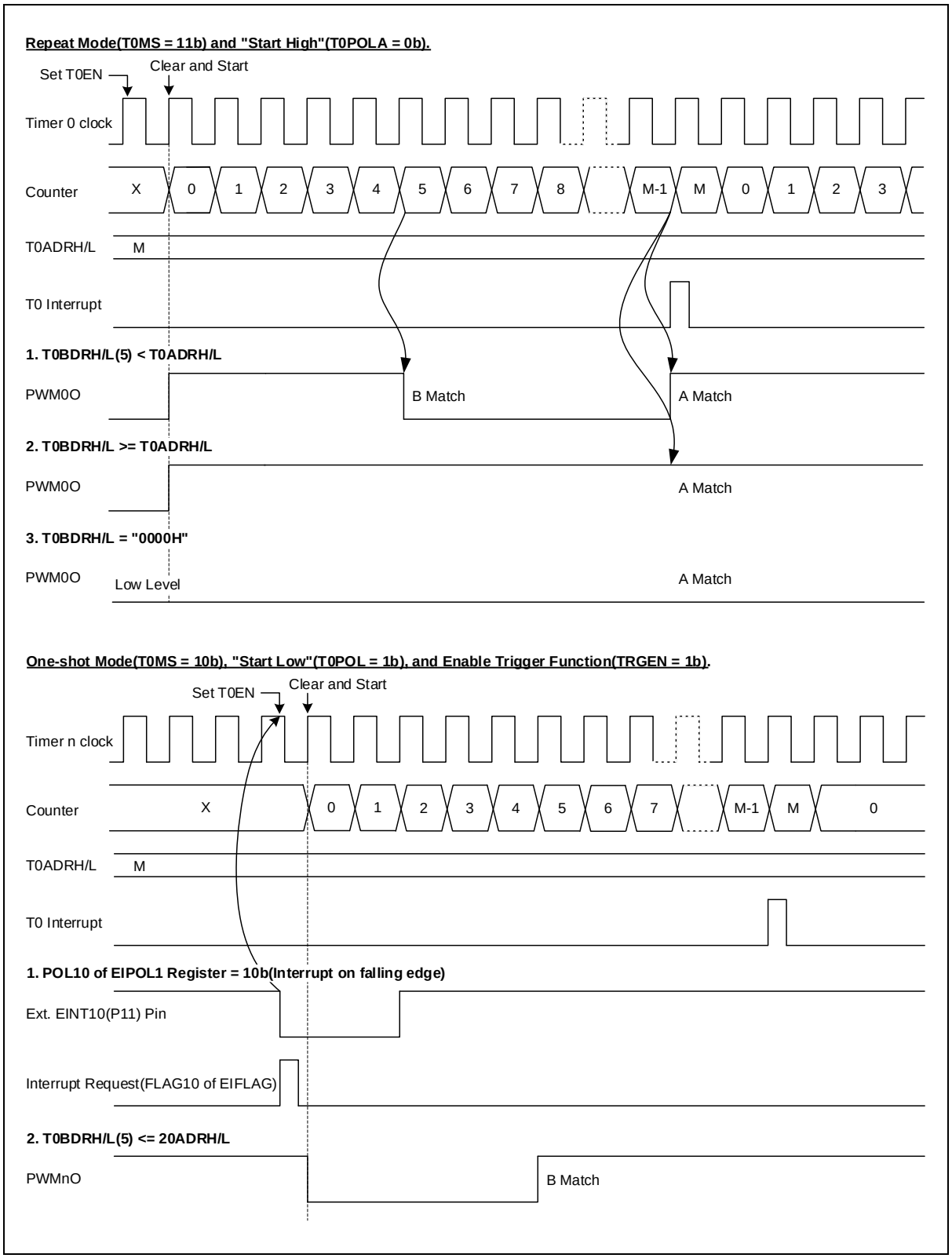
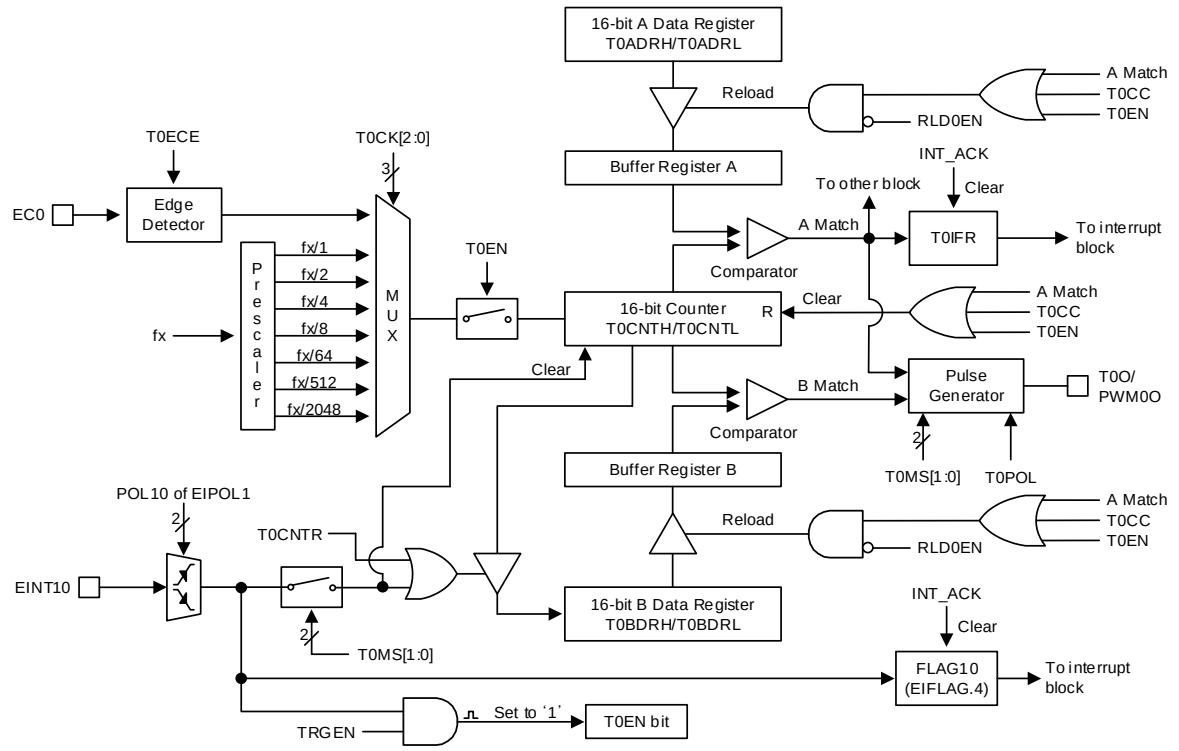


Figure 26. 16-bit PPG Mode Timing chart for Timer 0

10.1.4 Block diagram



NOTES:

1. The T0EN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.
2. The RLD0EN bit should be "0b" when the T0EN bit is changed "0b" to "1b".

Figure 27. 16-bit Timer 0 Block Diagram

10.2 Timer 1

A 16-bit timer TIMER 1 incorporates a multiplexer and nineteen registers such as timer1A data register high/low, timer1B data register high/low, timer1 control register high/low, siren control register, siren max data high/low register, siren min data high/low register, siren up/down match times register, siren up/down bundle times register, siren down decrement data register, siren down increment match times register, siren up increment data register and siren up decrement match times register (T1ADRH, T1ADRL, T1BDRH, T1BDRL, T1CRH, T1CRL, SIRENCR, MAXDRL, MAXDRH, MINDRL, MINDRH, DWMAT, DWBNDL, DWDECD, DWINCM, UPMAT, UPBNDL, UPINCD, UPDECM).

TIMER 1 operates in one of five operating modes:

- 16-bit capture mode
- 16-bit timer/ counter mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)
- Siren

Specifically in capture mode, data is captured into input capture data register (T1BDRH/T1BDRL) by EINT10/EINT11. TIMER 1 outputs the comparison result between counter and data register through T1O port in timer/counter mode. TIMER 1 outputs PWM wave form through PWM1O port in the PPG mode.

A timer/counter 1 uses an internal clock or an external clock (EC1) as an input clock source. The clock sources are introduced below, and one is selected by clock selection logic which is controlled by clock selection bits (T1CK[2:0]).

- TIMER 1 clock sources: f_X/1, 2, 4, 8, 64, 512, 2048 and EC1

Table 8. TIMER 1 Operating Modes

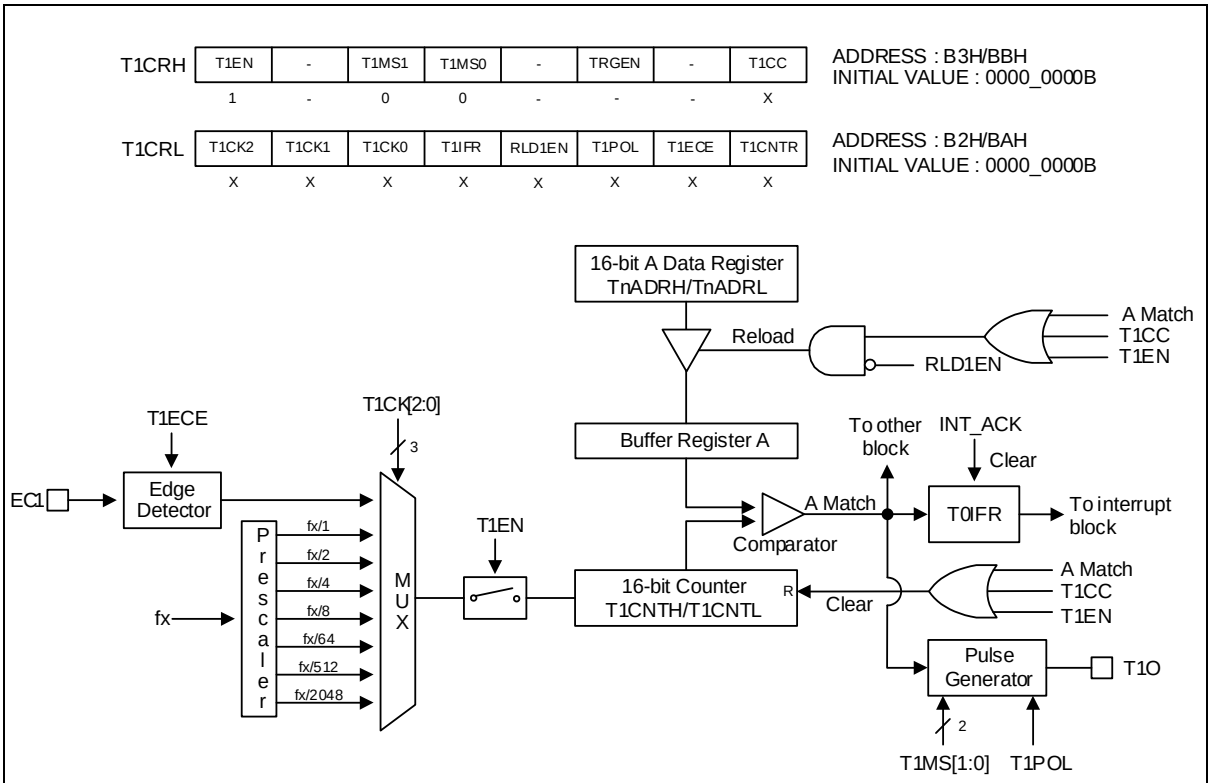
T1EN	P1FSRH[1:0](T1)	T1MS[1:0]	T1CK[2:0]	Timer 1
1	01	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	01	10	XXX	16 Bit PPG Mode(one-shot mode)
1	01	11	XXX	16 Bit PPG Mode(repeat mode)

10.2.1 16-bit timer/ counter mode

16-bit timer/counter mode is selected by control register as shown in Figure 28. As shown in Figure 28, a 16-bit timer has a counter and data registers.

Counter registers have increasing values by internal or external clock input. TIMER 1 can use the input clock with one of 1, 2, 4, 8, 64, 512 and 2048 prescaler division rates (T1CK[2:0]). When the value of T1CNTH, T1CNTL and the value of T1ADRH, T1ADRL are identical each other in Timer 1, a match signal is generated and the interrupt of Timer 1 occurs. T1CNTH, T1CNTL value is automatically cleared by match signal. It can be cleared by software (T1CC) too.

The external clock (EC1) counts up the timer at the rising edge. If the EC1 is selected as a clock source by T1CK[2:0], EC1 port should be set to the input port by P13IO bit.



NOTE: RLD1EN bit must be '0b' when T1EN bit is changed from '0b' to '1b'.

Figure 28. 16-bit Timer/ Counter Mode of TIMER 1

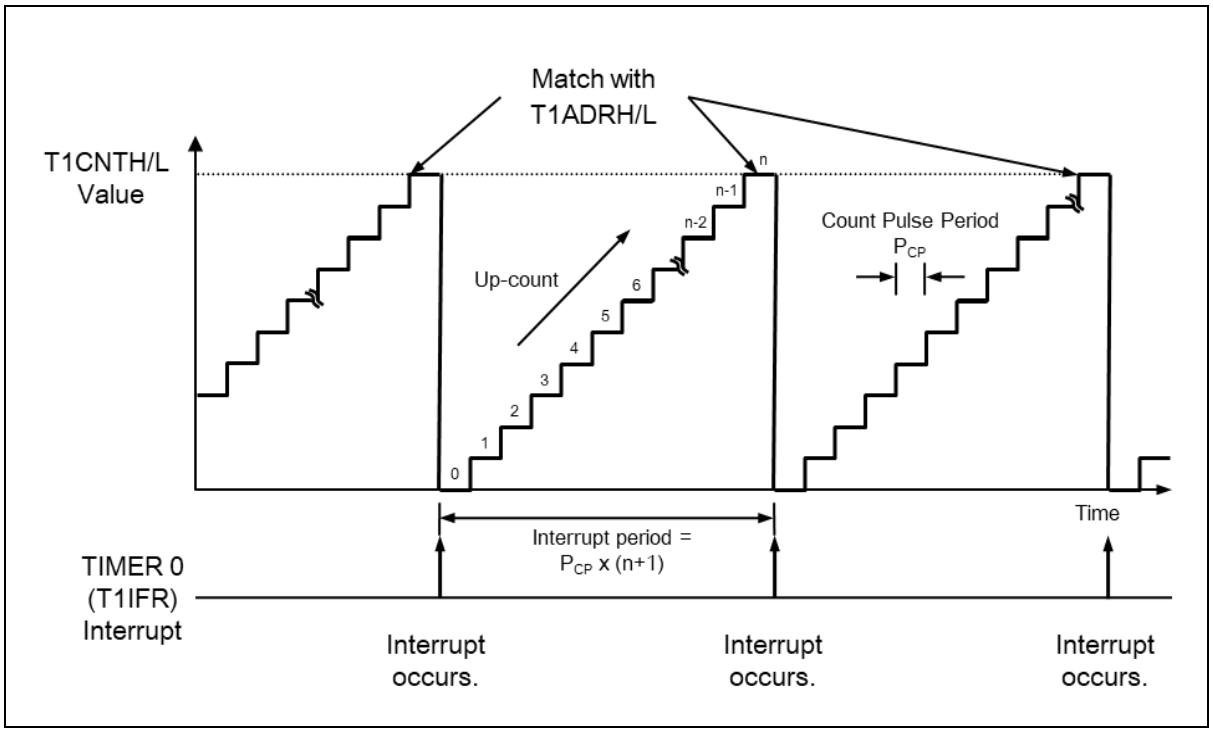
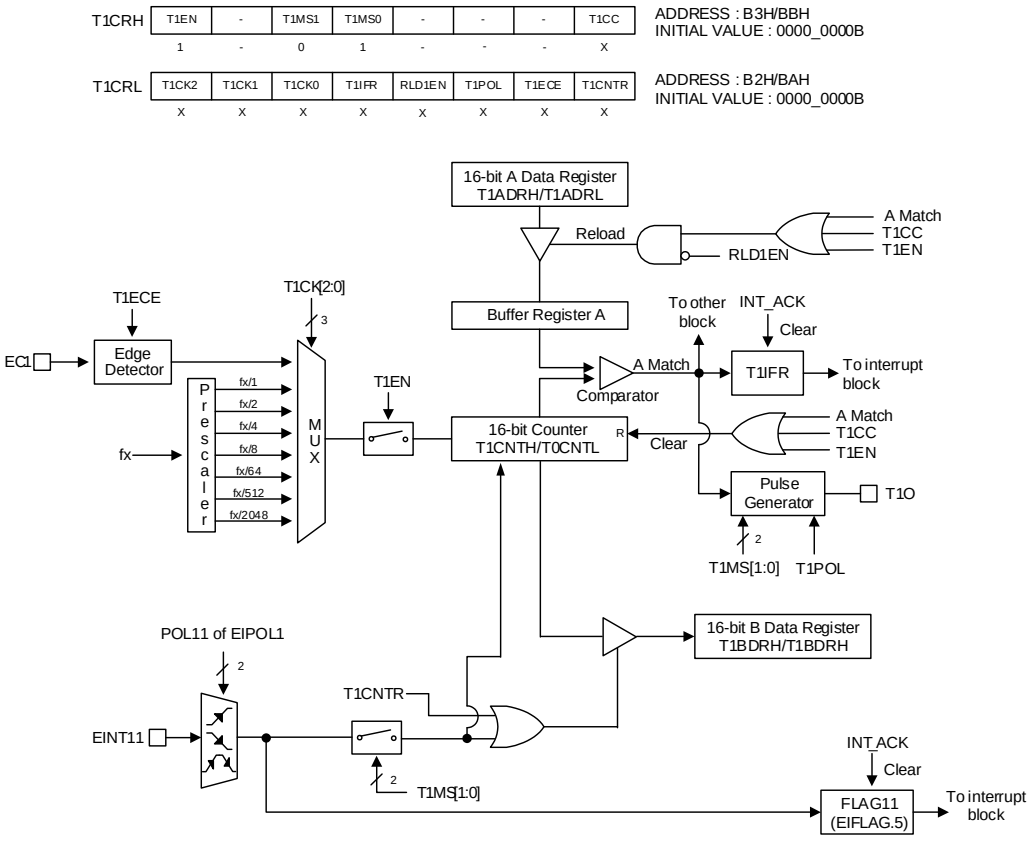


Figure 29. 16-bit Timer/ Counter 1 Interrupt Example

10.2.2 16-bit capture mode

16-bit timer 1 capture mode is set by configuring T1MS[1:0] as '01'. It uses an internal/external clock as a clock source. Basically, the 16-bit timer 1 capture mode has the same function as the 16-bit timer/counter mode, and the interrupt occurs when T1CNTH/T1CNTL is equal to T1ADRH/T1ADRL. The T1CNTH, T1CNTL values are automatically cleared by match signal. It can be cleared by software (T1CC) too.

A timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer. Capture result is loaded into T0BDRH/T0BDRL. According to EIPOL1 registers settings, the external interrupt EINT10/EINT11 function is selected. EINT10/EINT11 pin must be set as an input port.



NOTE: RLD1EN bit must be '0b' when T1EN bit is changed from '0b' to '1b'.

Figure 30. 16-bit Capture Mode of TIMER 1

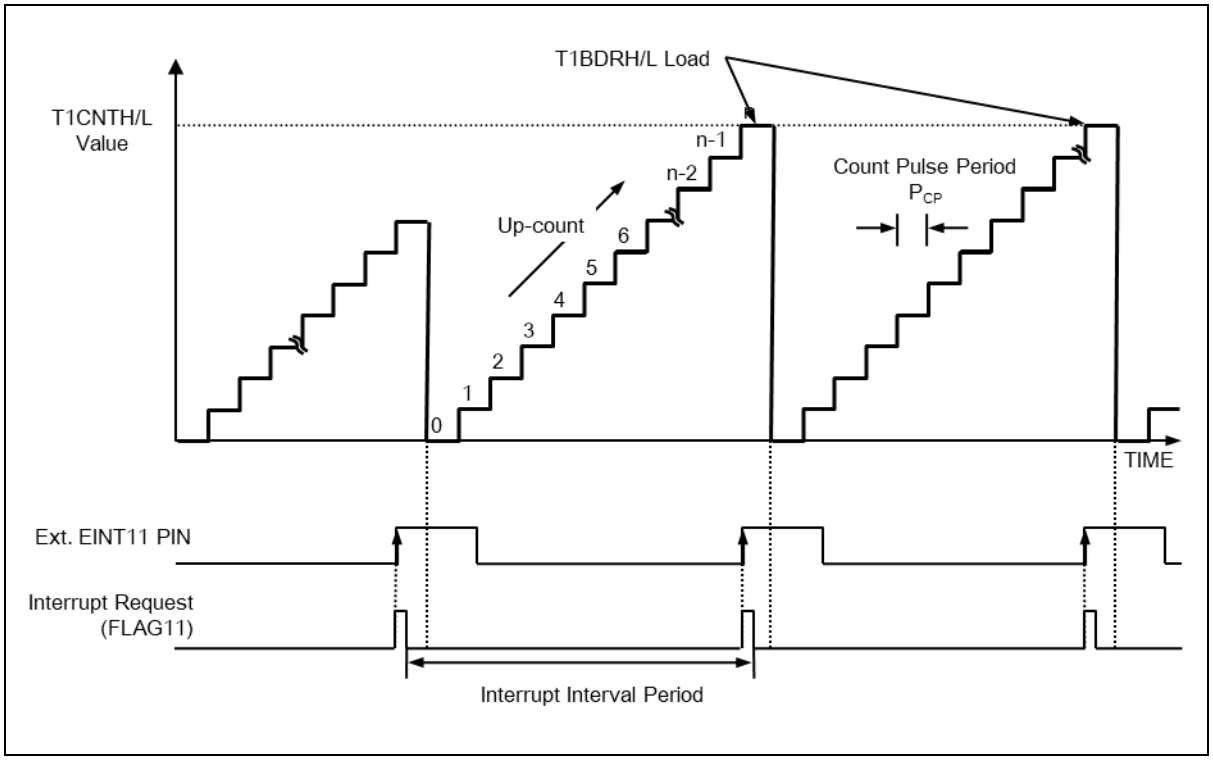


Figure 31. Input Capture Mode Operation of TIMER 1

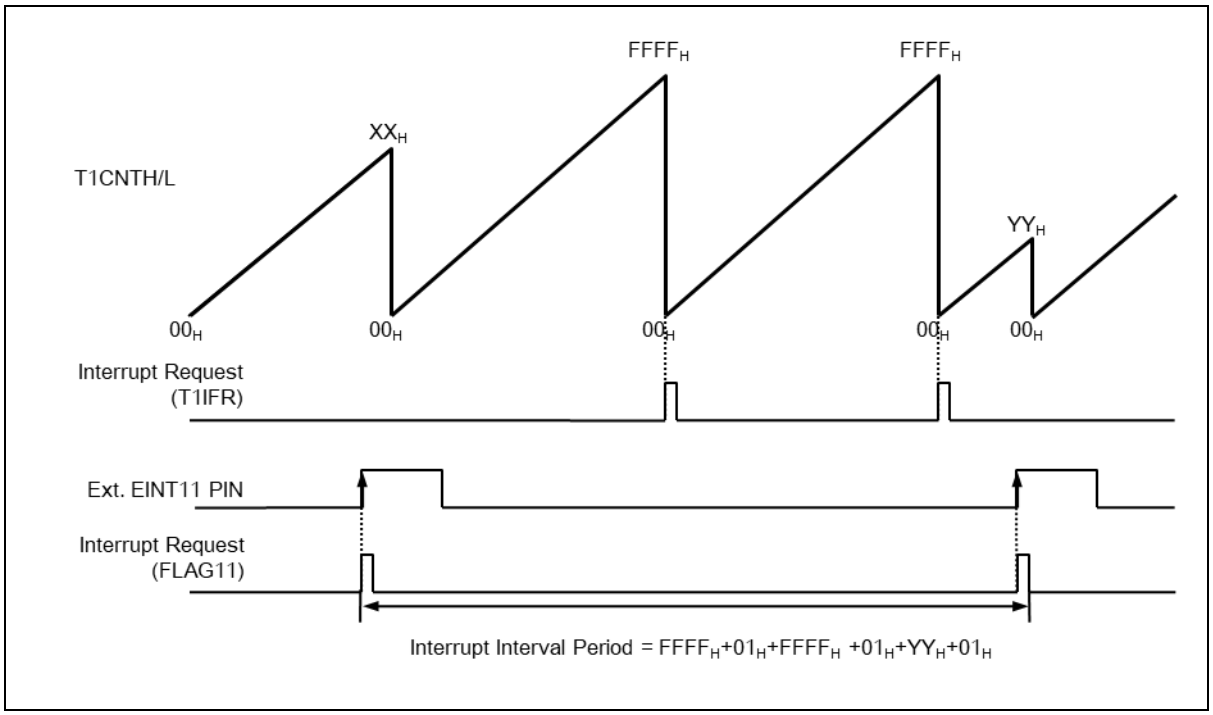
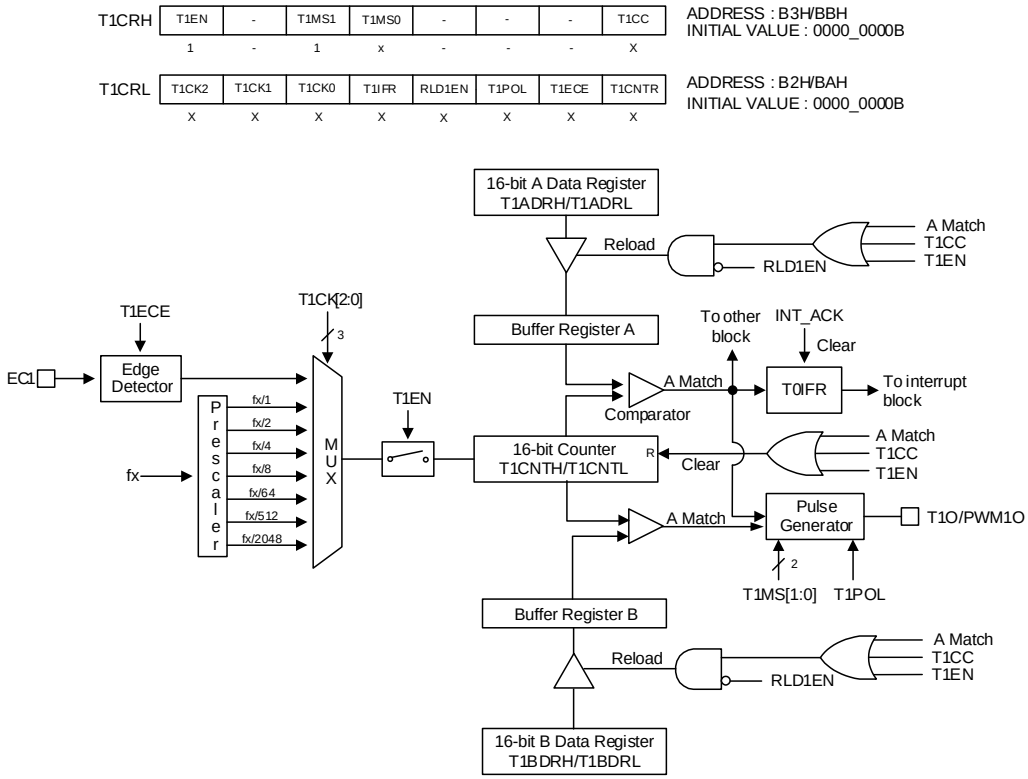


Figure 32. Express Timer Overflow in Capture Mode

10.2.3 16-bit PPG mode

TIMER 1 has a PPG (Programmable Pulse Generation) function. In PPG mode, T1O/PWM1O pin outputs up to 16-bit resolution PWM output.

For this function, T1O/PWM1O pin must be configured as a PWM output by setting P1FSRH[1:0](T1) to '01'. Period of the PWM output is determined by T1ADRH/T1ADRL, and duty of the PWM output is determined by T1BDRH/T1BDRL.



NOTES:

1. T1EN is automatically cleared to logic '0' after one pulse is generated at a PPG one-shot mode.
2. RLD1EN bit must be '0b' when T1EN bit is changed from '0b' to '1b'.

Figure 33. 16-bit PPG Mode of TIMER 1

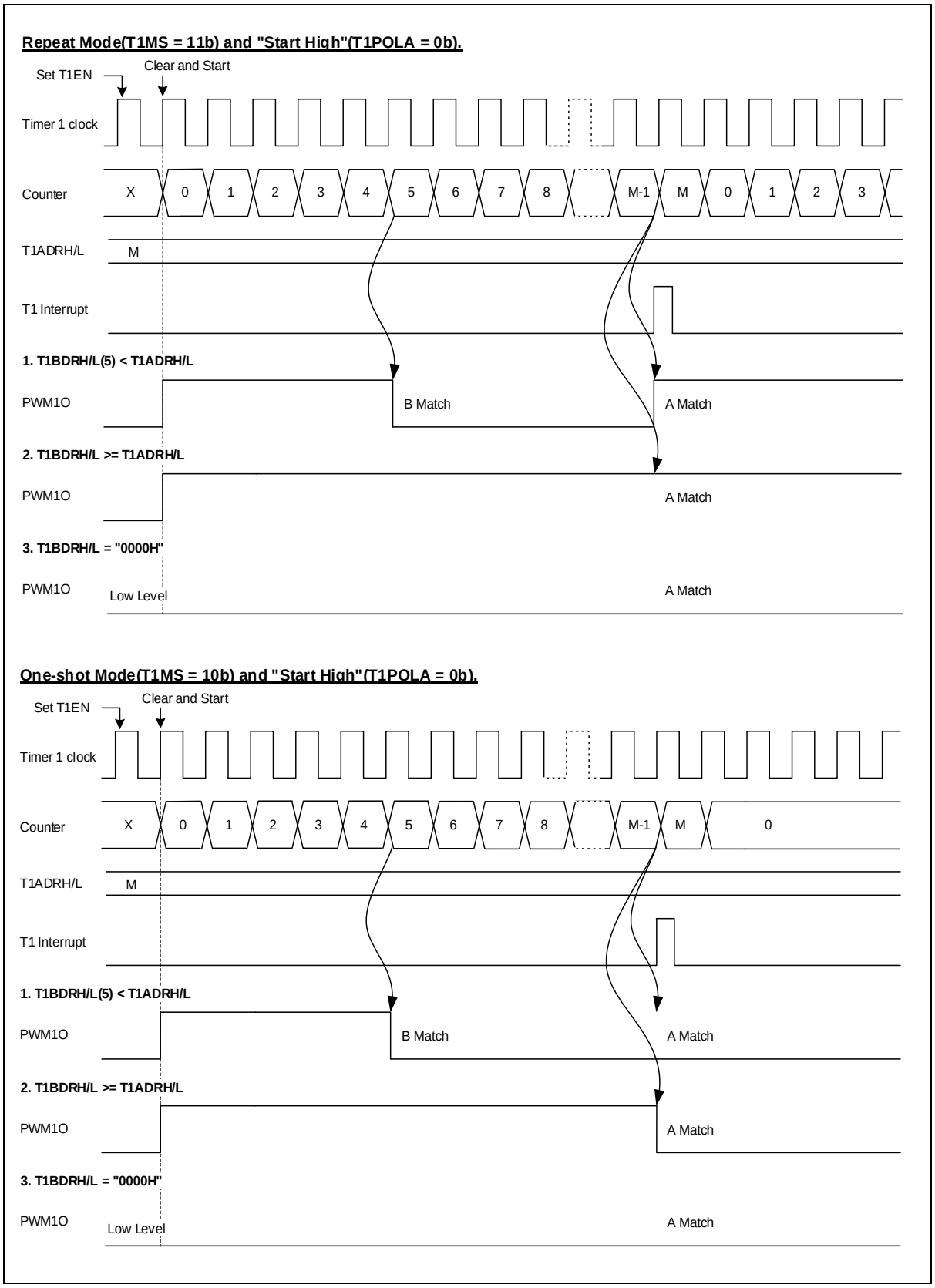


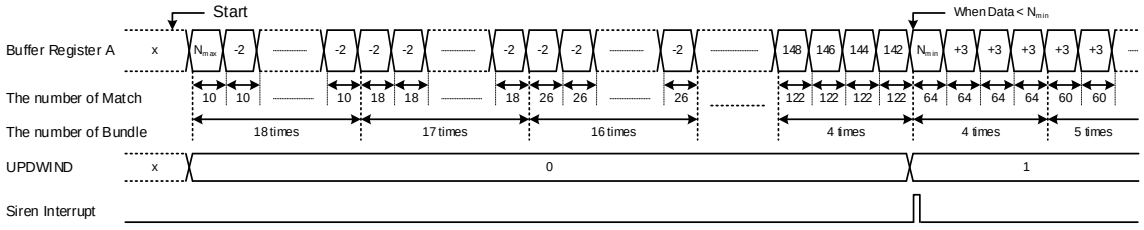
Figure 34. 16-bit PPG Mode Timing Chart of TIMER 1

10.2.4 Siren signal timing chart

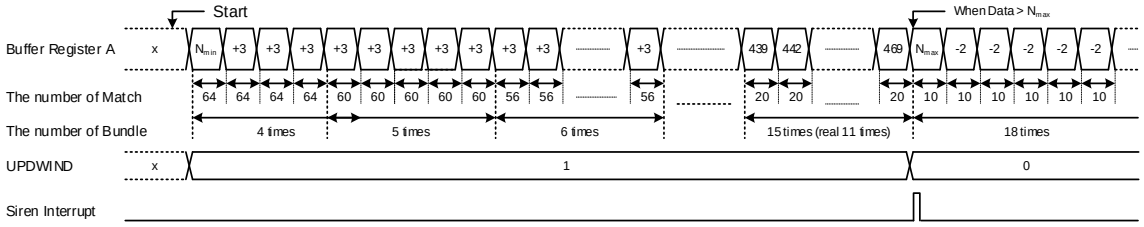
Value of the siren related registers are as follows:

- MAXDR: N_{max}
- MINDR: N_{min}
- DWMAT: 10, DWBNDL: 18, DWDECD: 2, DWINCM: 8
- UPMAT: 64, UPBNDL: 4, UPINCD: 3, UPDECM: 4

1. On down data (up frequency) with UPDW = 0



2. On up data (down frequency) with UPDW = 1

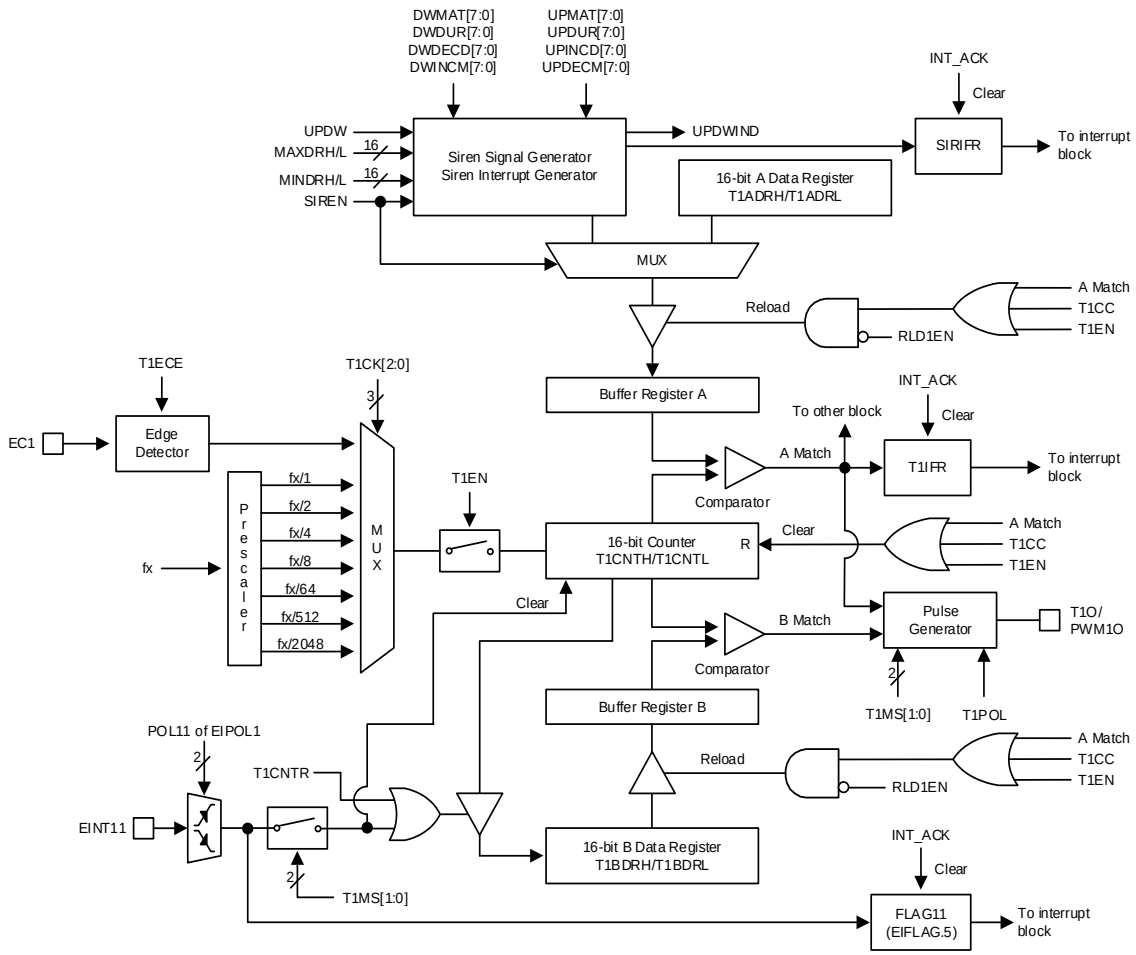


NOTES:

1. Where N_{max} = 470 and N_{min} = 142.
2. The match times and bundle times in the siren generator is equal to or greater than 1.

Figure 35. Siren Signal Timing Chart

10.2.5 Block diagram



NOTES:

1. T1EN is automatically cleared to logic ‘0’ after one pulse is generated at a PPG one-shot mode.
2. RLD1EN bit must be ‘0b’ when T1EN bit is changed from ‘0b’ to ‘1b’.

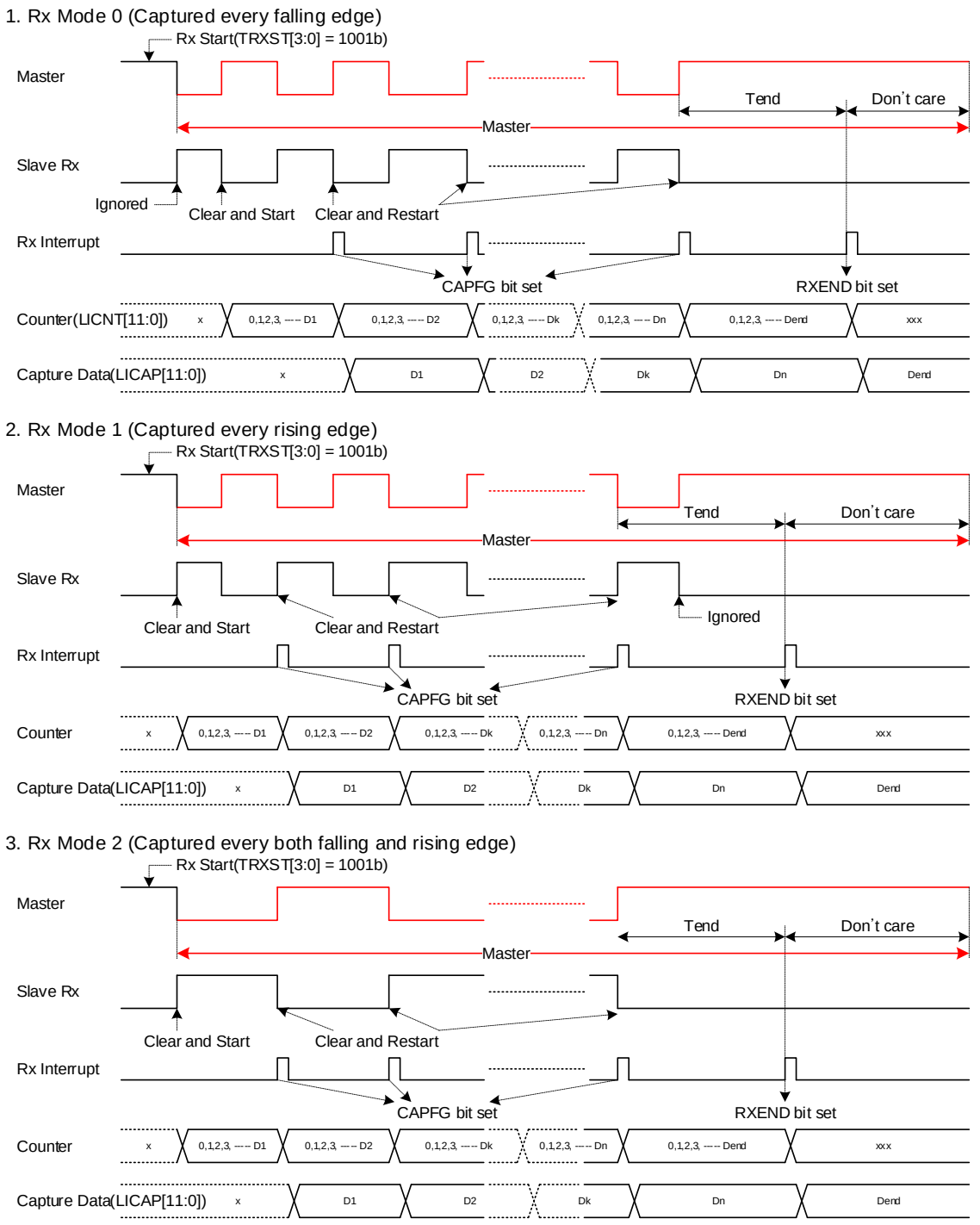
Figure 36. 16-bit Timer 1 in Block Diagram

11 Line interface

The line Interface has two operating modes:

- Receive Mode (RX Types 0~2)
- Transmit Mode (TX Mode 0~4)

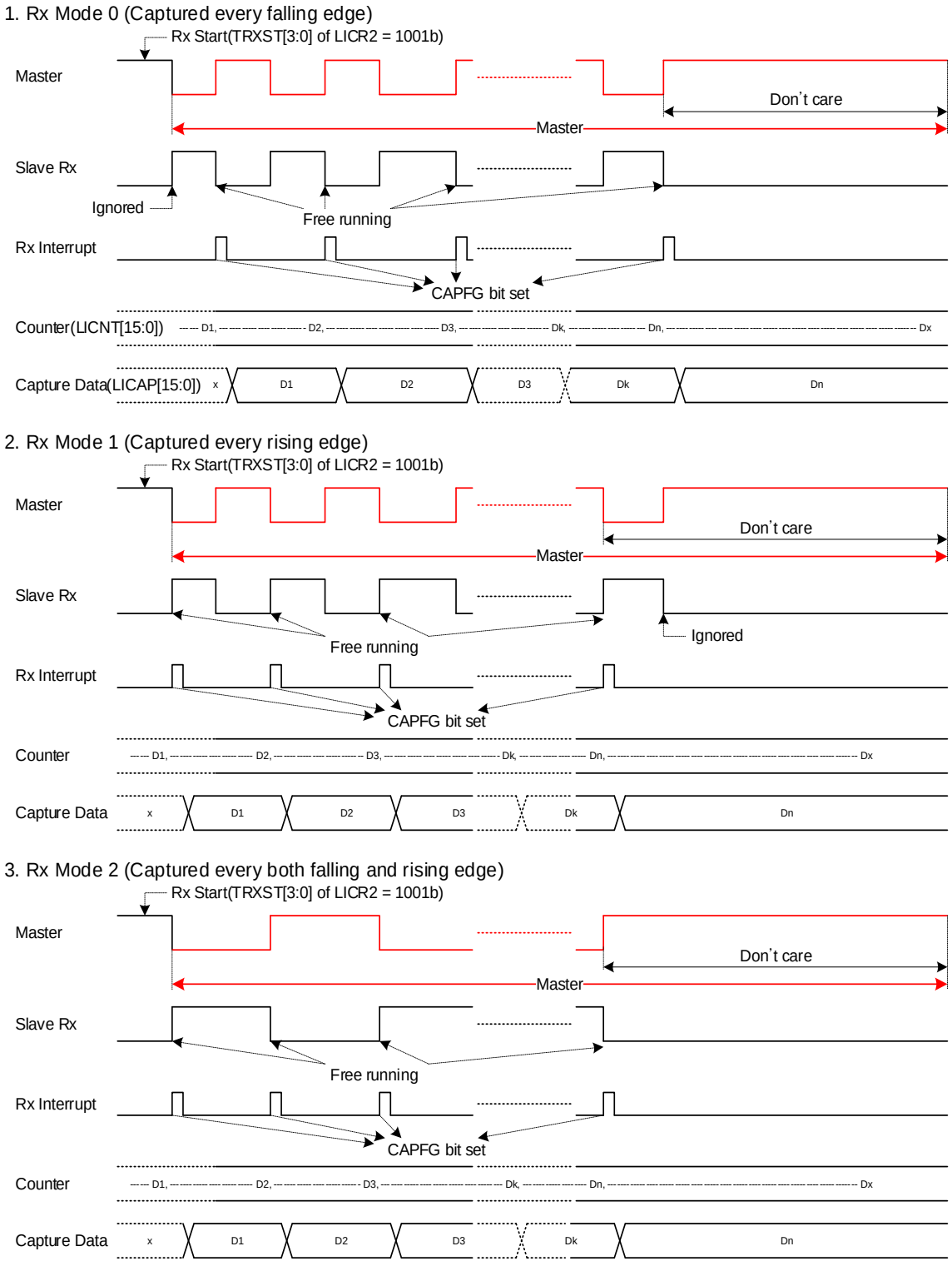
11.1 Line interface timing chart



NOTES:

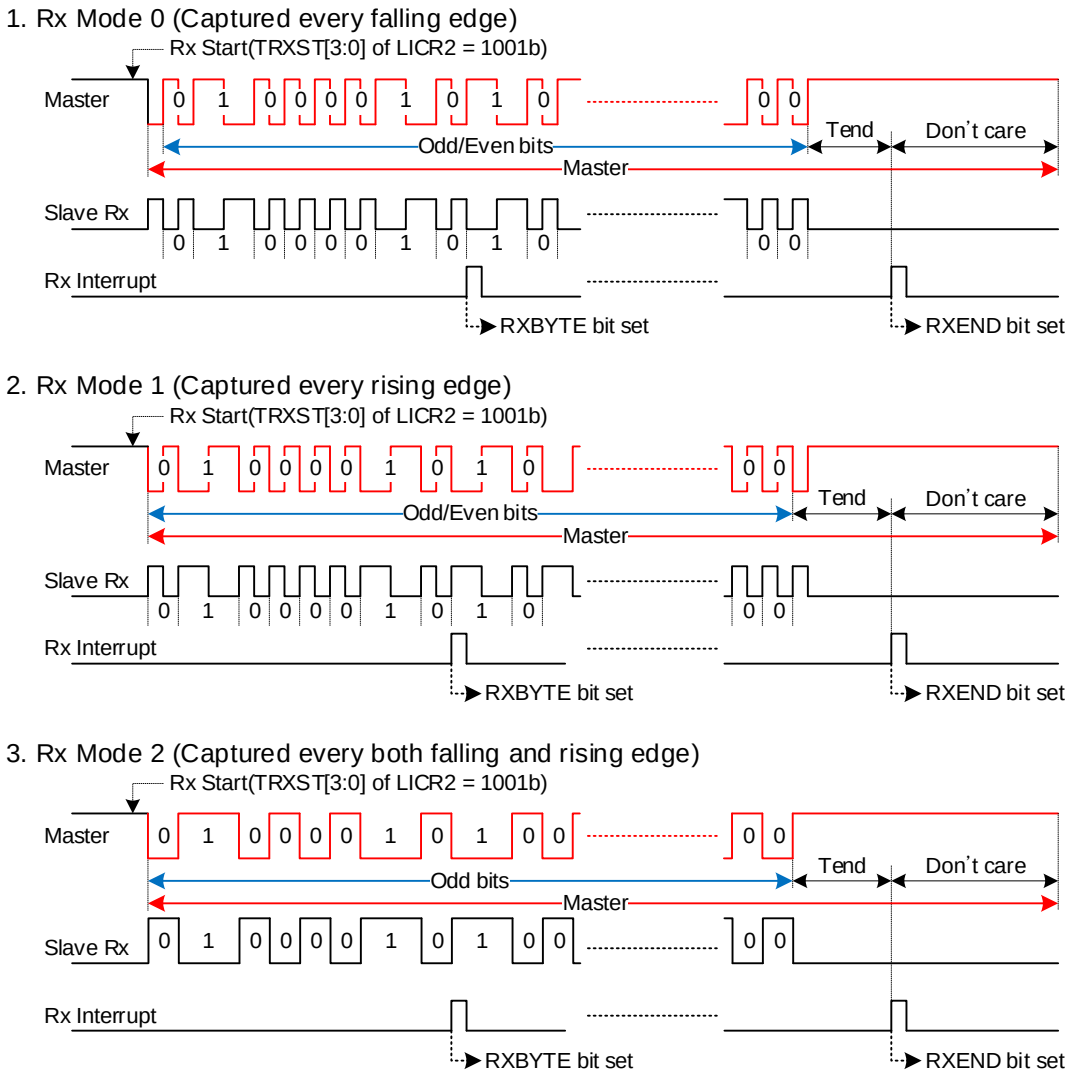
1. Rx end: Tend ≥ TENDR
2. The slave Tx is always low level during Rx modes.
3. The TENDR register should be greater than or equal to 0x000A.

Figure 37. Rx Type 0 Timing Chart (Counter clear/restart at valid edge)



NOTE: The slave Tx is always low level during Rx modes.

Figure 38. Rx Type 1 Timing Chart (Counter free running)



NOTES:

1. The slave Tx is always low level during Rx modes.
2. Each value for comparison should be spaced at least 5 or higher.

Figure 39. Rx Type 2 Timing Chart (Receive bits by H/W)

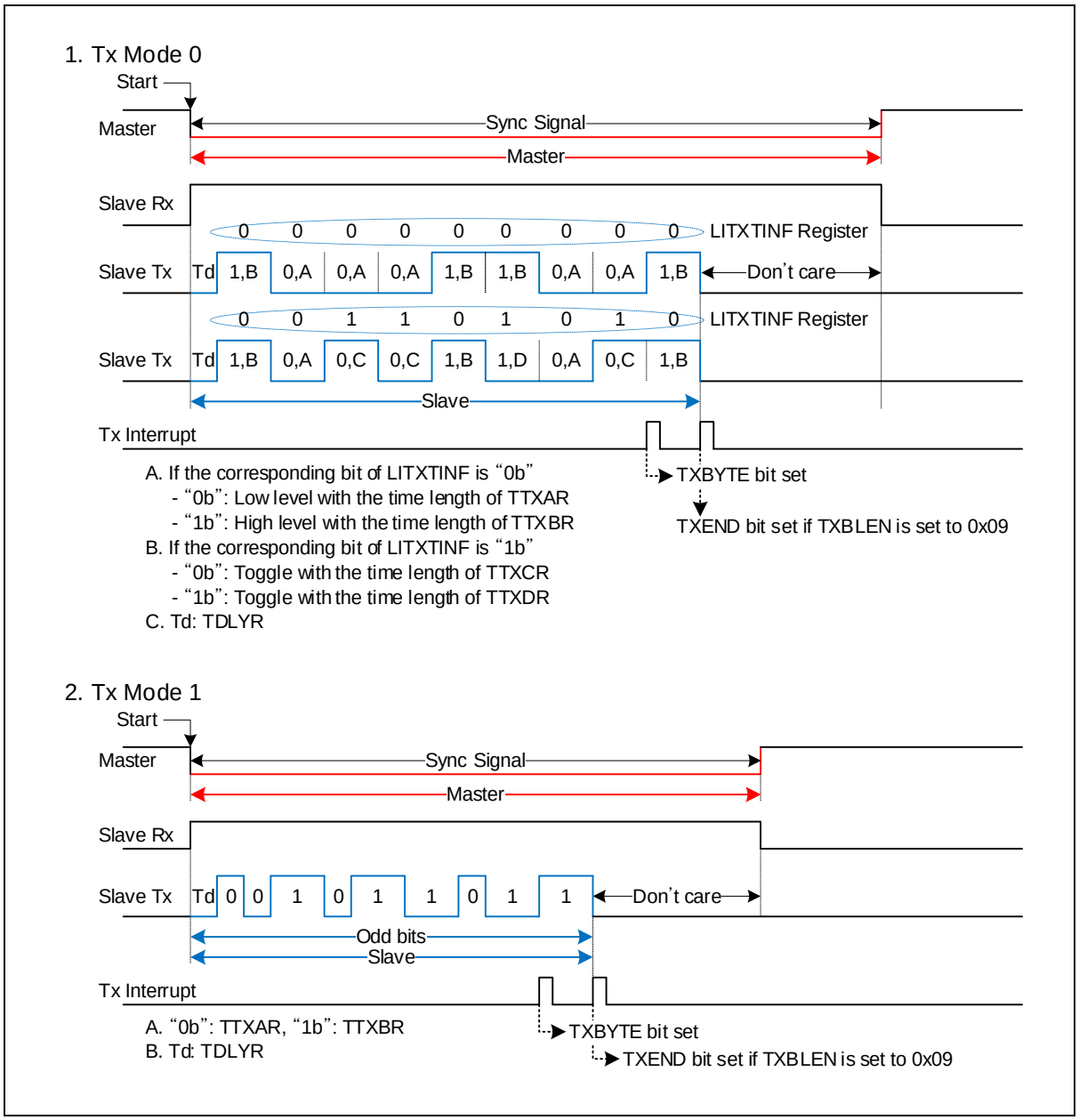
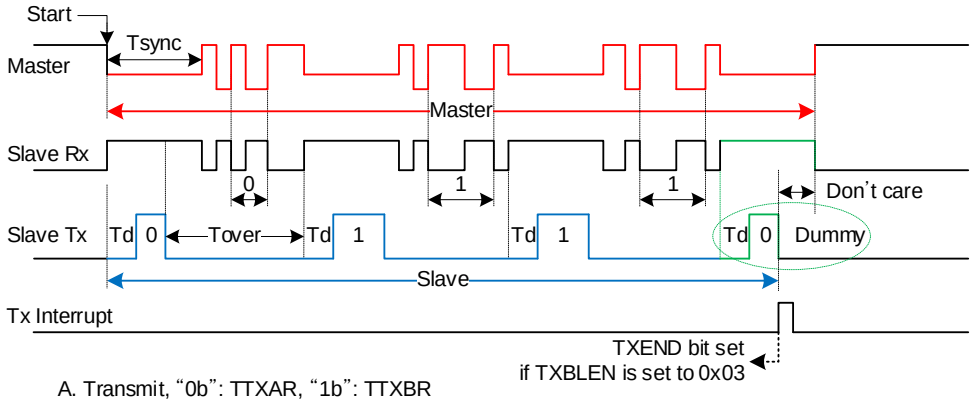


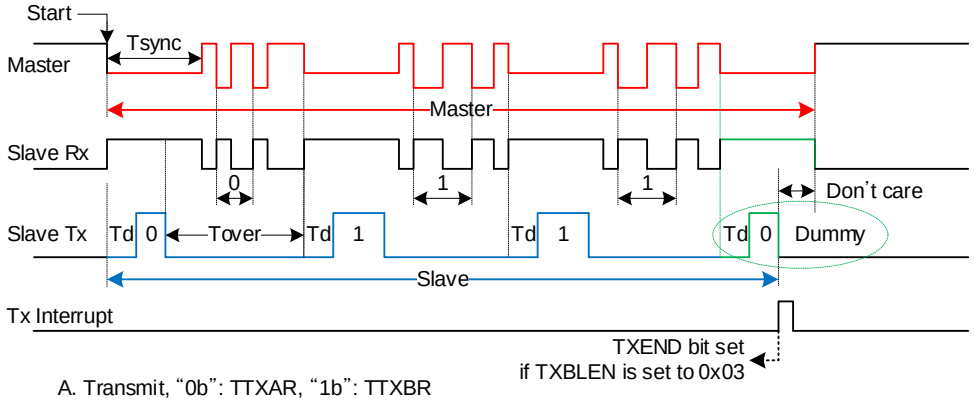
Figure 40. Tx Modes Timing Chart (Mode: 0, 1)

3. Tx Mode 2 (Check response at falling edge)



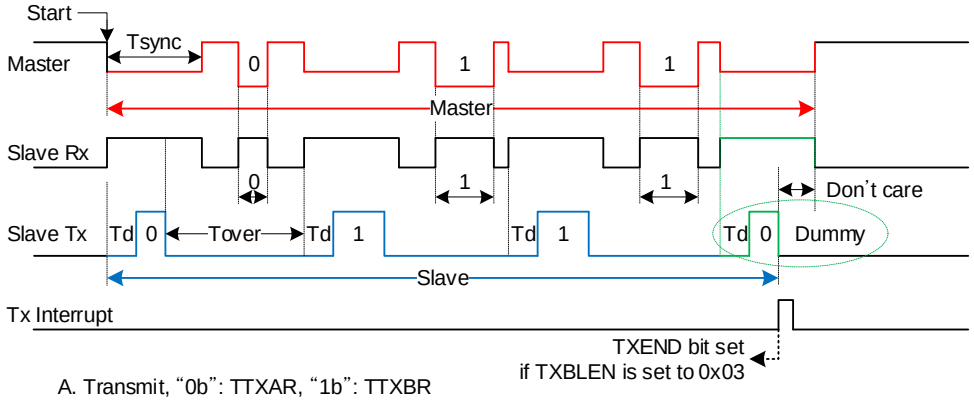
A. Transmit, "0b": TTXAR, "1b": TTXBR
B. Response, TMINR < "0b" ≤ TTXRR, TTXRR < "1b" ≤ TMAXR
C. Td: TDLYR
D. Tx error: Tbit ≤ TMINR, Tbit > TMAXR, Tover ≥ TENDR, Tx bit ≠ Response bit

4. Tx Mode 3 (Check response at rising edge)



A. Transmit, "0b": TTXAR, "1b": TTXBR
B. Response, TMINR < "0b" ≤ TTXRR, TTXRR < "1b" ≤ TMAXR
C. Td: TDLYR
D. Tx error: Tbit ≤ TMINR, Tbit > TMAXR, Tover ≥ TENDR, Tx bit ≠ Response bit

5. Tx Mode 4 (Check response at both falling and rising edge)

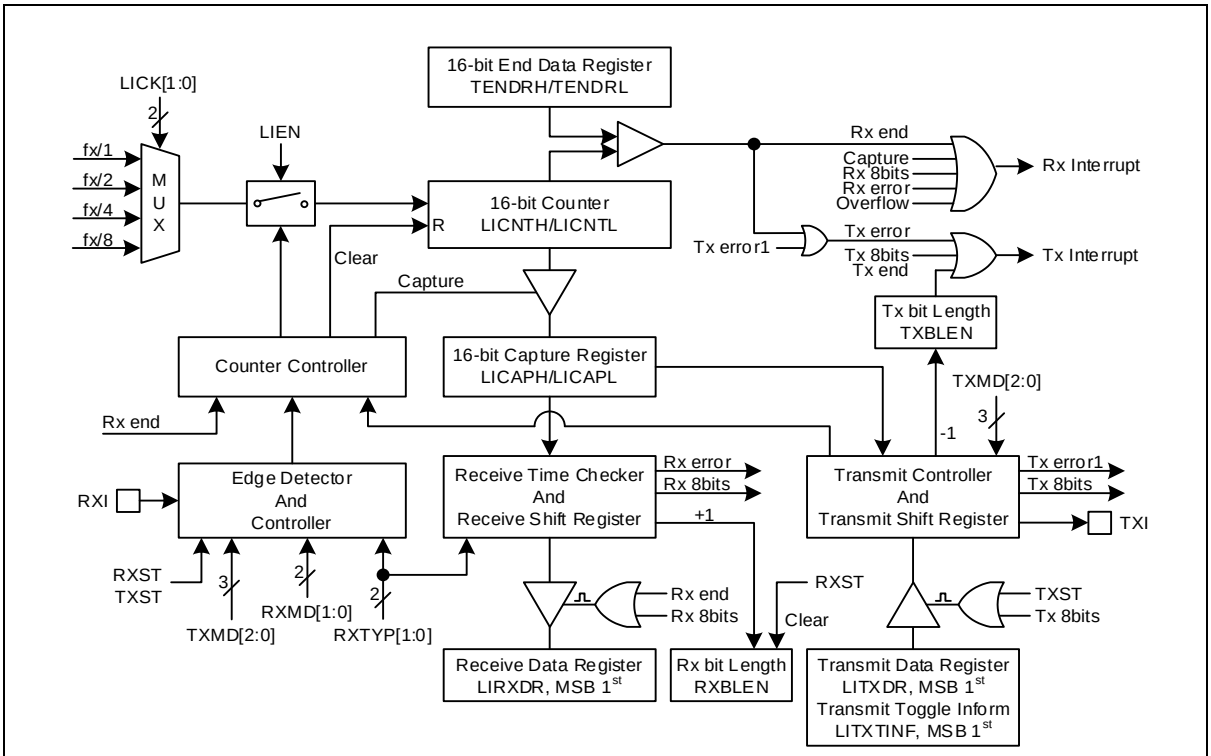


A. Transmit, "0b": TTXAR, "1b": TTXBR
B. Response, TMINR < "0b" ≤ TTXRR, TTXRR < "1b" ≤ TMAXR
C. Td: TDLYR
D. Tx error: Tbit ≤ TMINR, Tbit > TMAXR, Tover ≥ TENDR, Tx bit ≠ Response bit

NOTE: Each value for comparison should be spaced at least 5 or higher.

Figure 41. Tx Modes Timing Chart (Mode: 2, 3, and 4)

11.2 Block diagram



NOTES:

1. The TENDR register value should be greater than the TMAXR register value.
2. The transmission and reception is always MSB 1st.
3. All time calculation registers are calculated by n+1.

Figure 42. Line Interface Block Diagram

12 10-bit ADC

Analog-to-Digital converter (A/D) allows conversion of an analog input signal to corresponding 10-bit digital value. An A/D module has eleven analog inputs.

Output of the multiplexer is the input into the converter which generates the result through successive approximation. The A/D module has four registers which are the A/D converter control high register (ADCCRH), A/D converter control low register (ADCCRL), A/D converter data high register (ADCDRH), and A/D converter data low register (ADCDRL). The channels to be converted are selected by configuring the ADSEL[3:0]. Registers ADCDRH and ADCDRL contain the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADCDRH and ADCDRL, the A/D conversion status bit AFLAG is set to '1', and the A/D interrupt is set. During A/D conversion, AFLAG bit is read as '0'.

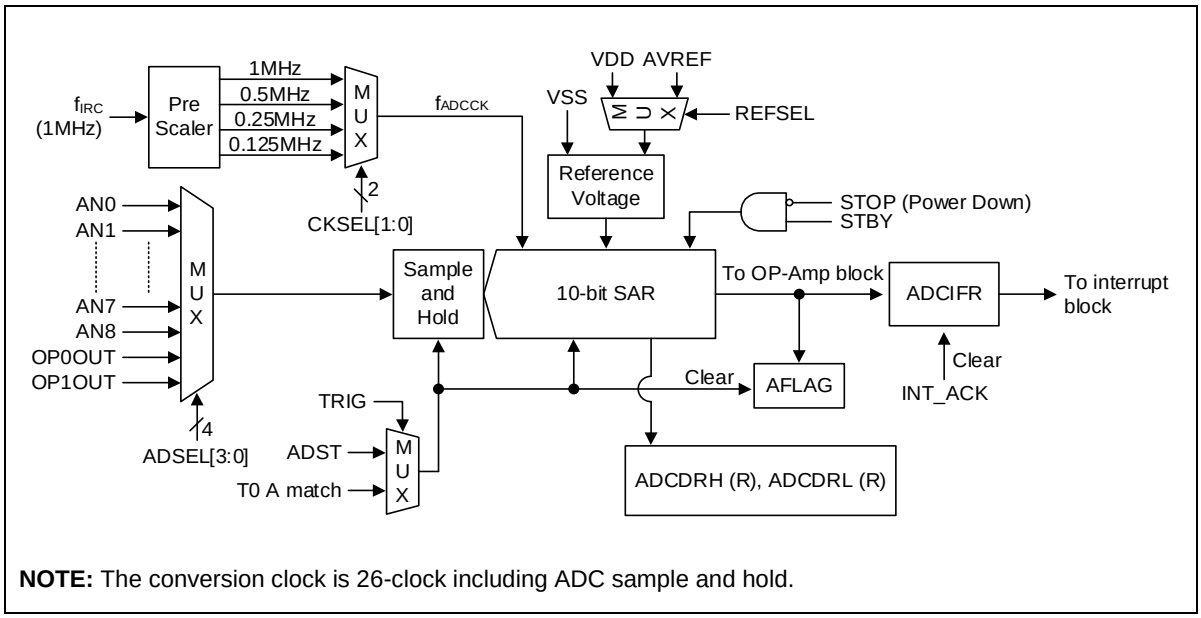
12.1 Conversion timing

The A/D conversion process requires 6 clocks to sample/hold, 2 steps (2 clock edges) to convert each bit, and 2 clocks to set up A/D conversion. Therefore, total of 28 clocks are required to complete a 10-bit conversion: Conversion clock with a 1MHz ADC clock frequency, one clock cycle is 1 us. Each bit conversion requires 2 clocks, the conversion rate is calculated as follows:

"6 clocks for S&H" + "2 clocks/bit × 10 bits" + set-up time = 28 clocks,

28 clock × 1 us = 28 us at 1 MHz

12.2 Block diagram



NOTE: The conversion clock is 26-clock including ADC sample and hold.

Figure 43. 10-bit ADC Block Diagram

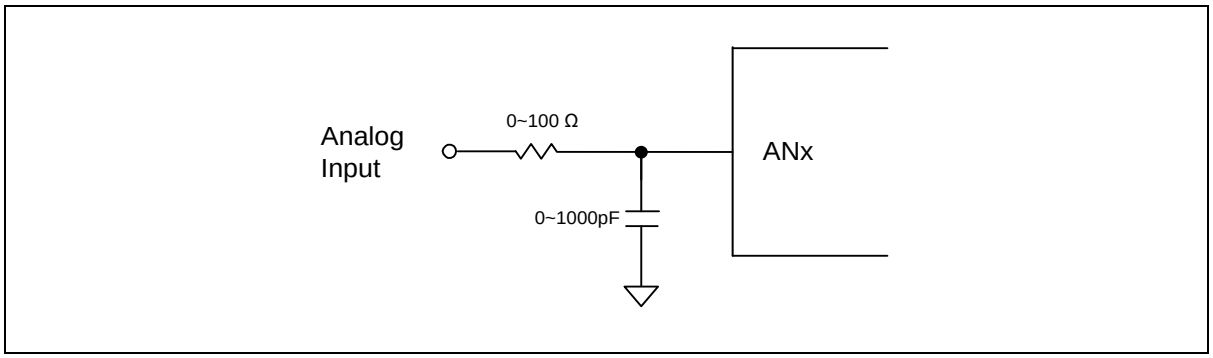


Figure 44. A/D Analog Input Pin with Capacitor

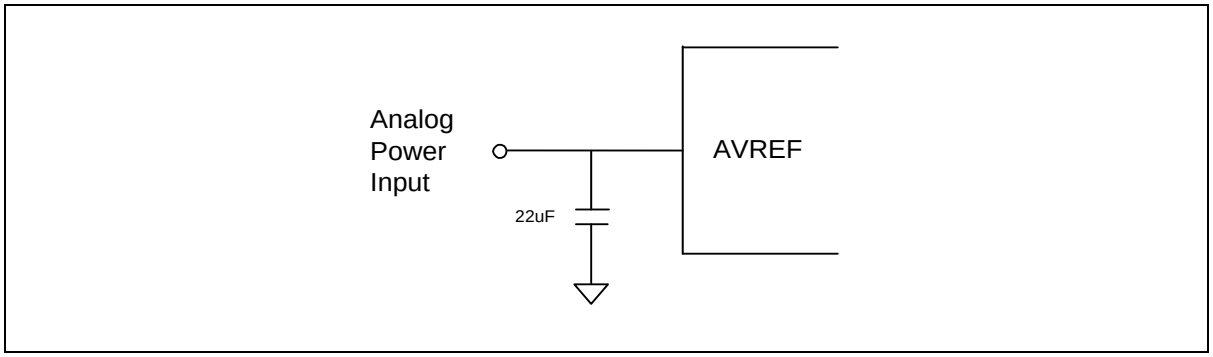


Figure 45. A/D Power (AVREF) Pin with Capacitor

12.3 ADC operation

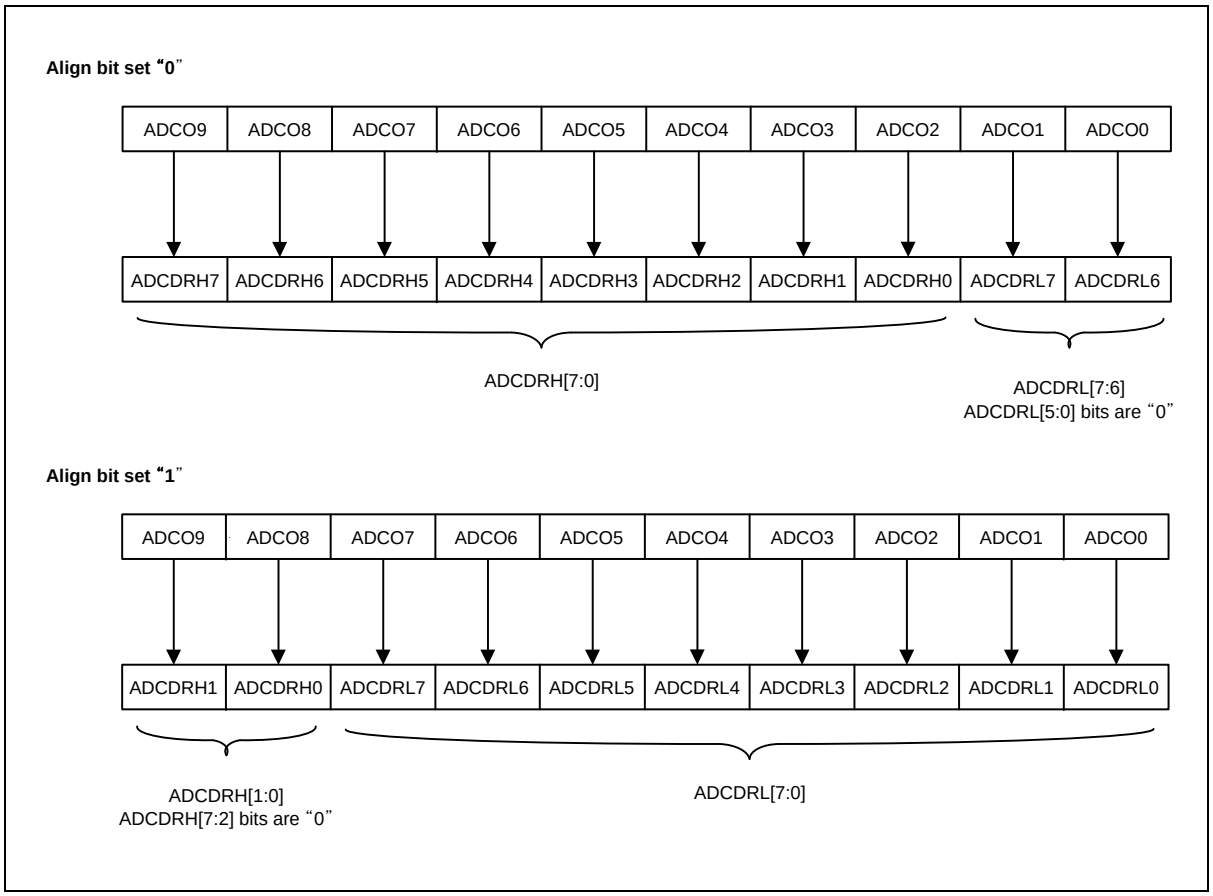


Figure 46. ADC Operation for Align Bit

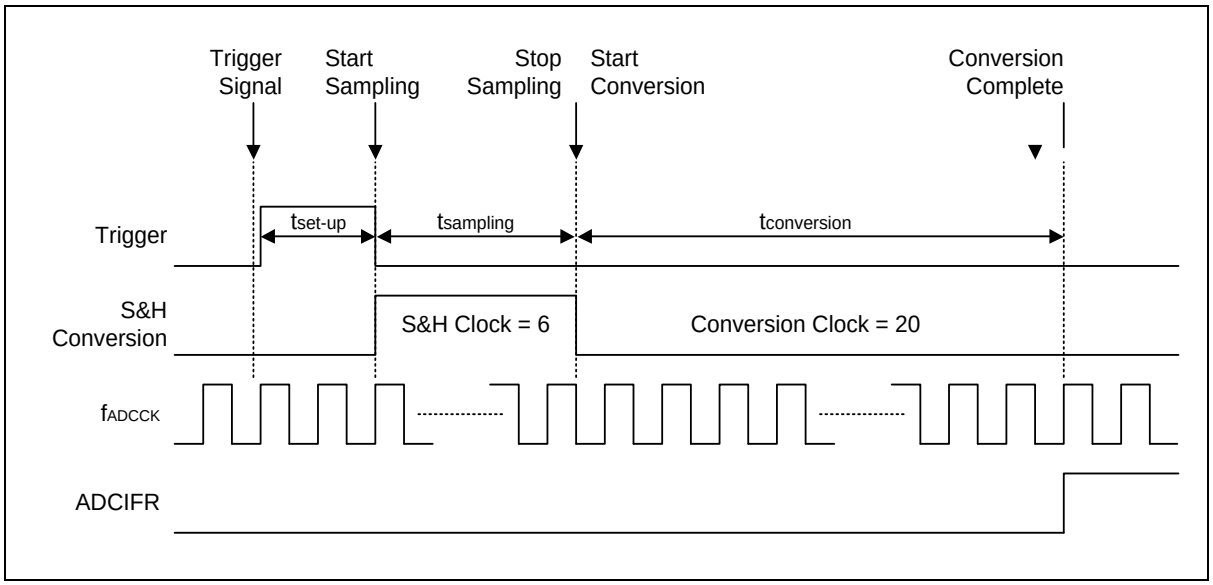


Figure 47. ADC Timing Chart

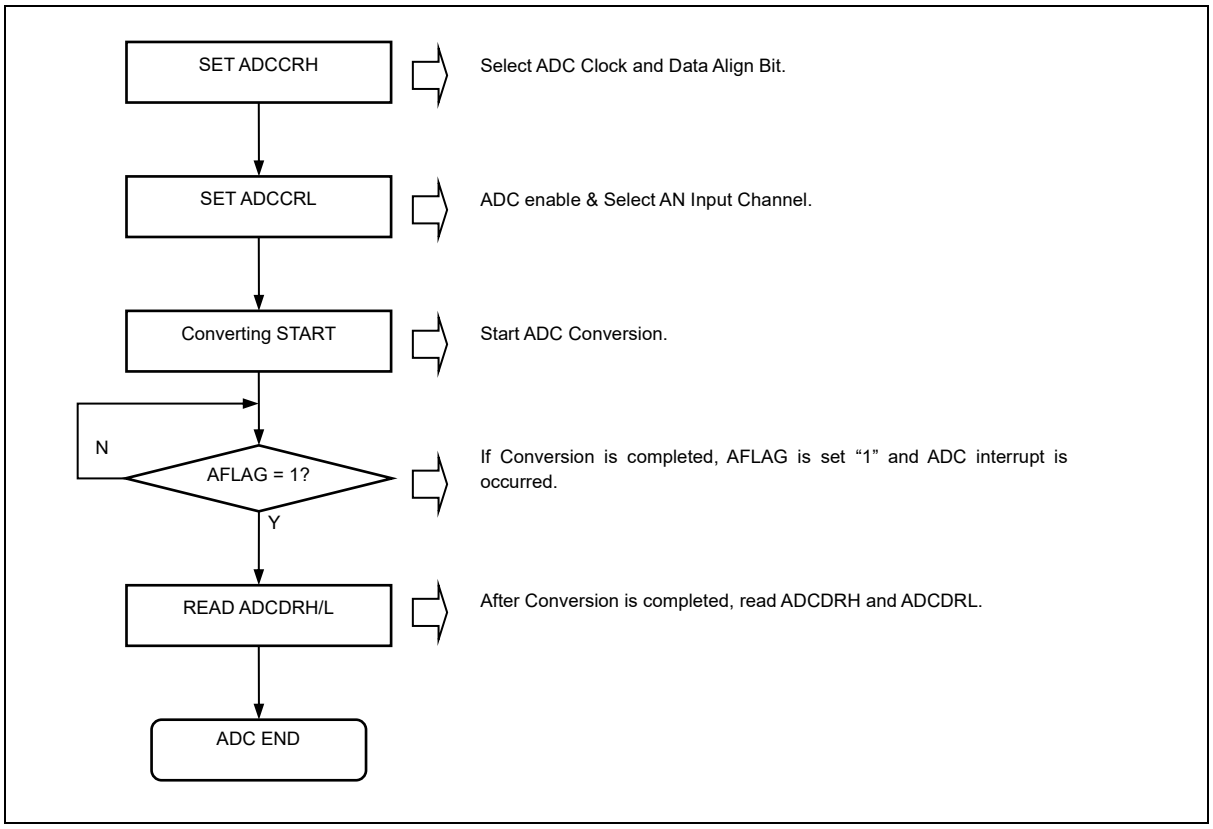
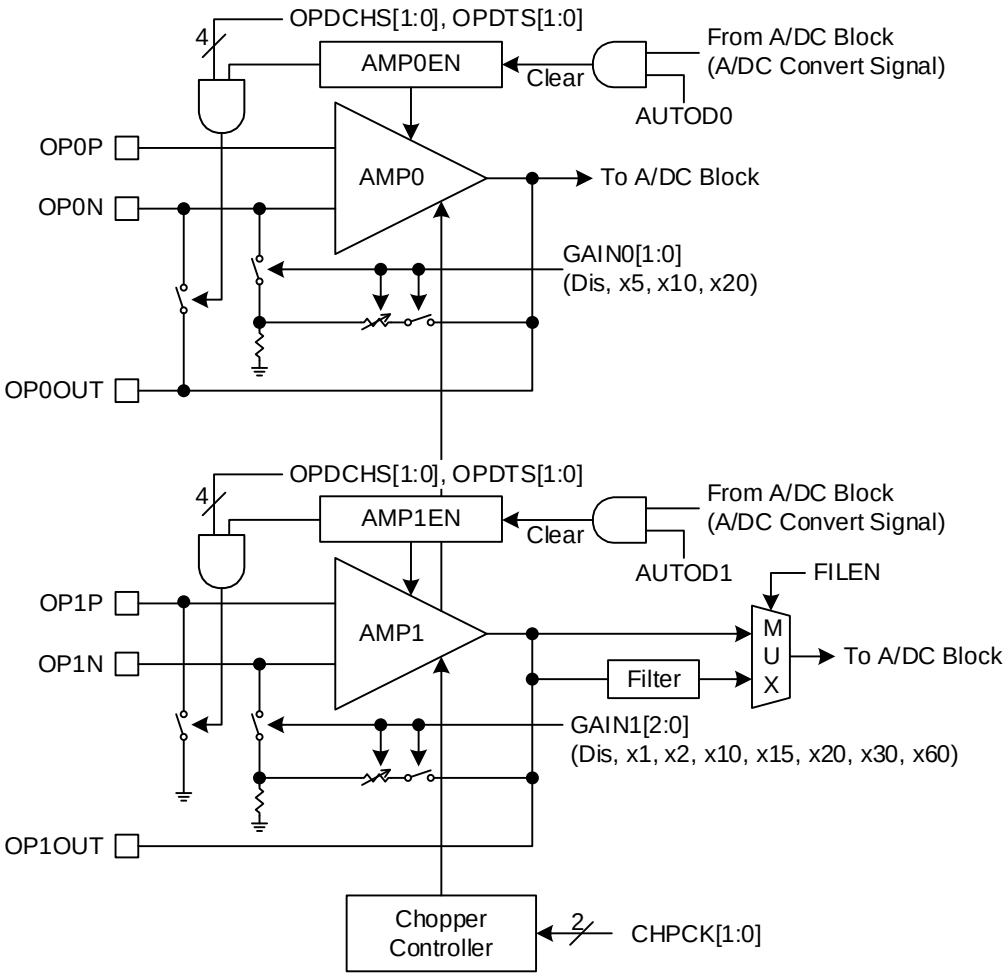


Figure 48. A/D Converter Operation Flow

13 Operational amplifier

There is operational amplifier (OP-AMP) two channel in A96L523. The operational amplifier (OP-AMP) has three registers which are OP-AMP control register 0(AMPCR0) and OP-AMP control register 1(AMPCR1) and Chopper control register (CHPCR).

13.1 Block diagram



NOTE: The feedback resistors for gain on each amp are disconnected during one or more of amp and gain is disabled.

Figure 49. Operational Amplifier Block Diagram

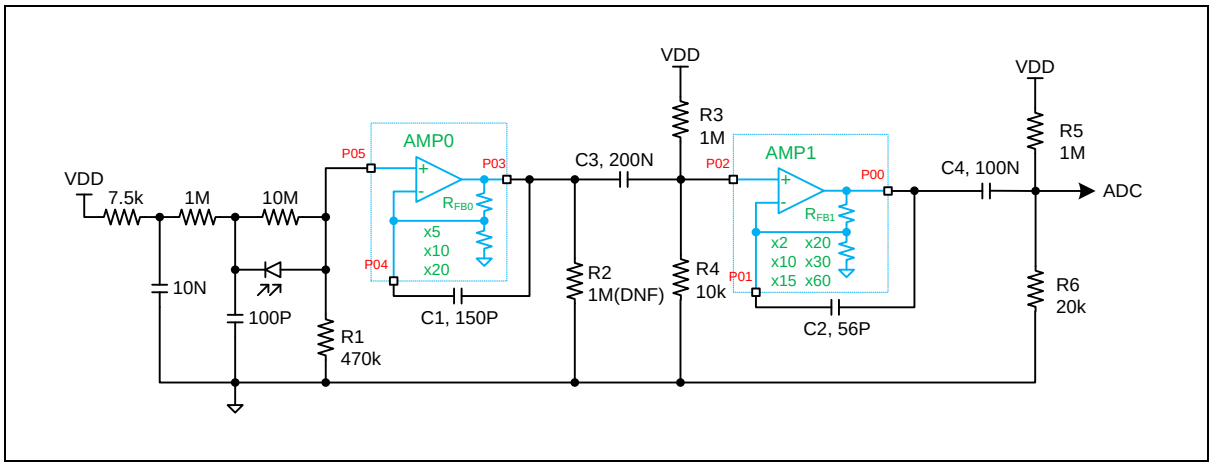


Figure 50. Recommend circuit for internal gain.

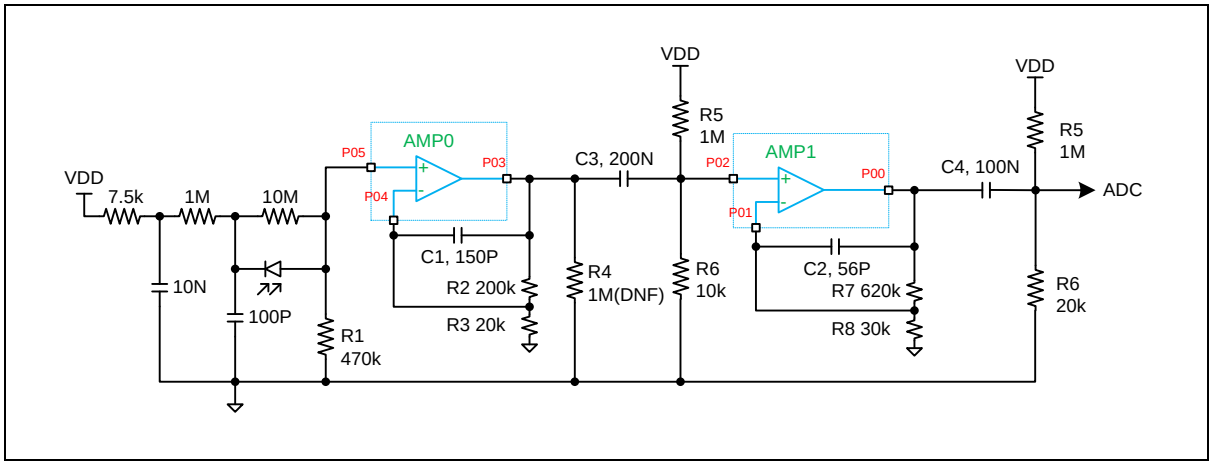


Figure 51. Recommend circuit for internal gain.

14 USART (UART + SPI)

The USART is an acronym of UART, USART and SPI, A96L523 has one USART function block. USART consists of USART control register1/2/3/4, USART status register, USART baud-rate generation register and USART data register.

The operation mode is selected by the operation mode of USART selection bits (USTMS[1:0]). There are three operating modes as shown below:

- Asynchronous mode (UART)
- Synchronous mode (USART)
- SPI mode

All functions are explained with USART as followings.

14.1 USART UART mode

The Universal Asynchronous Serial Receiver and Transmitter (UART) is a highly flexible serial communication device. The main features are listed below.

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Baud Rate Generator
- Supports Serial Frames with 5, 6, 7, 8, or 9 Data Bits and 1 or 2 Stop Bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data Overrun Detection
- Framing Error Detection
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete

The UART has a baud rate generator, transmitter and receiver. The baud rate generator for asynchronous operation. The Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. The write buffer allows continuous transfer of data without any delay between frames. The receiver is the most complex part of the UART module due to its clock and data recovery units. The recovery unit is used for asynchronous data reception. In addition to the recovery unit, the receiver includes a parity checker, a shift register, a two-level receive FIFO (USTDR) and control logic. The receiver supports the same frame formats as the transmitter and can detect frame error, data overrun and parity errors.

14.2 UART block diagram

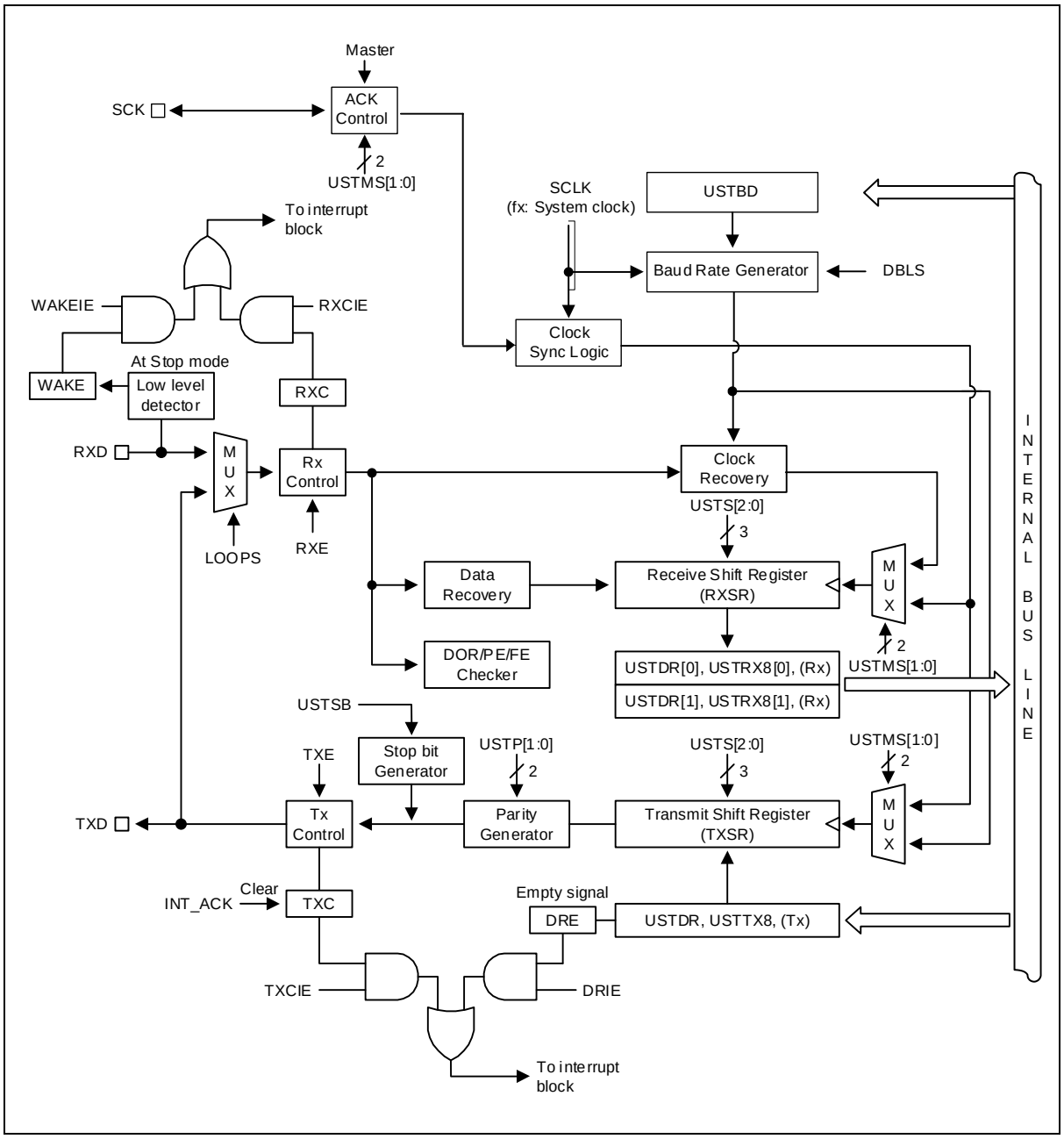


Figure 52. UART Block Diagram

14.3 Clock generation

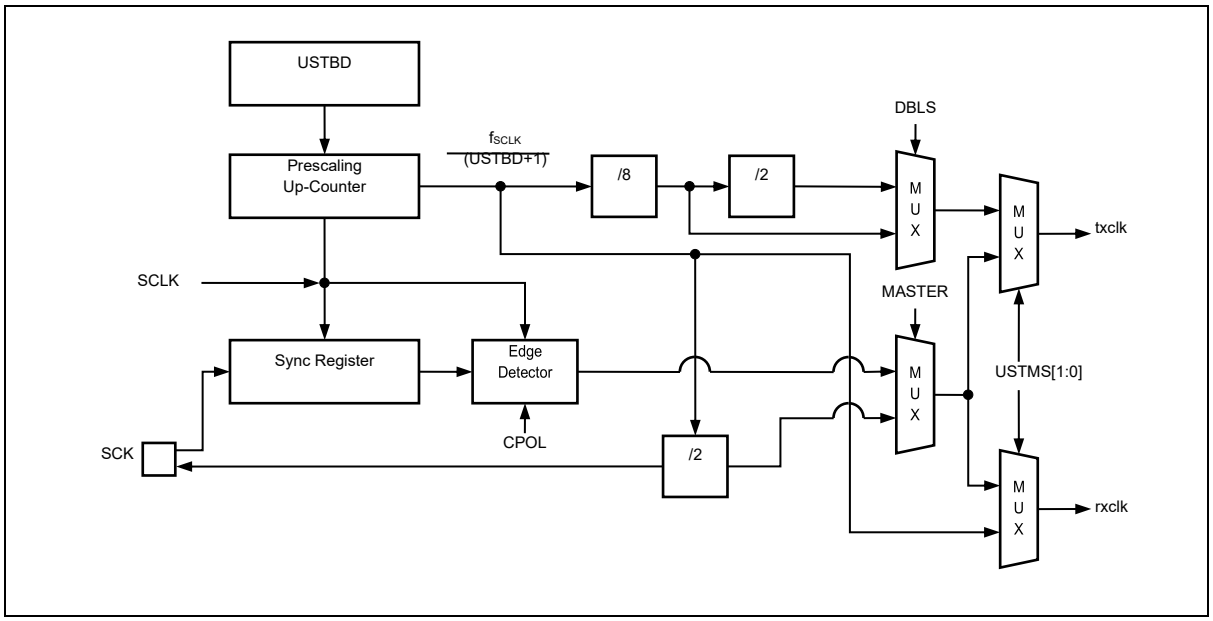


Figure 53. Clock Generation Block Diagram

The clock generation logic generates the base clock for the transmitter and receiver. The USART supports four modes of clock operation and those are normal asynchronous, double speed asynchronous, master synchronous and slave synchronous mode. The clock generation scheme for master SPI and slave SPI mode is the same as master synchronous and slave synchronous operation mode.

The USTMS[1:0] bits in USTCR1 register selects asynchronous or synchronous operation. Asynchronous double speed mode is controlled by the DBLS bit in the USTCR2 register. The MASTER bit in USTCR3 register controls whether the clock source is internal (master mode, output pin) or external (slave mode, input pin). The SCK pin is active only when the USART operates in synchronous or SPI mode.

Following table shows equations for calculating the baud rate (in bps).

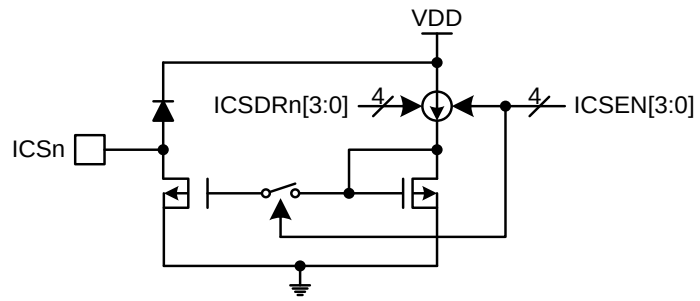
Table 9. Equations for Calculating Baud Rate Register Setting

Operating Mode	Equation for Calculating Baud Rate
Normal Mode(DBLS=0)	$\text{Baud Rate} = \frac{\text{fx}}{16(\text{USTBD} + 1)}$
Double Speed Mode(DBLS=1)	$\text{Baud Rate} = \frac{\text{fx}}{8(\text{USTBD} + 1)}$
Synchronous or SPI Master Mode	$\text{Baud Rate} = \frac{\text{fx}}{2(\text{USI0BD} + 1)}$

15 Constant sink current generator

Constant Sink Current Generator can provide constant current while I_{CS} voltage ranges from 1.8V to 3.6V. The constant current value is controlled by configuring the ICSDR0/ICSDR1 registers, and the sink current value is between 50mA and 290mA.

15.1 Block diagram



NOTE: If the sink current generator of an ICSn pin is disabled by the ICSCR[3:0] bits, the corresponding ICSn pin is high and the current flowing is zero.

Figure 54. Constant Sink Current Generator Block Diagram (Where n = 0 and 1)

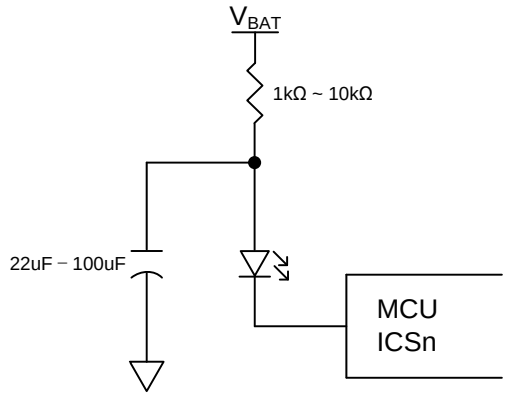


Figure 55. Constant Sink Current Generator Pin with Capacitor

16 FLASH CRC/checksum generator

The Flash CRC (Cyclic Redundancy Check) generator is used to get a 16-bit CRC code from Flash ROM and a generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the Flash memory integrity. The CRC generator helps compute a signature of the software during runtime, to be compared with a reference signature.

The CRC generator has following features:

- Auto CRC and User CRC Mode
- CRC Clock : f_{IRC}, $f_{IRC}/2$, $f_{IRC}/4$, $f_{IRC}/8$ and fx (System clock)
- CRC-16 polynomial: 0x8C81: X16 + X15 + X11 + X10 + X7 +1

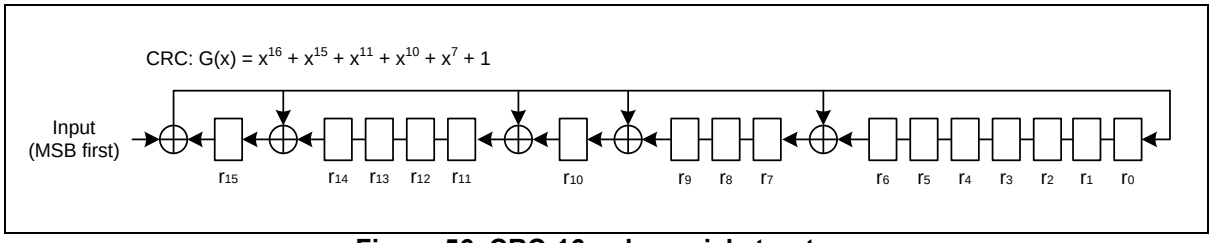


Figure 56. CRC-16 polynomial structure

16.1 Block Diagram

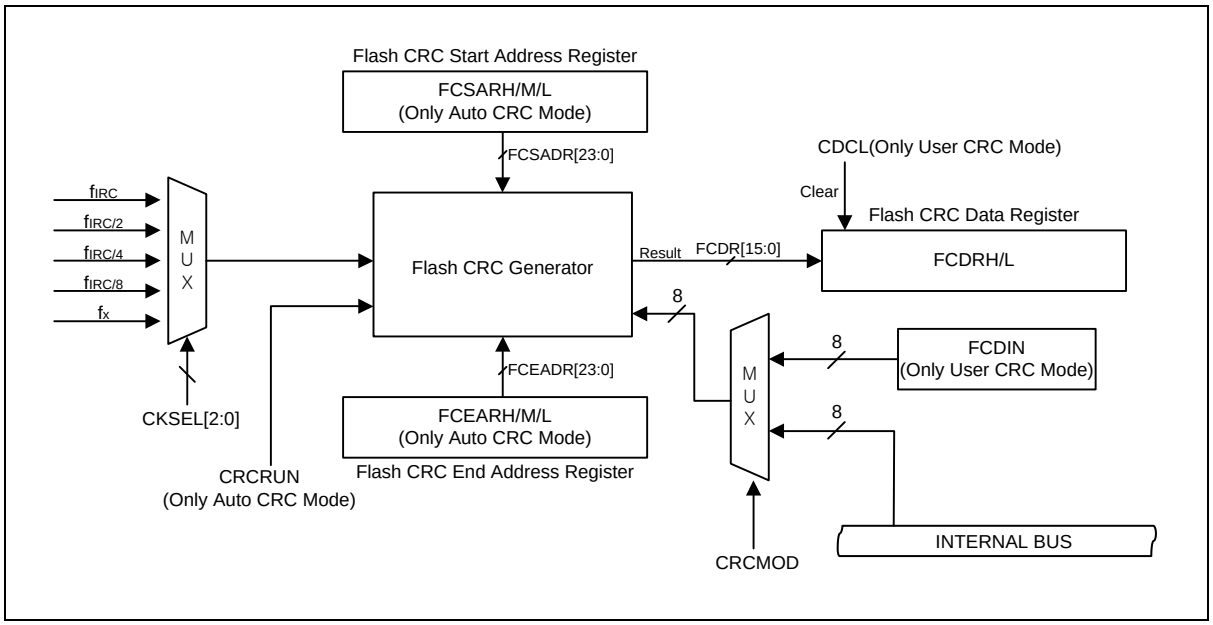


Figure 57. Flash CRC Generator Block Diagram

17 Power down operation

The A96L523 has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides two kinds of power saving functions, IDLE and STOP mode. In two modes, program is stopped.

17.1 Peripheral operation in IDLE/STOP mode

Table 10. Peripheral Operation during Power down Mode

Peripheral	IDLE Mode	STOP Mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain
Basic Interval Timer	Operates Continuously	Stop
Watch Dog Timer	Operates Continuously	Stop (Can be operated with WDTRC OSC)
Timer0/1	Operates Continuously	Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally)
ADC	Operates Continuously	Stop
USART	Operates Continuously	Stop
Siren	Operates Continuously	Stop
Line Interface	Operates Continuously	Stop
Internal OSC	Oscillation	Stop
WDTRC OSC (1KHz)	Can be operated with setting value	Can be operated with setting value
Constant Sink Current	Retain	Retain
I/O Port	Retain	Retain
Control Register	Retain	Retain
Address Data Bus	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0, EC1), External Interrupt, WDT, USART

18 Reset

Table 11 introduces hardware setting values:

Table 11. Reset State

On Chip Hardware	Initial Value
Program Counter (PC)	0000H
Accumulator	00H
Stack Pointer (SP)	07H
Peripheral Clock	On
Control Register	Refer to the Peripheral Registers

18.1 Reset source

The A96L523 has five types of reset sources. The following is the reset sources.

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset (In the case of LVREN = `0 `)
- OCD Reset

18.2 RESET block diagram

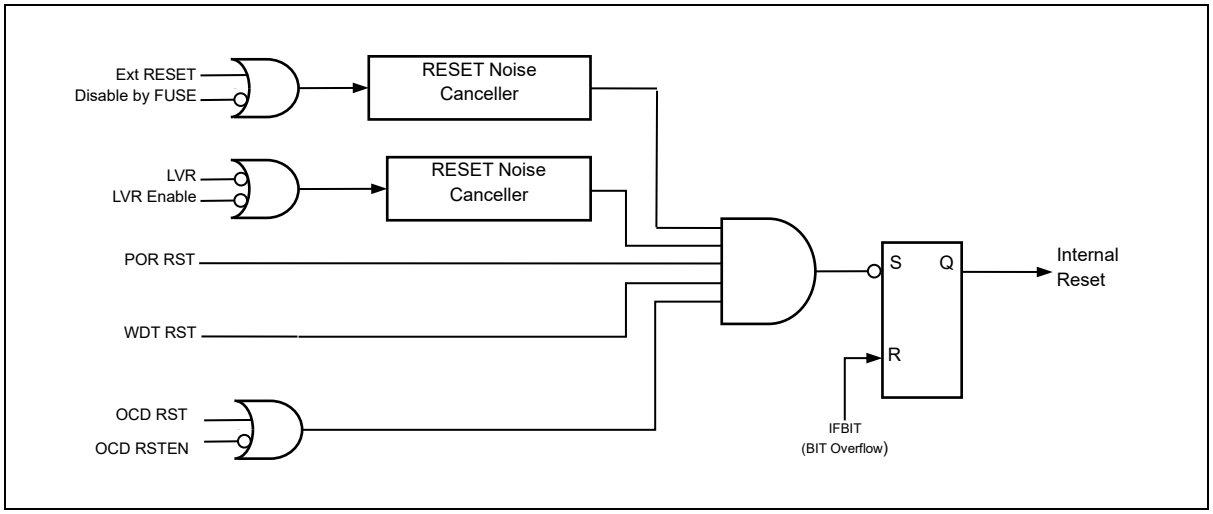


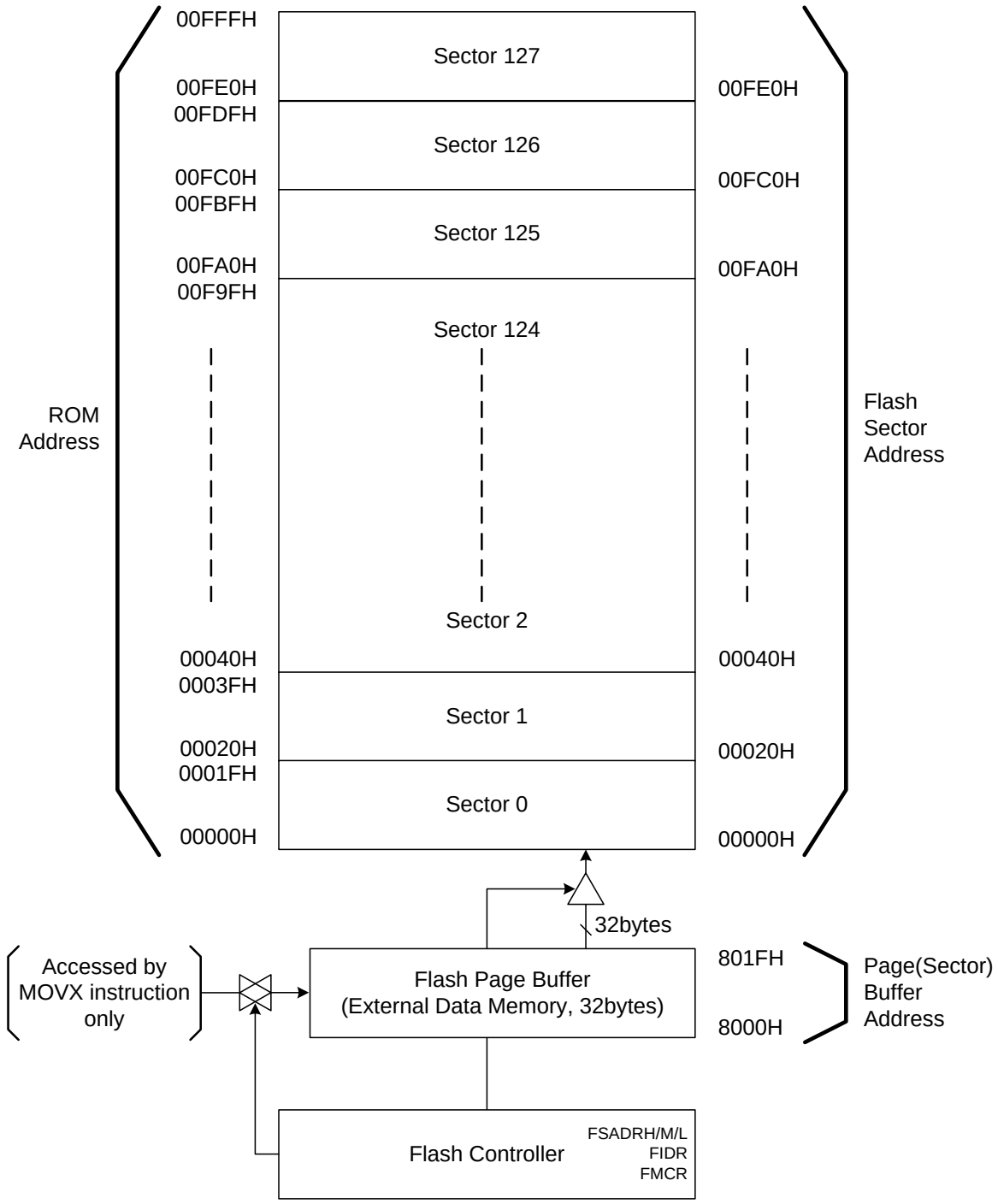
Figure 58. RESET Block Diagram

19 Flash memory

A96L523 incorporates flash memory to which a program can be written, erased, and overwritten while mounted on the board. The flash memory can be read by 'MOVC' instruction and it can be programmed in OCD, serial ISP mode or user program mode.

- Flash Size : 4Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000 program/erase cycles at typical voltage and temperature for flash memory

19.1 Flash program ROM structure



NOTES:

1. The Flash memory doesn't support byte erase mode.
2. The flash shouldn't be entered in erase/write mode during EEPROM program. So before the flash program start, the EEPROM busy bit (EEMBUSY) should be checked whether the bit is "1b"or not. If the bit is "1b", do not start flash program.

Figure 59. Flash Program ROM Structure

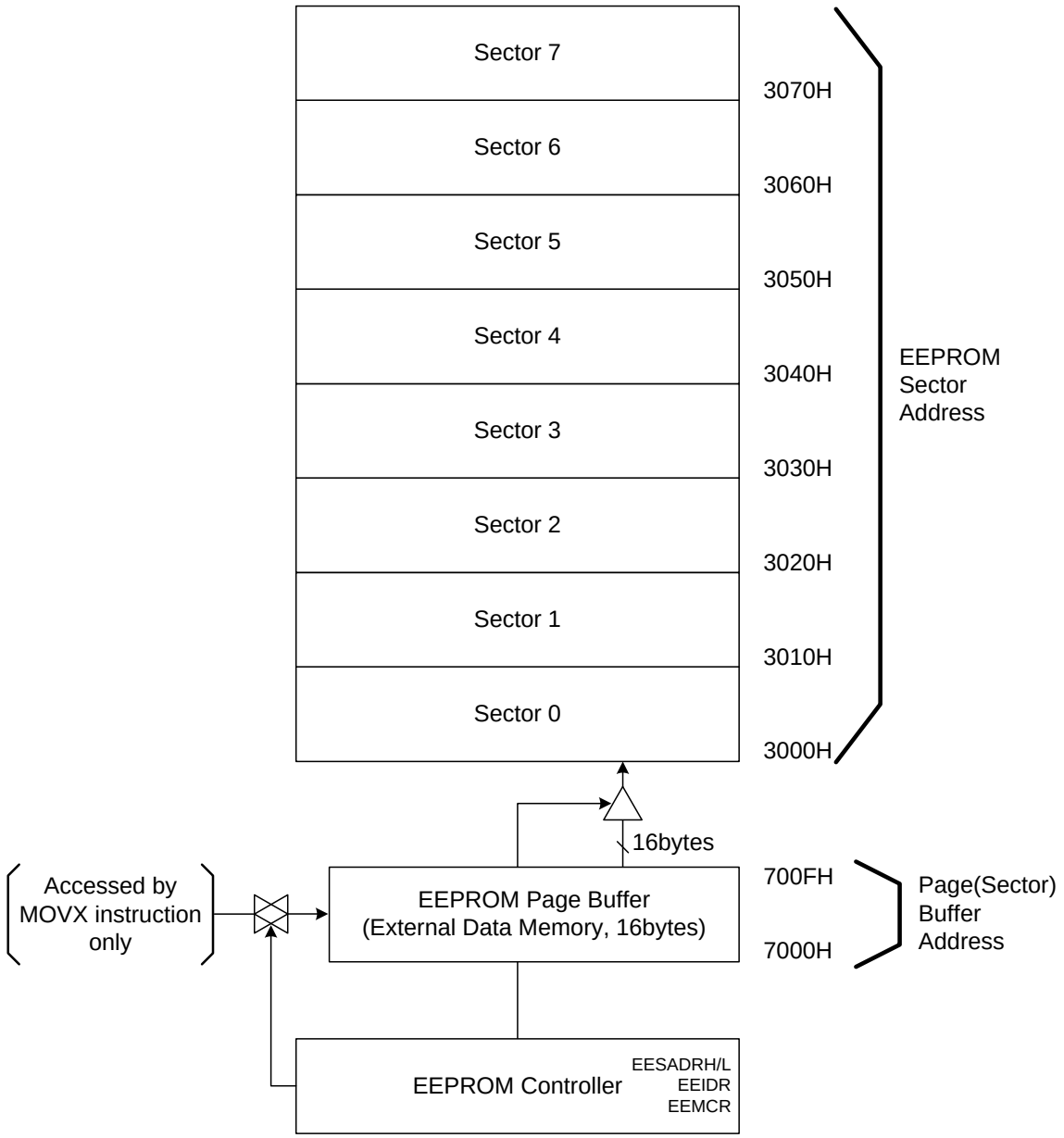
20 EEPROM memory

The A96L523 includes EEPROM memory of 128bytes. It can be written, erased, and overwritten. The EEPROM memory can be read by ‘MOVX’ instruction.

- EEPROM Size : 128bytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 100,000 program/erase cycles at typical voltage and temperature for memory

The write/erase cycles of the internal EEPROM can be increased significantly if it is divided into smaller and used in turn. If 128bytes are divided into 4 areas with 32bytes and the each area from 1st to 4th is used up to 100,000 cycles, the total erase/write is for 400,000 cycles.

20.1 EEPROM structure



NOTES:

1. The EEPROM supports byte and sector erase mode.
2. The EEPROM supports byte and sector write mode.
3. The EEPROM is in extended data memory area.
4. If Idle and Stop are executed on EEPROM erase/write, the erase/write is forcibly terminated. So before entering into the Idle mode or the Stop mode, the EEPROM busy bit (EEMBUSY) should be checked whether the bit is “1b”or not. If the bit is “1b”, do not enter into the Idle mode or in the Stop mode.

Figure 60. EEPROM Structure

21 Configure option

21.1 Configure option control

The data for configure option should be written in the configure option area (001EH – 001FH) by programmer (Writer tools).

CONFIGURE OPTION 1: ROM Address 001FH

7	6	5	4	3	2	1	0
R_P	HL	–	VAPEN	–	–	–	RSTS

Initial value: 00H

R_P	Code Read Protection	
	0	Disable
	1	Enable
HL	Code Write Protection	
	0	Disable
	1	Enable
VAPEN	Vector Area (00H – FFH) Write Protection	
	0	Disable Protection (Erasable by instruction)
	1	Enable Protection (Not erasable by instruction)
RSTS	Select RESETB pin	
	0	Disable RESETB pin (P10)
	1	Enable RESETB pin

CONFIGURE OPTION 2: ROM Address 001EH

7	6	5	4	3	2	1	0
–	–	–	–	–	PAEN	PASS1	PASS0

Initial value: 00H

PAEN	Enable Specific Area Write Protection		
	0	Disable (Erasable by instruction)	
	1	Enable (Not erasable by instruction)	
PASS [1:0]	Select Specific Area for Write Protection **NOTE**: When PAEN = '1', it is applied.		
	PASS1	PASS0	Description
	0	0	0.7Kbytes (Address 0100H – 03FFH)
	0	1	1.7Kbytes (Address 0100H – 07FFH)
	1	0	2.7Kbytes (Address 0100H – 0BFFH)
	1	1	3.6KBytes (Address 0100H – 0F7FH)

22 Logic functional description

22.1 Initial function

The VDD voltage is increasing by the external power VIN voltage increasing. If the VDD voltage is 2.4V then the UVLO signal go to high. By this signal, the internal reset is release.

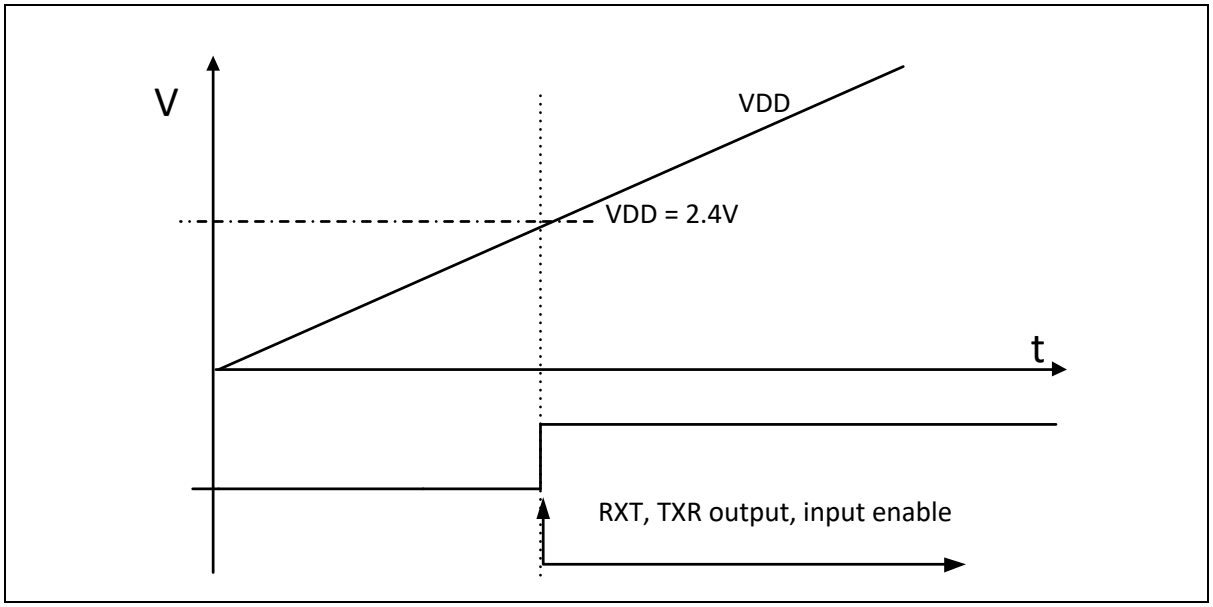


Figure 61. Reset release by VDD

22.2 Power charging

The A96L523 includes the inrush current limit by PMOS transistor. If the VIN voltage level is higher than the VOUT voltage level, the switch turns on via the comparator. At this time, capacitor C0 of VOUT becomes charged state, and if VOUT voltage is higher than or equal to VIN, the switch turns off.

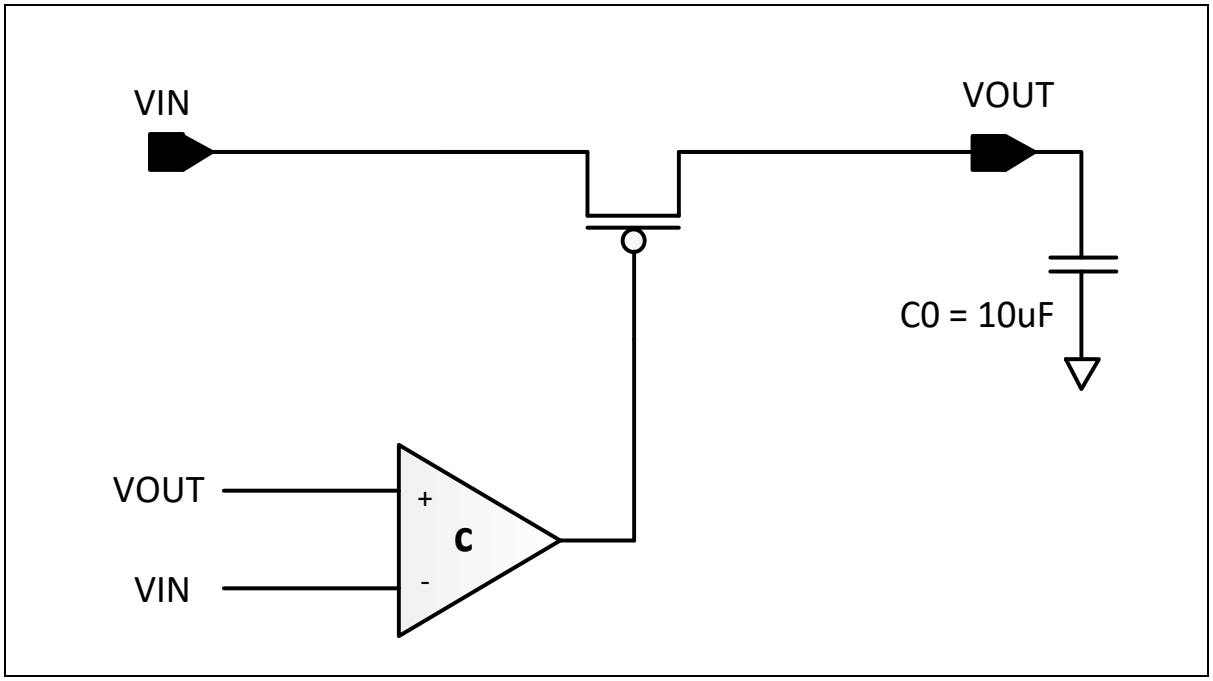


Figure 62. Power charging by VIN and VOUTV

22.3 RXT, RXR function

In case of line interface communication, data can be transferred by changing the VIN voltage. In the previous method, external comparator and resistor components were required. The A96L523 supports this function inside the IC

When the voltage difference between VOUT and VIN is more than 7.5V, Pin state changes to High through RXT pin and communication with Target MCU is performed with RXT pin.

If VOUT is operating voltage (8.5V or more) and VIN voltage is lower than 7.5V, RXT pin state becomes high. The period is called the TX period, and the TXR pin is used to change the VIN voltage at the target MCU. An N-MOS transistor is built in the IC. The A96L523 has the internal comparator. The comparator is operated as follow timing diagram.

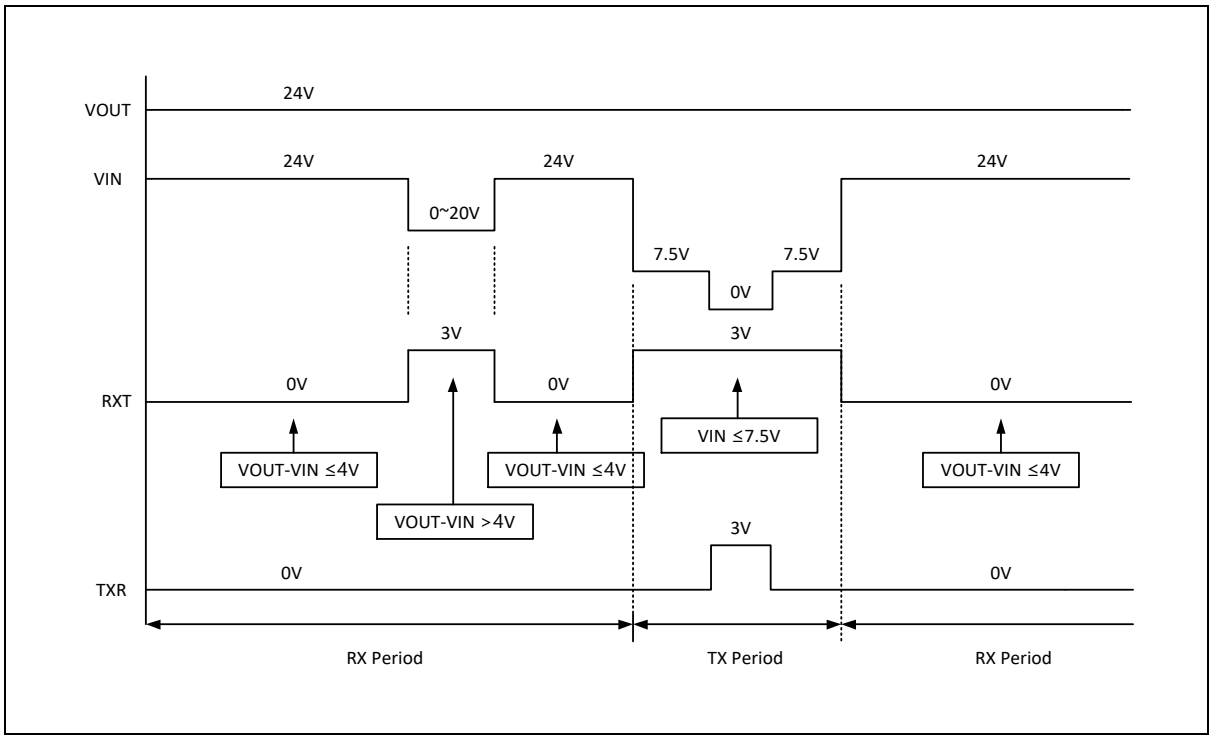


Figure 63. Timing Diagrams of RXT and TXR

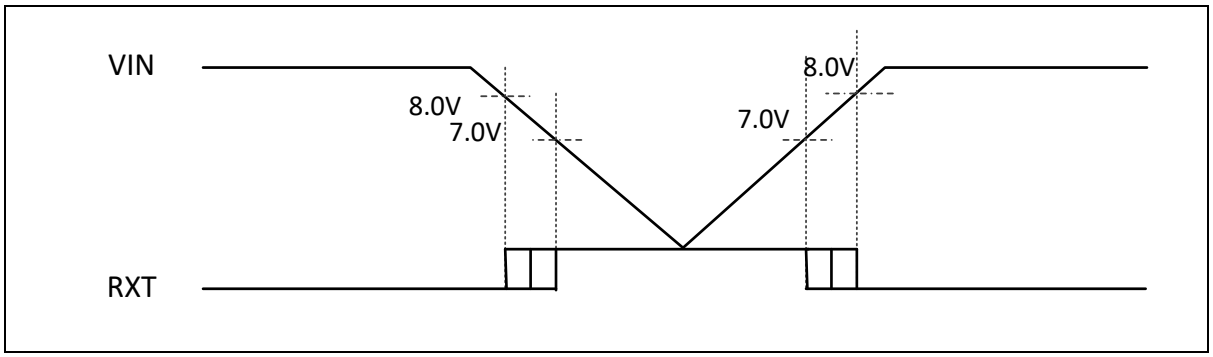


Figure 64. VIN and RXT Timing Diagram

22.4 LDO description

The A96L523 includes one LDO (Low Drop Output voltage) for microcontroller and indicated LED driver power. In the initial operation phase, when the power/signal line is connecting to VIN pin, the C0 capacitor on pin VOUT is charged. The BGR circuit generates the VREF voltage. The LDO circuit can generate the LDO voltage by VREF voltage.

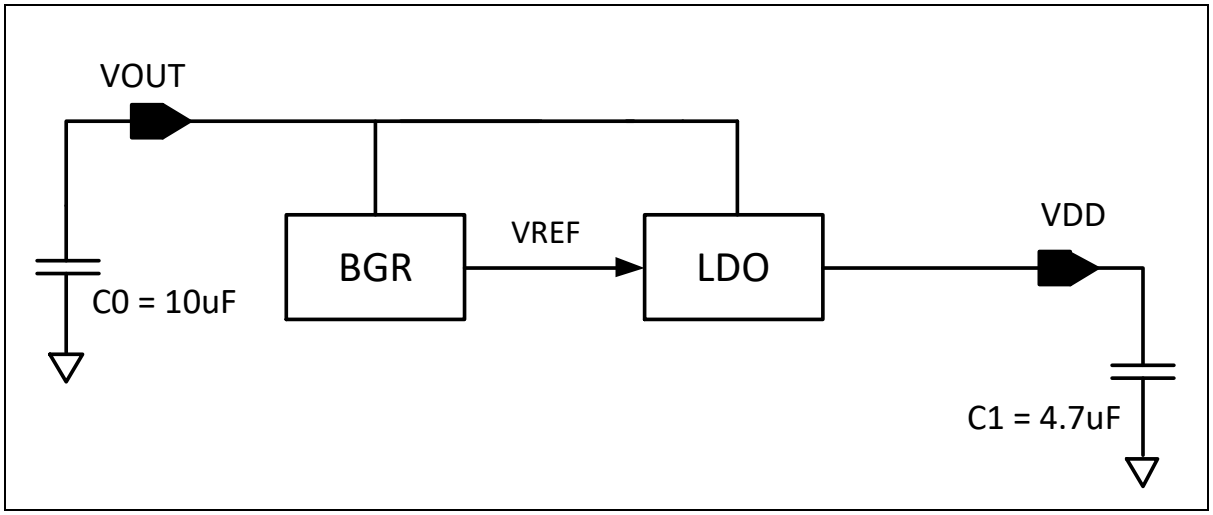


Figure 65. Block diagram of LDO

23 Electrical characteristics

23.1 Absolute maximum ratings

Table 12. Absolute Maximum Ratings (MCU)

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	VDD	-0.3 ~ +4.0	V	–
Normal Voltage Pin	V_I	-0.3 to VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 to VDD+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	120	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65 to +150	°C	–

Table 13. Absolute Maximum Ratings (Logic)

Parameter [NOTE]	Symbol	Rating	Unit
Supply Voltage	VIN	-0.5 to +47	V
	VSS	-0.5 to +0.5	V
Input / Output Pin Voltage	VIO	-0.5 to +35	V
LDO Output Current	IVDD	40	mA
Ground Current	IGND	40	mW
Total Power Dissipation	PT	300	mW
Storage Temperature	TSTG	-55 to +150	℃

NOTE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device

23.2 Recommended operating conditions

Table 14. Recommended Operating Conditions

(T_A=-40°C to +85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 0.125 to 1.0MHz, Internal RC	2.0	–	3.6	V
Supply Voltage	VIN		8.5		42	V
Operating Temperature	T_{OPR}		-40 NOTE	–	85	°C

NOTE: Electrolytic capacitors degrade at low temperatures, so consider using tantalum capacitors at low temperatures.

23.3 A/D converter characteristics

Table 15. A/D Converter Characteristics (MCU)

(TA= -40°C to +85°C, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	–	–		–	10	–	bit
Integral Linear Error	ILE	AVREF= 2.7V to 3.6V, fx= 1MHz		–	–	±3	LSB
Differential Linearity Error	DLE			–	–	±1	
Top Offset Error NOTE1	TOE			–	–	±5	
Zero Offset Error NOTE2	ZOE			–	–	±5	
Conversion Time	t_{CON}	AVREF= 2.7V to 3.6V		28	–	–	us
Analog Input Voltage	V_{AN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	NOTE3		2.0	–	VDD	
Sample/Hold Time	t_{SH}	–		6	–	–	us
A/DC Input Leakage Current	IAN	AVREF=3.3V		–	–	2	uA
A/DC Current	I_{ADC}	Enable	VDD= 3.3V	–	300	500	uA
		Disable		–	–	0.1	uA

NOTES:

1. Zero offset error is the difference between 0000000000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 1111111111 and the converted output for top input voltage (AVREF).
3. If AVREF is less than 2.7V, the resolution degrades by 1-bit whenever AVREF drops 0.1V. (@ADCLK = 0.5MHz, under 2.7V-resolution has no test.)

23.4 Power-on Reset characteristics

Table 16. Power-on Reset Characteristics (MCU)

(TA= -40°C to +85°C, VDD=2.0V ~ 3.6V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	0.2V to 2.0V	0.05	–	100	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

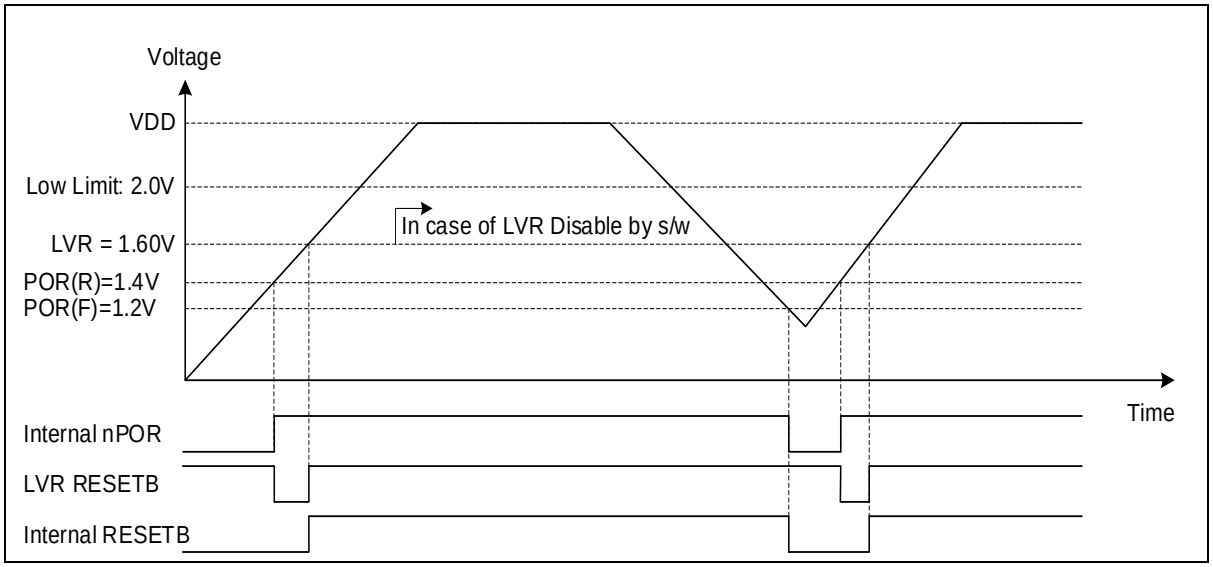


Figure 66. Power-on Reset Timing

23.5 Low Voltage Reset characteristics

Table 17. LVR Characteristics (MCU)

(T_A= -40°C to +85°C, VDD=2.0V ~ 3.6V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR}	The LVR can select all levels		–	1.60	1.89	V
				2.05	2.20	2.35	
				2.50	2.70	2.90	
Hysteresis	△V	–		–	10	100	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR Current	I_{LVR}	Enable	VDD= 3V, Run mode	–	4.0	8.0	uA
		Disable		–	–	0.1	

23.6 Operational amplifier 0/1 characteristics

Table 18. Operational Amplifier 0/1 Characteristics (MCU)

(T_A= -40°C to +85°C, VDD=2.7V ~ 3.6V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Offset Voltage	V_{OF}	VDD=3.3V	—	±10	±100	uV
Input Offset Current	I_{OF}	VDD=3.3V, VCM=0V	—	15	50	pA
Common-mode Rejection Ratio	CMRR	VDD=3.3V, DC VCM=0V to VDD-1.2V	80	100	—	dB
Power Supply Rejection Ration	PSRR	VDD=3.3V	80	100	—	
Open Loop Voltage Gain	—	VDD=3.3V	100	120	—	dB
Gain Error	ERR	VDD=3.3V, VIN ≥ 0.1V, x10 VIN<(Input x Gain)	—	—	1	%
Input Common-mode Voltage Range	V_{IN}	VDD=3.3V	0	—	VDD-1.2	V
Output Voltage Range	V_O	VDD=3.3V, RL=10KΩ	VSS+0.1	—	VDD-0.1	V
Output Short Circuit Current	ISCH	VDD=3.3V, Absolute	—	12	—	mA
	ISCL		—	12	—	
Gain Bandwidth	f_{GB}	VDD=3.3V	1	2	—	MHz
Voltage Follower Pulse Response	T_{AR}	VDD=3.3V, Small Signal	—	5	10	us
OP-AMP 0/1 Total Current	I_{AMP}	Enable, VDD=3.3V, No Load	—	150	220	uA
		Disable, VDD=3.3V, No Load	—	—	0.1	
Enable Time of AMP0/1	t_{ON}	VDD=3.3V, Gain=x20/x30, RL=10KΩ with 50pF	—	—	150	us
Input Noise Voltage Density	e_{ni}	Input Referred f=1Hz	—	0.1	—	uV/rt Hz
		Input Referred f=1KHz	—	50	—	nV/rt Hz
Slew Rate	S_R	VDD=3.3V, RL=10K, CL=50pF	—	0.7	—	V/us
Input Capacitance	C_{IN}	Common mode, T_A = +25℃	—	6	—	pF
Phase Margin	P_M	VDD=3.3V, RL=10K, CL=50pF	—	60	—	Degrees
Chopping Clock	f_{CHOP}	—	125	—	500	KHz

23.7 Internal RC oscillator characteristics

Table 19. Internal RC Oscillator Characteristics (MCU)

(T_A= -40°C to +85°C, VDD=2.0V ~ 3.6V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{IRC}	VDD=3.3V	–	1	–	MHz
Tolerance	–	T_A = -10°C to +40°C, with user(S/W) trim	–	–	±1.0	%
		T_A = -10°C to +40°C			±2.0	

		T_A = -40°C to +85°C			±3.0	
Clock Duty Ratio	T_{OD}	–	40	50	60	%
Stabilization Time	T_{FS}	–	–	–	100	us
IRC Current	I_{IRC}	Enable	–	15	–	uA
		Disable	–	–	0.1	uA

23.8 Internal Watch-Dog Timer RC oscillator characteristics

Table 20. Internal WDTRC Oscillator Characteristic (MCU)

(T_A= -40°C to +85°C, VDD=2.0V ~ 3.6V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	–	0.5	1	2	KHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

23.9 DC characteristics

Table 21. DC Characteristics (MCU)

(T_A= -40°C to +85°C, VDD=2.0V to 3.6V, VSS=0V, f_{IRC} = 1MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P00, P01, P06, P07, P1, RESETB		0.8VDD	–	VDD	V
	V_{IH2}	All input pins except VIH1		0.7VDD	–	VDD	
Input Low Voltage	V_{IL1}	P00, P01, P06, P07, P1, RESETB		–	–	0.2VDD	V
	V_{IL2}	All input pins except VIL1		–	–	0.3VDD	
Output High Voltage	V_{OH}	VDD=3.3V, IOH = – 6mA; All output ports		VDD-1.0	–	–	V
Output Low Voltage	V_{OL}	VDD=3.3V, IOL = 8mA; All output ports		–	–	1.0	V
Input High Leakage Current	I_{IH}	All Input ports		–	–	1.0	uA
Input Low Leakage Current	I_{IL}	All Input ports		- 1.0	–	–	uA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A=25℃, All Input ports	VDD=3.0V	50	100	200	KΩ
	R_{PU2}	VI=0V, T_A=25℃, RESETB	VDD=3.0V	300	500	700	KΩ
Supply Current	I_{DD1} (RUN)	f_{IRC} = 1MHz	VDD= 3V±10%	–	240	320	uA
		f_{IRC} = 0.5MHz		–	150	200	
	I_{DD2} (IDLE)	f_{IRC} = 1MHz	VDD= 3V±10%	–	100	150	uA
		f_{IRC} = 0.5MHz		–	90	140	
	I_{DD5}	STOP, VDD= 3V±10%, T_A= 25°C		–	0.5	3.0	uA

NOTES:

1. Where the fx is the selected system clock, the fIRC is an internal RC oscillator.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current include the current of the power-on reset (POR) block.

Table 22. DC Characteristics (Logic)

(T_A= 25°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Voltage	VIN	-	8.5	24	42	V
LDO Output Voltage	VDD	IOUT=1mA VOUT=24V @ T=25°C	2.91	3.0	3.09	V
	dVDD	IOUT=1mA to 5mA, VOUT=24V	-	15	20	mV
		IOUT=5mA to 20mA, VOUT=24V	-	15	45	
LDO Output Tolerance	Vtol	VDD=3.0V @-10 to 60°C	-3		3	%
PSRR	PSRR	F=100Hz	50			dB
TXR Pull-down	IiH	VDD=3V	20	40	60	uA
Inrush Current	IVIN1	VIN=0V to 24V, @rise time 10ms		24	35	mA
TXR Current	IVIN2	VIN=7V, VOUT = 24V	60			mA
Input High Voltage TXR	Vih	VDD=3V	0.8*VDD		VDD	V
Input Low Voltage TXR	Vil	VDD=3V	0		0.2*VDD	V
Output High Voltage RXT	Voh	VDD=3V, Ioh= -1mA	0.8*VDD		VDD	V
Output Low Voltage RXT	Vol	VDD=3V, Iol=1mA	0		0.2*VDD	V
VIN Input Voltage for RXT High	VRXH1	VOUT =8.5V	7.0		8.0	V
VOUT-VIN Voltage for RXT High	VRXH2	VOUT=24V	7.0		8.0	V
Static Current	IVIN	VIN=24V, VOUT = 24V, TXR = 0V, @T=25°C		60	90	uA

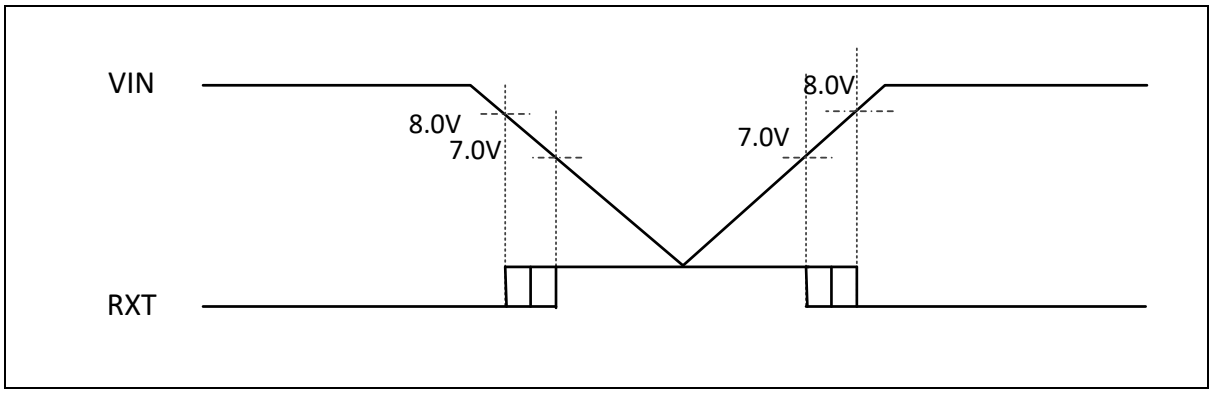


Figure 67. VIN and RXT Timing Diagram

23.10 Constant sink current electrical characteristics

Table 23. Constant Sink Current Electrical Characteristics (MCU)

(TA= -40°C to +85°C, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Constant Sink Current	I_{CS}	VDD=3V, V_{ICS}=1.5V, T_A= 25°C	ICSDR[3:0] = 0	-7%	49	+7%	mA
			ICSDR[3:0] = 1	-7%	65	+7%	
			ICSDR[3:0] = 2	-7%	80	+7%	
			ICSDR[3:0] = 3	-7%	96	+7%	
			ICSDR[3:0] = 4	-7%	111	+7%	
			ICSDR[3:0] = 5	-7%	127	+7%	
			ICSDR[3:0] = 6	-7%	142	+7%	
			ICSDR[3:0] = 7	-7%	158	+7%	
			ICSDR[3:0] = 8	-7%	173	+7%	
			ICSDR[3:0] = 9	-7%	188	+7%	
			ICSDR[3:0] = 10	-7%	203	+7%	
			ICSDR[3:0] = 11	-7%	218	+7%	
			ICSDR[3:0] = 12	-7%	232	+7%	
			ICSDR[3:0] = 13	-7%	246	+7%	
			ICSDR[3:0] = 14	-7%	260	+7%	
			ICSDR[3:0] = 15	-7%	274	+7%	
		VDD=3V, V_{ICS}=1V to 2.0V, T_A= -40 to +85°C	ICSDR[3:0] = n n : 0 to 15	-15%	Typ.	+15%	
		VDD=2.7V to 3.6V, V_{ICS}=1V to VDD-1.0V, T_A= -40 to +85°C	ICSDR[3:0] = n n : 0 to 15	-20%	Typ.	+20%	

23.11 AC characteristics

Table 24. AC Characteristics (MCU)

(T_A= -40°C to +85°C, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RST}	VDD = 3V	10	–	–	us
RXT Response time	Trx, tfxfMCP	VOUT=24V	-	4	-	us
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt, VDD = 3V	200	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	EC0/EC1, VDD = 3V	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	EC0/EC1, VDD = 3V	20	–	–	

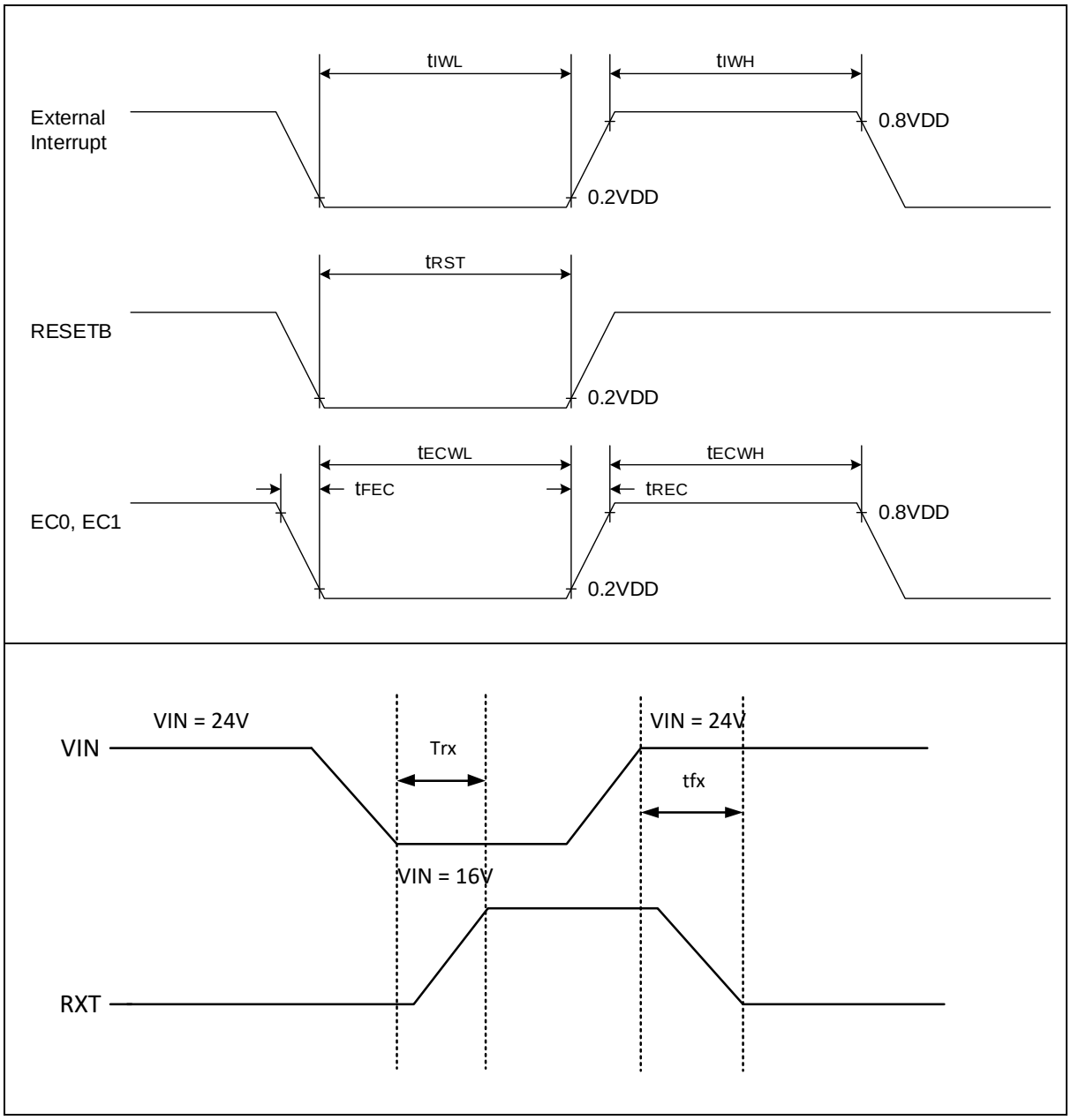


Figure 68. AC Timing (Logic)

23.12 SPI characteristics

Table 25. SPI Characteristics (MCU)

(T_A= -40°C to +85°C, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	t_{SCK}	Internal SCK source	2000	–	–	ns
Input Clock Pulse Period		External SCK source	2000	–	–	
Output Clock High, Low Pulse Width	t_{SCKH}, t_{SCKL}	Internal SCK source	700	–	–	
Input Clock High, Low Pulse Width		External SCK source	700	–	–	
First Output Clock Delay Time	t_{FOD}	Internal/External SCK source	1000	–	–	
Output Clock Delay Time	t_{DS}	–	–	–	250	
Input Setup Time	t_{DIS}	–	1000	–	–	
Input Hold Time	t_{DIH}	–	1000	–	–	

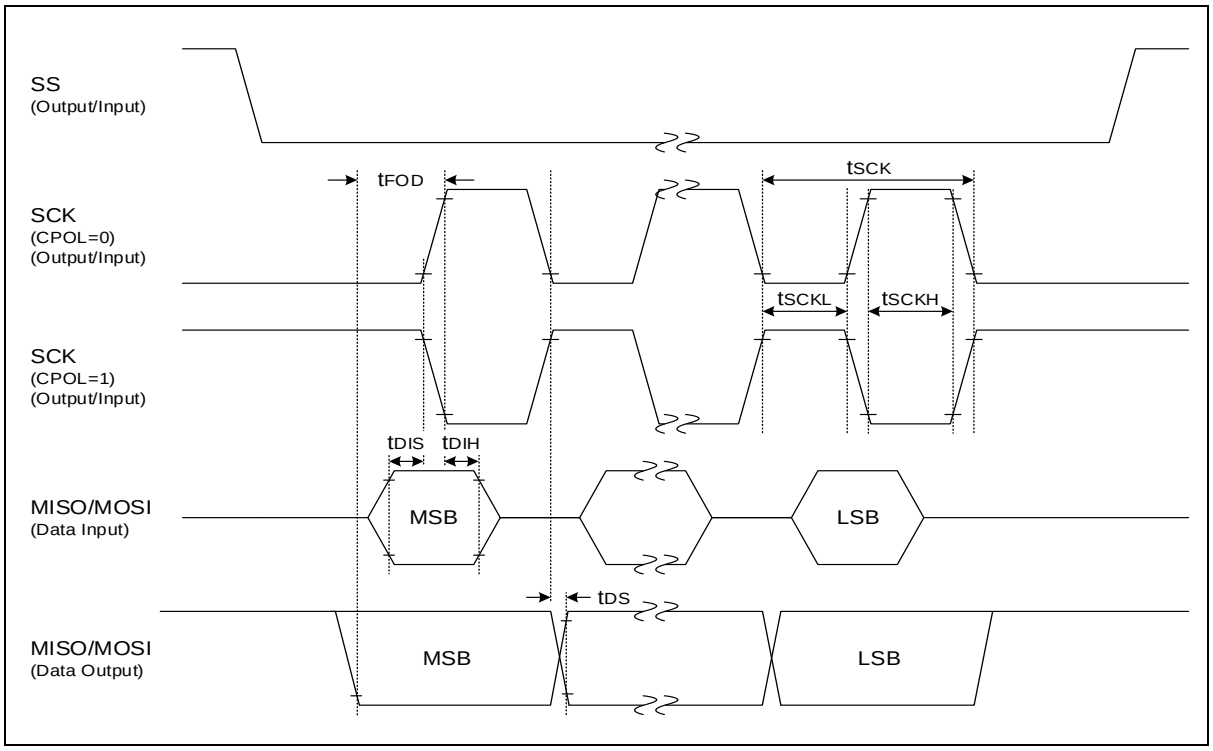


Figure 69. SPI Timing

23.13 UART timing characteristics

Table 26. UART Timing Characteristics (MCU)

(T_A= -40°C to +85°C, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	t_{SCK}	13.92	t_{CPU} x 16	18.08	us
Output data setup to clock rising edge	t_{S1}	6.5	t_{CPU} x 13	–	
Clock rising edge to input data valid	t_{S2}	–	–	6.5	
Output data hold after clock rising edge	t_{H1}	t_{CPU} – 0.1	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	5.5	t_{CPU} x 8	10.5	

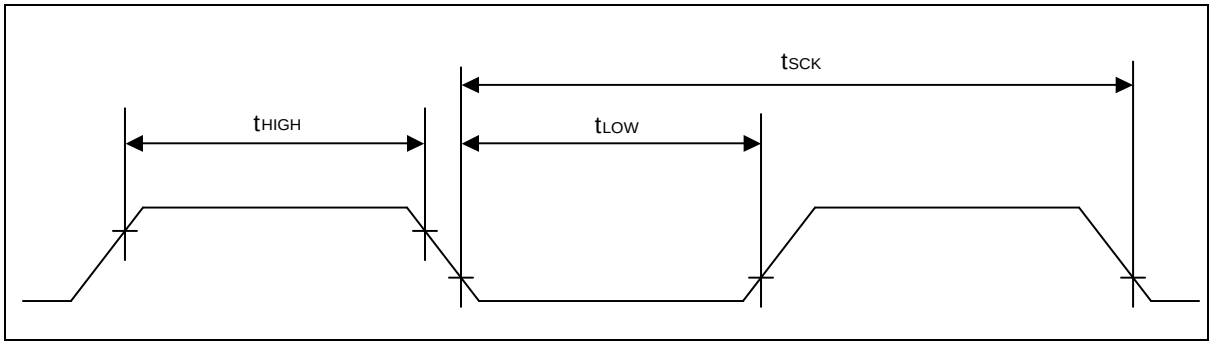


Figure 70. Waveform for UART Timing Characteristics

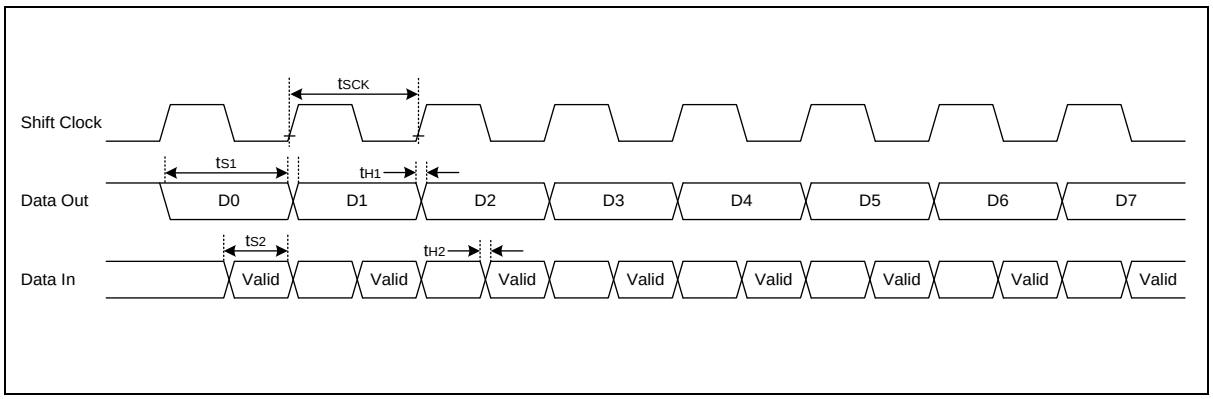


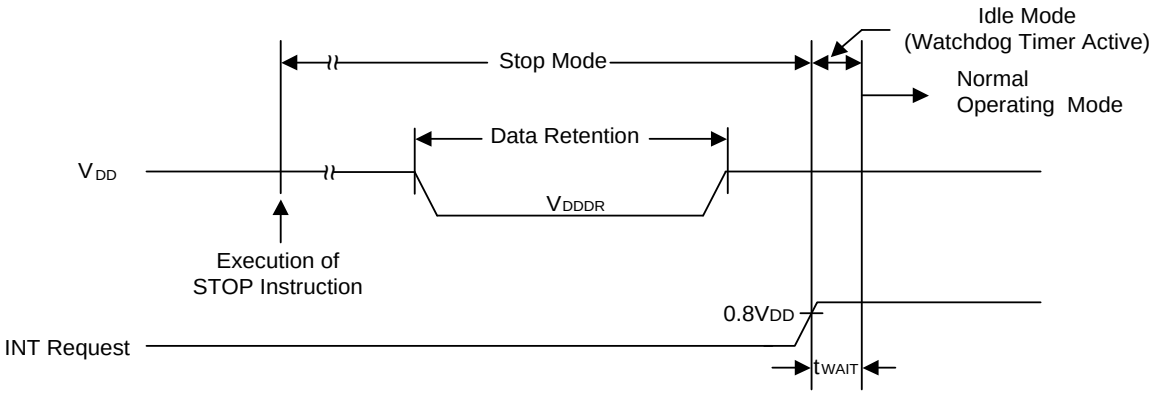
Figure 71. Timing Waveform for UART Module

23.14 Data retention voltage in stop mode

Table 27. Data Retention Voltage in Stop Mode (MCU)

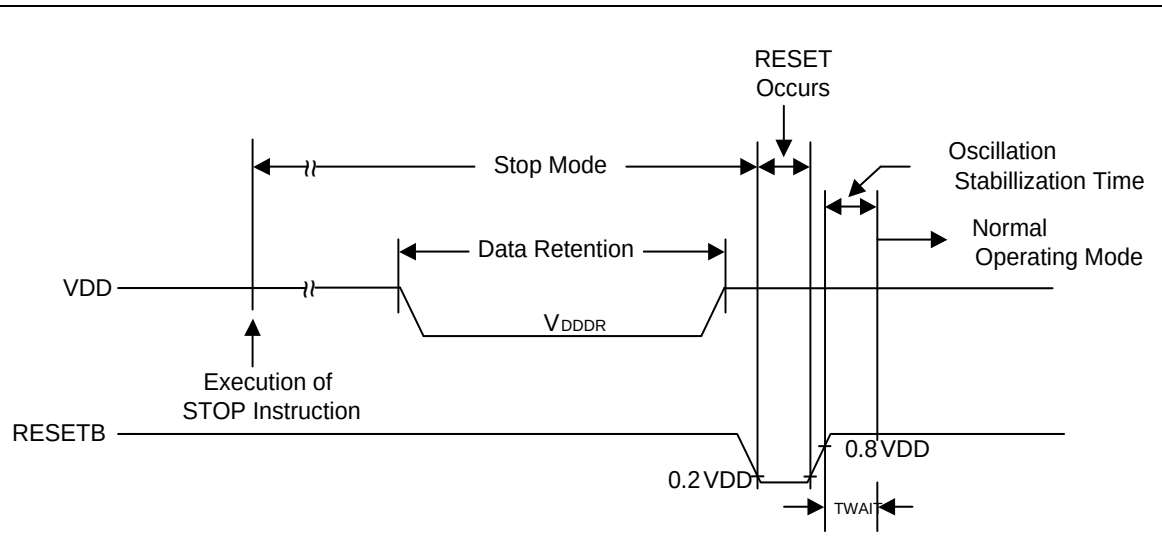
(TA= -40°C to +85°C, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	2.0	–	3.6	V
Data retention supply current	I_{DDDR}	VDDR= 2.0V, (T_A= 25°C), Stop mode	–	–	1	uA



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock).

Figure 72. Stop Mode Release Timing when Initiated by an Interrupt



NOTE: tWAIT is the same as (4096 X 4 X fIRC) = (16.4 mS at fx=1MHz).

Figure 73. Stop Mode Release Timing when Initiated by RESETB

23.15 Internal flash ROM characteristics

Table 28. Internal Flash ROM Characteristics (MCU)

(T_A= -40°C to +85°C, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.125	–	–	MHz
Endurance of Write/Erase (Sector 0 to 123)	NF_{WE}	Sector Erase, Byte Write	10,000	–	–	cycles
Endurance of Write/Erase (Sector 124 to 127)			100,000	–	–	

23.16 Internal EEPROM characteristics

Table 29. Internal Flash ROM Characteristics (MCU)

(T_A= -40°C to +85°C, VDD=2.0V ~ 3.6V, VSS=0V

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{ESW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{ESE}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{EBR}	–	–	–	5	us
EEPROM Programming Frequency	f_{PGM}	–	0.125	–	–	MHz
Endurance of Write/Erase	NE_{WE}	Sector Erase, Byte Write	100,000	–	–	cycles

NOTES:

1. The write/erase cycles of the internal EEPROM can be increased significantly if it is divided into smaller and used in turn.
2. Ex) If 128bytes are divided into 4 areas with 32bytes and the each area from 1st to 4th is used up to 100,000 cycles, the total erase/write is for 400,000 cycles.

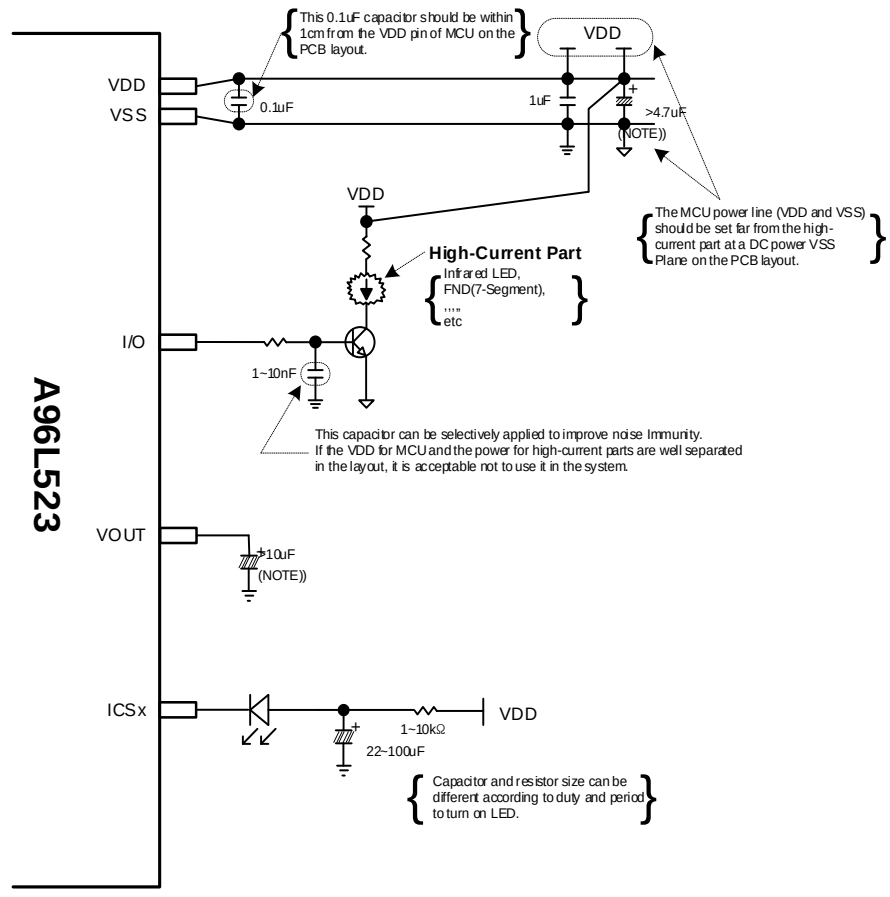
23.17 Input/ output capacitance

Table 30. Input/ Output Capacitance (MCU)

(T_A= -40°C to +85°C, VDD=2.0V to 3.6V, VSS=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

23.18 Recommended circuit and layout



NOTES:

1. Vout and VDD capacitors are the minimum size conditions,
2. When Vout = 100uF and VDD = 47uF or more, it shows the best performance

Figure 74. Recommended Circuit and Layout

23.19 UVLO characteristics

Table 31. UVLO Characteristics (Logic)

(TA= -40°C to +85℃)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
RESET Release Level		-	-	2.4	-	V

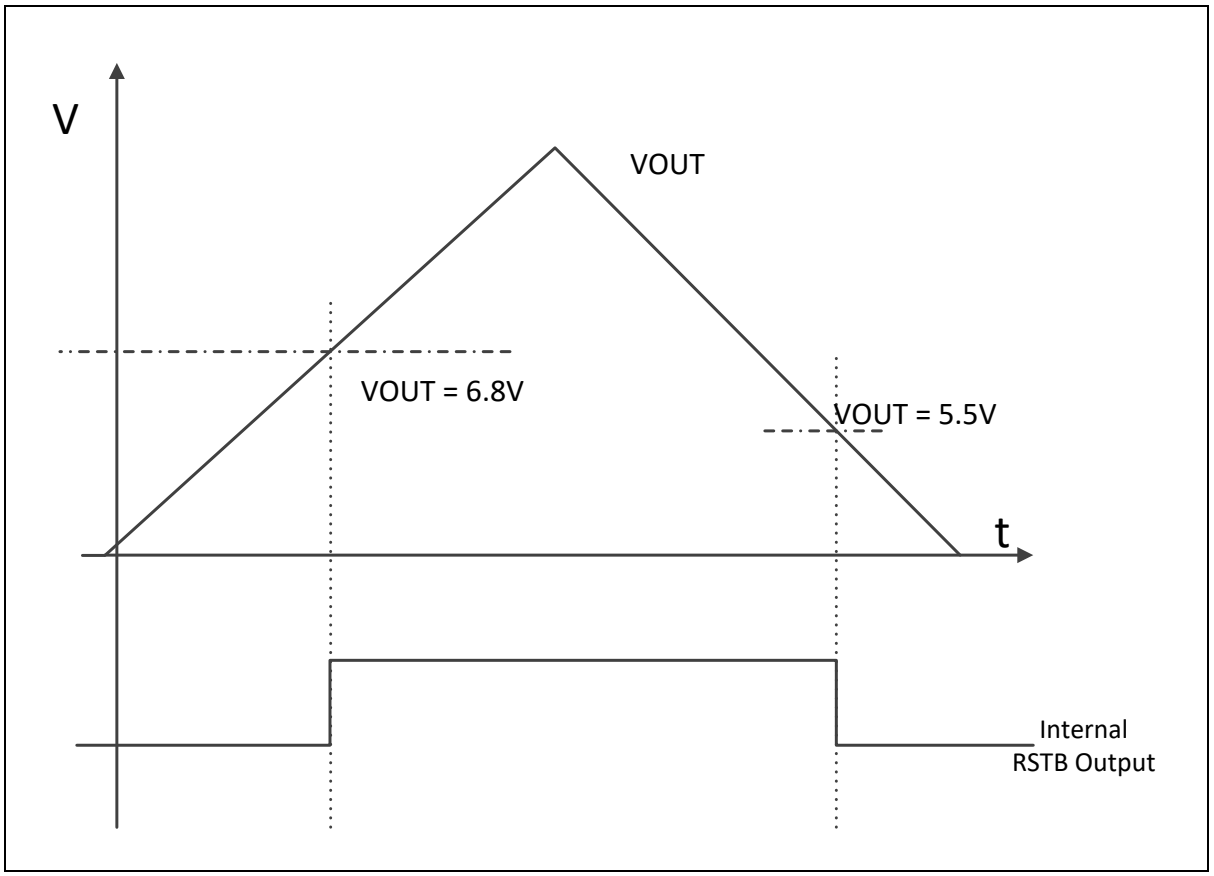


Figure 75. Internal UVLO Timing Diagrams

23.20 Typical characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

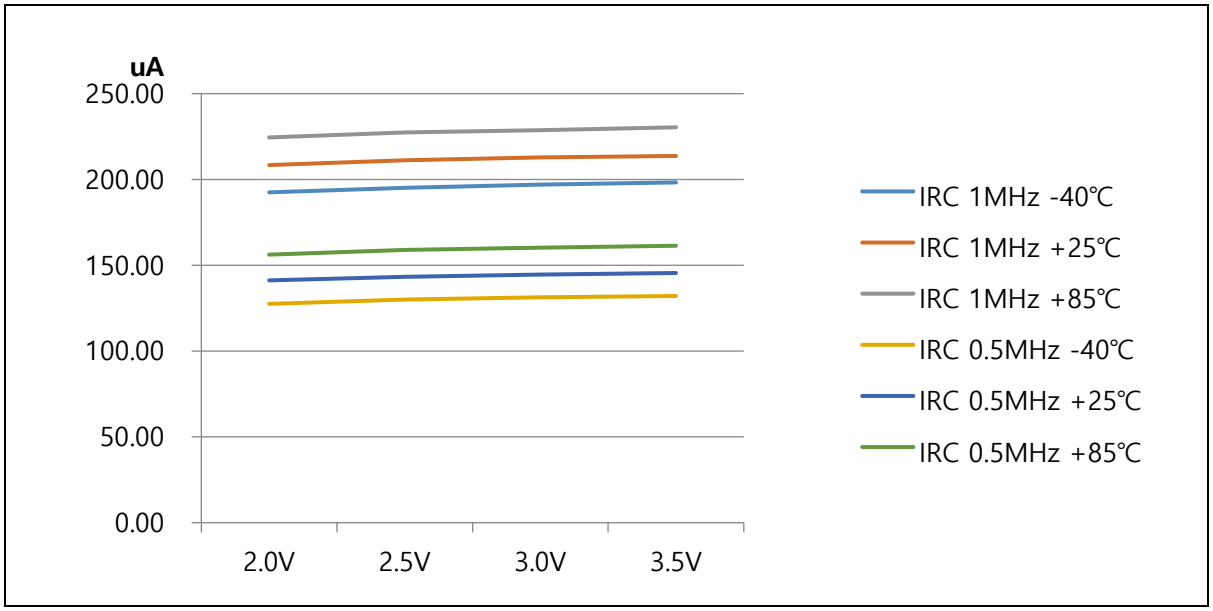


Figure 76. IRC RUN (IDD1) Current

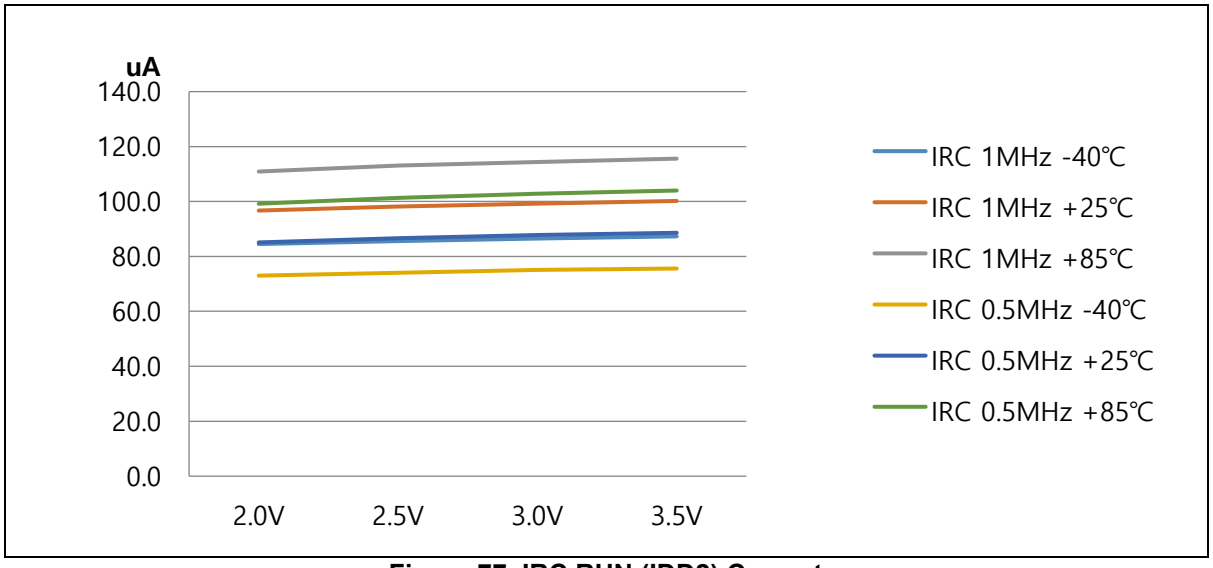


Figure 77. IRC RUN (IDD2) Current

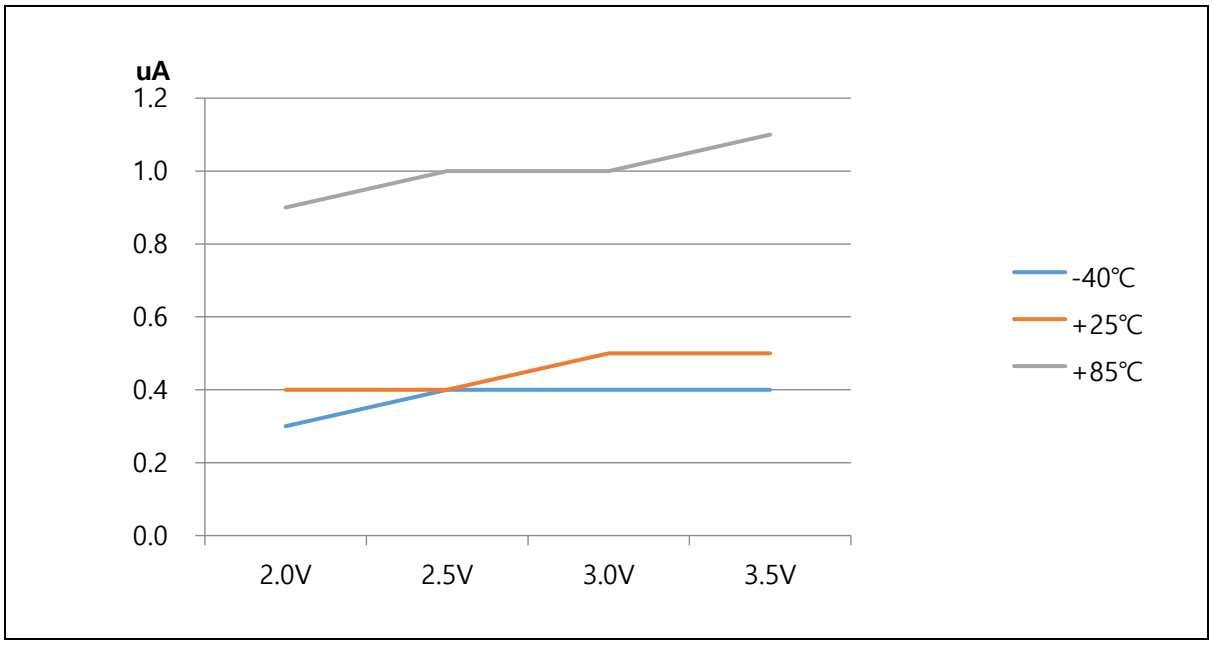


Figure 78. STOP (IDD5) Current

24 Package information

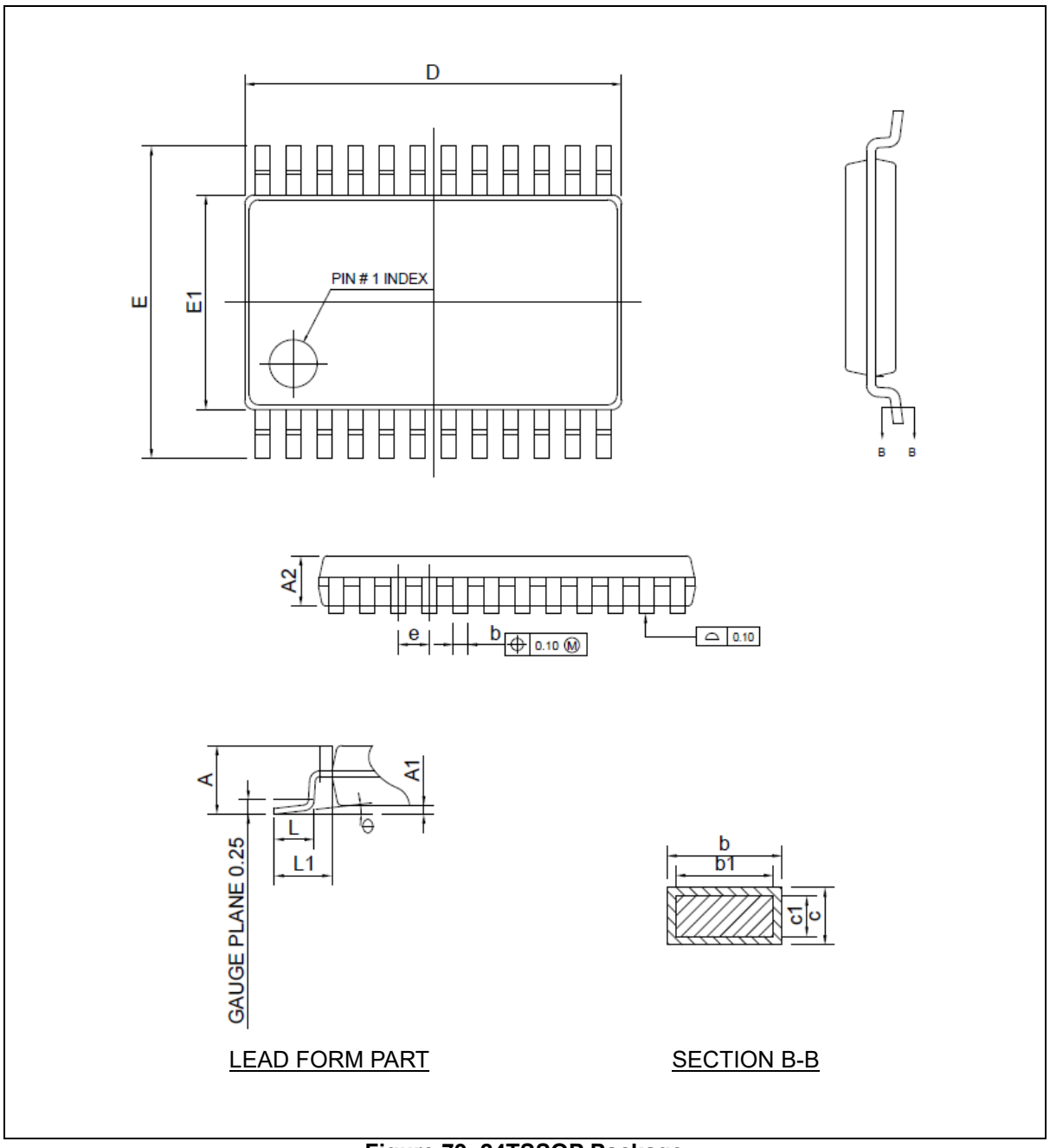


Figure 79. 24TSSOP Package

Table 32. 24 TSSOP Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	—	8°

NOTES:

1. All dimensions refer to JEDEC standard MO-153-AD.
2. Dimension ‘D’ does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burr shall not exceed 0.15mm per side.
3. Dimension ‘E1’ does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.

25 Ordering information

Table 33. A96L523 Device Ordering Information

Device Name	FLASH	IRAM	EEPROM	ADC	I/O PORT	Line interface	Package
A96L523LRN	4 Kbytes	256 bytes	128 Bytes	9 inputs	14	6	24 TSSOP

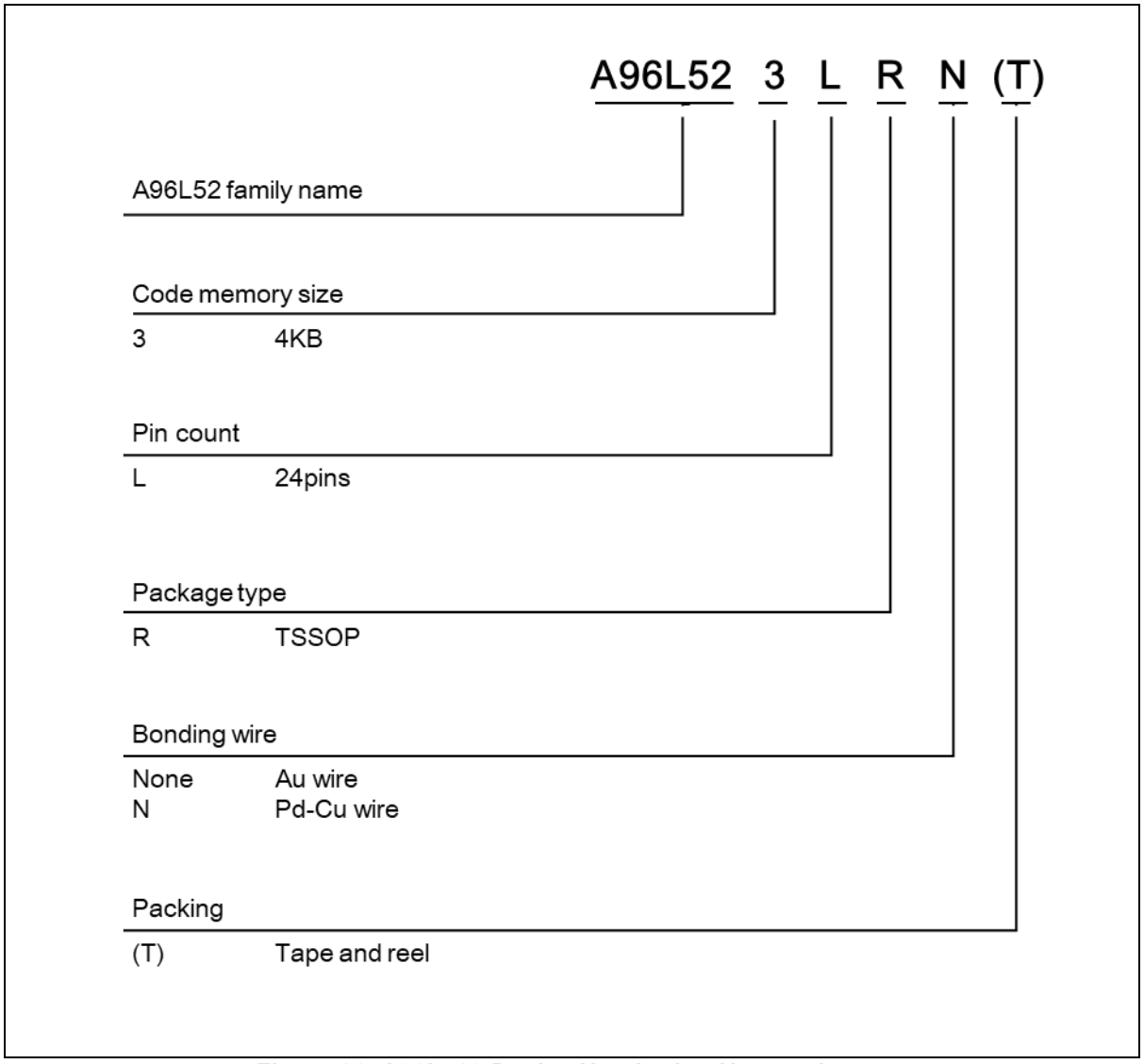


Figure 80. A96L523 Device Numbering Nomenclature

Appendix

A. Flash protection for invalid erase/write

This is example to prevent changing code or data in flash by abnormal operation (noise, unstable power, malfunction, etc.).

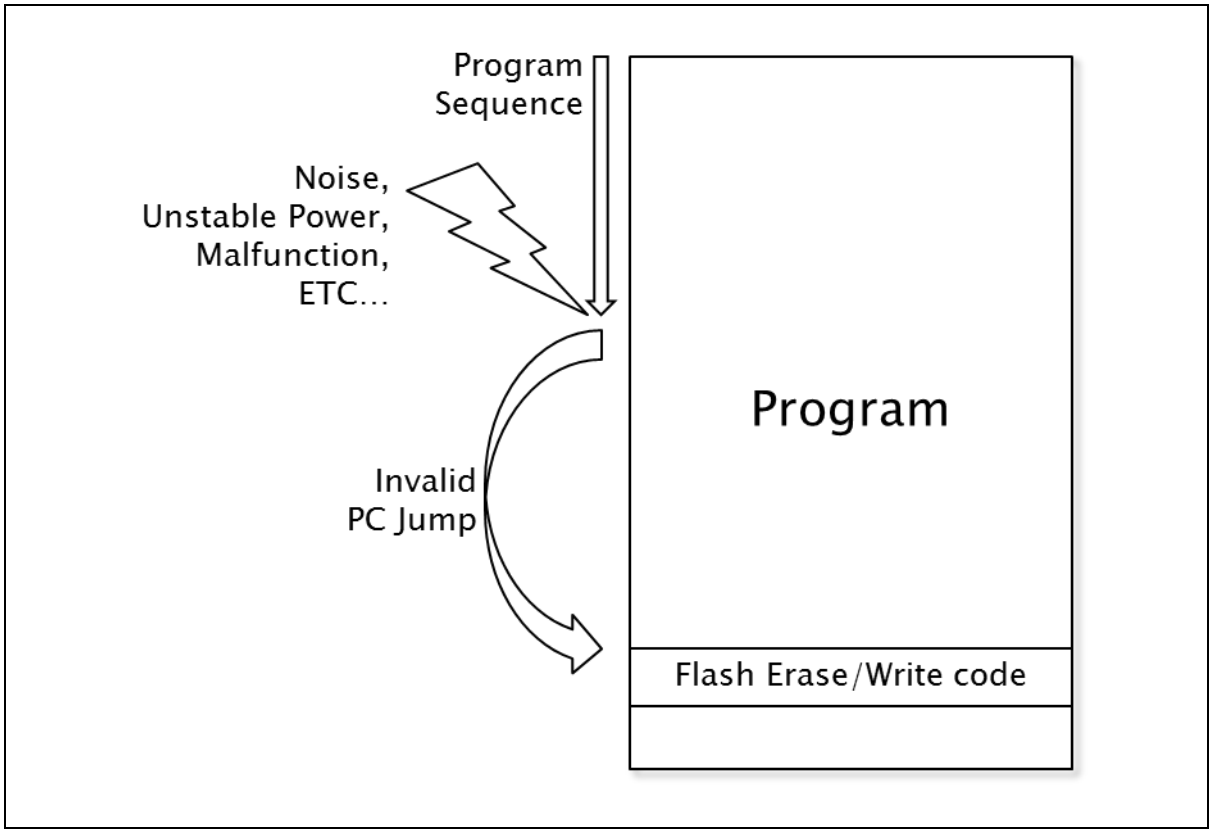


Figure 81. Flash invalid Erase/Write

How to protect the flash

- Divide into decision and execution to Erase/Write in flash.
  - Check the program sequence from decision to execution in order of precedence about Erase/Write.
  - Setting the flags in program and check the flags in main loop at the end
  - When the Flash Erase/Write is executed, check the flags. If not matched, do not execute.
- Check the range of Flash Sector Address
  - If the flash sector address is outside of specific area, do not execute.
- Use the Dummy Address
  - Set the flash sector address to dummy address in usually run time.
  - Change the flash sector address to real area range shortly before Erase/Write.
  - Even if invalid Erase/Write occurred, it will be Erase/Write in dummy address in flash.
- Use the LVR/LVI
  - Unstable or low powers give an adverse effect on MCU. So use the LVR/LVI

Flowchart

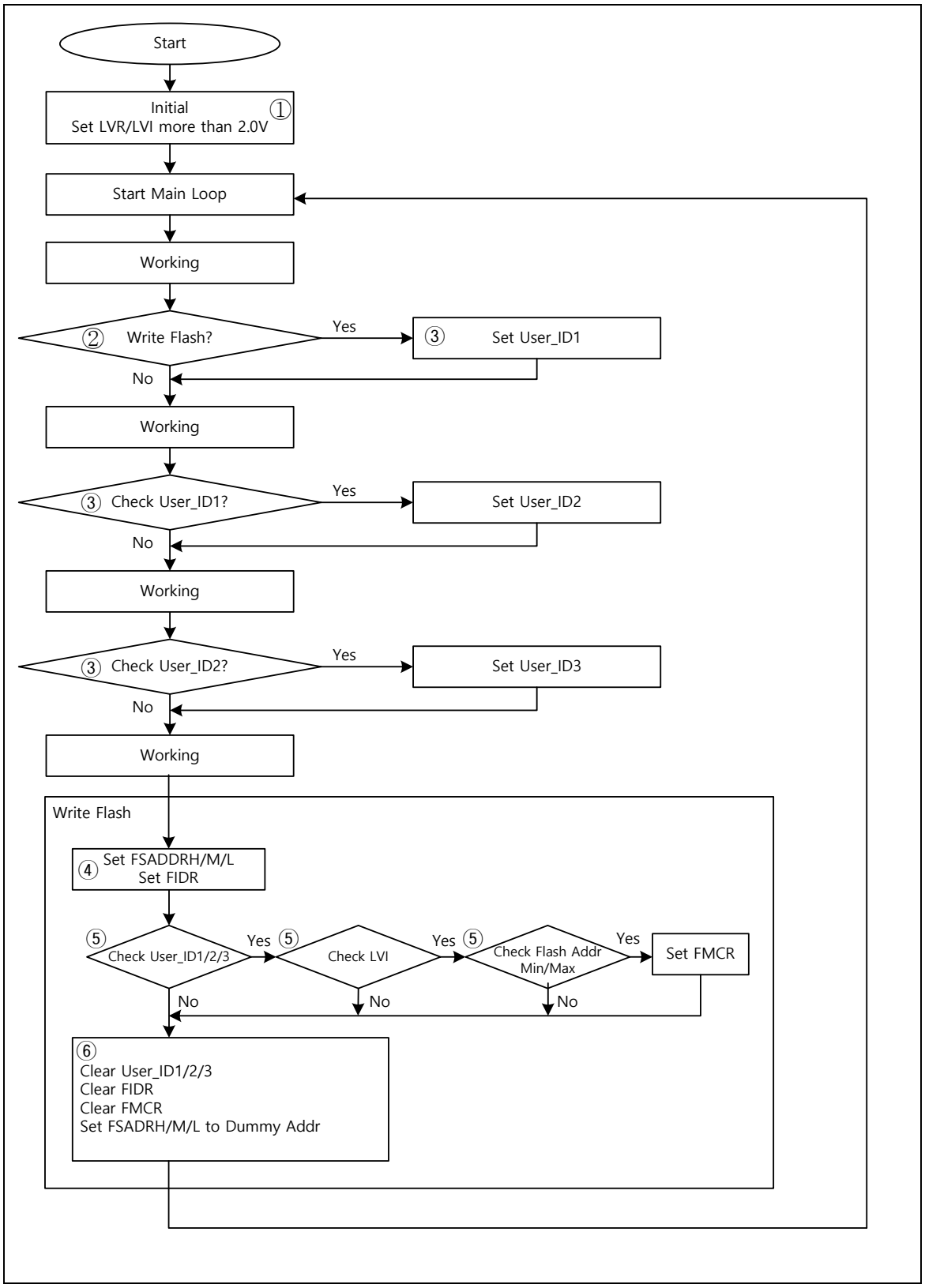


Figure 82. Flow chart of protect flash

Descript of flowchart

① Initialization

- Set the LVR/LVI: Check the power by LVR/LVI and do not execute under unstable or low power.
- Initialize User_ID1/2/3
- Set Flash Sector Address High/Middle/Low to Dummy address
  Dummy address is set to unused area range in flash.

② Decide to Write

- When the Erase/Write are determined, set flag. Do not directly Erase/Write in flash.
- Make the user data.

③ Check and Set User_ID1/2/3

- In the middle of source, insert code which can check and set the flags.
- By setting the User_ID 1/2/3 sequentially and identify the flow of the program.

④ Set Flash Sector Address

- Set address to real area range shortly before Erase/Write in flash.
  Set to Dummy address after Erase/Write
  Even if invalid work occurred, it will be Erase/Write in Dummy address in flash.

⑤ Check Flags

- If every flag (User_ID1/2/3, LVI, Flash Address Min/Max) was set, than do Erase/Write.
- If the Flash Sector Address is outside of Min/Max, do not execute
- Address Min/Max is set to unused area.

⑥ Initialize Flags

- Initialize User_ID1/2/3
- Set Flash Sector Address to Dummy Address

⑦ Sample Source

- Refer to the ABOV homepage.
- It is created based on the MC97F2664.
- Each product should be modified according to the Page Buffer Size and Flash Size

Other methods to protect flash

- Protection by Configure option
  - Set flash protection by MCU Write Tool (OCD, PGM+, etc.)

Vector Area:

00H~FFH

Specific Area:

0.7KBytes (Address 0100H – 03FFH)

1.7KBytes (Address 0100H – 07FFH)

2.7KBytes (Address 0100H – 0BFFH)

3.6KBytes (Address 0100H – 0F7FH)

— The range of protection may be different each product.

B. Example circuit

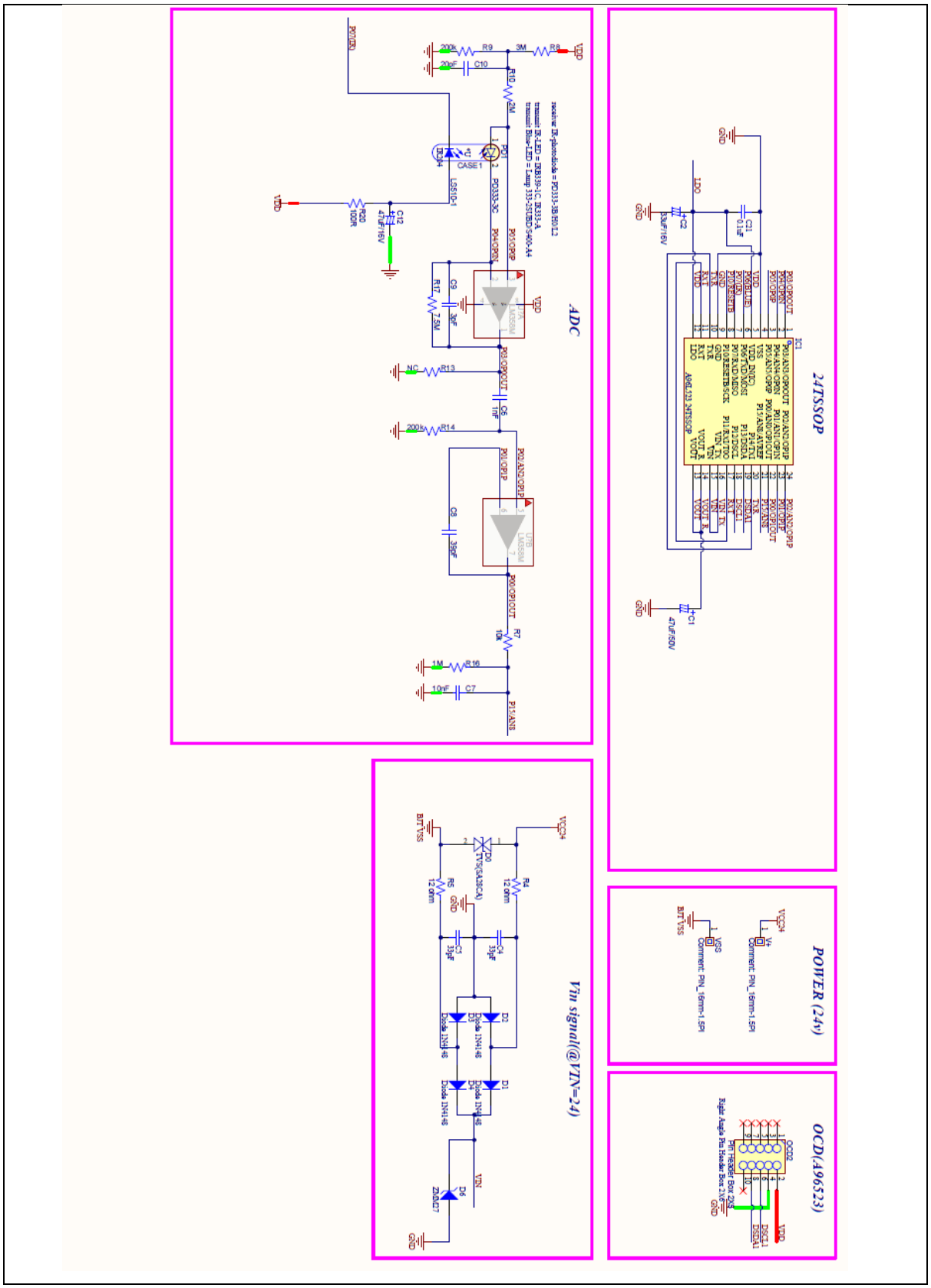


Figure 83. Example circuit using only IR LED

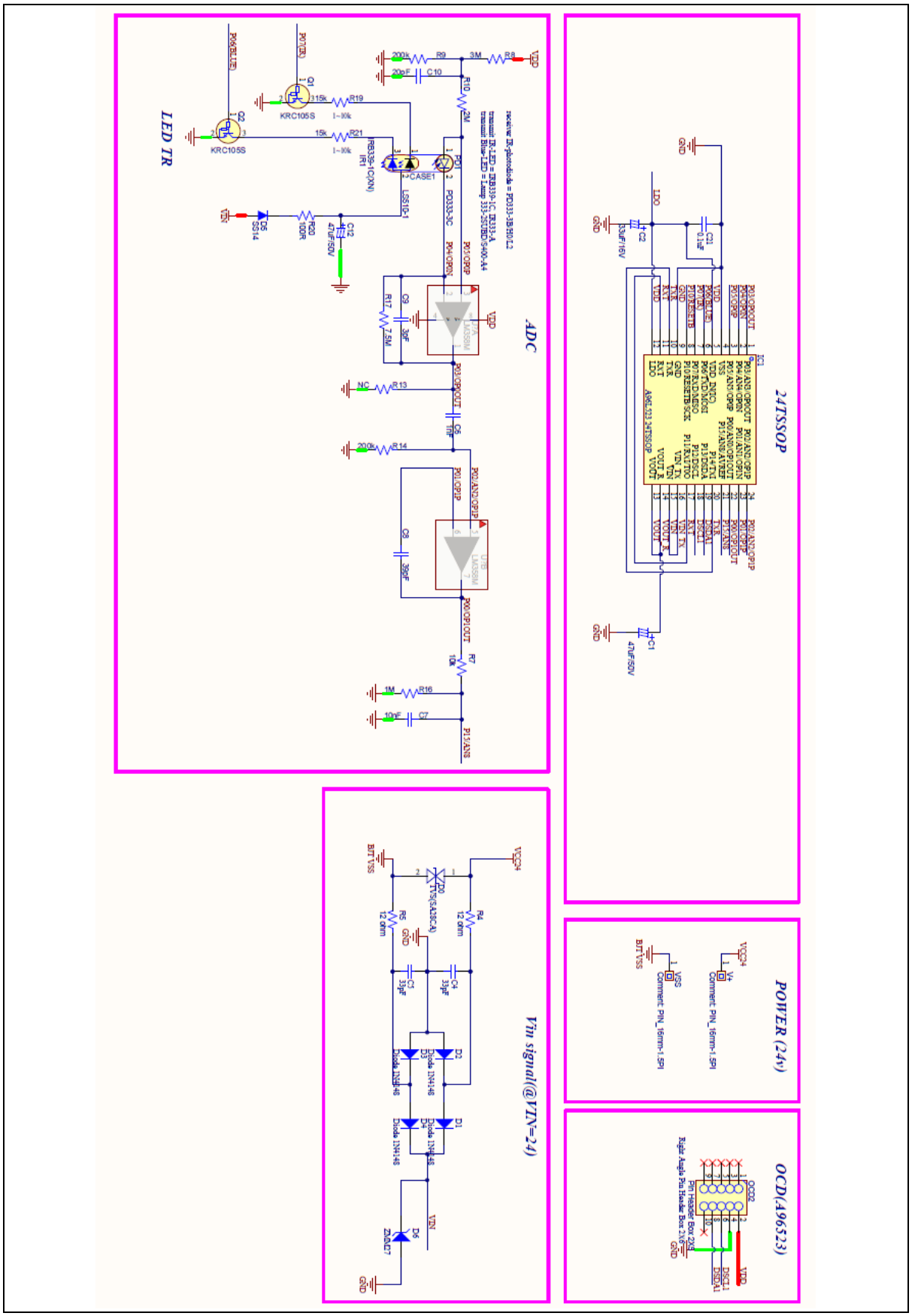


Figure 84. Example circuit using IR LED and Blue LED

Revision history

Date	Revision	Description
2020.01.07	1.00	1st creation
2020.01.13	1.01	• Updated UVLO block diagram • Updated logic block diagram
2020.01.28	1.10	• Updated features. • Updated description in 1.3.15 • Updated description in 14 • Updated inrush current in chapter 23.9 • Updated package information in chapter 24 • Updated Ordering information in chapter 25 • Updated proprietary notice
2020.02.04	1.11	• Fixed www.abov.co.kr to www abovsemi.com
2020.06.30	1.20	• Fixed static current value Max. 80uA to 90uA
2020.09.15	1.21	• Updated figure84 and 85
2020.10.19	1.22	• Updated figure84 and 85
2020.11.25	1.30	• Fixed T1CRL Register bit[3] T1BPOL to RLD1EN • Updated timer1 block diagrams • Deleted 16-bit complementary PWM mode of Timer1 • Updated Siren in timer1 • Add Input Capacitance in Table 18. Operational Amplifier 0/1 Characteristic.
2022.11.10	1.31	• Revised the font of this document

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