AC30M1x64, AC30M1x32 Datasheet

32-bit Cortex-M0 based
Programmable Motor Controller

Datasheet Version 1.01

Features

Core

- Maximum operating frequency: 40MHz
- 32-bit ARM Cortex-M0

Memory

- 64KB/32KB code flash memory
- 4KB SRAM

Clock, reset and power management

- Two main operating clocks: HCLK, PCLK
- Two system reset: cold reset, warm reset
- Power management mode: Run mode, Stop mode

Interrupt management

- Nested Vector Interrupt Controller (NVIC)

Timers

- Watchdog Timer
- 32-bit free-run timer(FRT)
- 4 general purpose timers
  - Periodic, one-shot, PWM, capture mode

Communication interfaces

- 2 UARTs, 1 I2C, 1 SPI

Motor Pulse-Width Modulation

- MPWM generators

DIV64

- 3-Phase Hardware Divider (DIV64)

ADC

- 12 analog input channels (48 PIN)

Development support

- SWD debug interface

Four types of package options

- LQFP48 (0.5mm pitch)
- LQFP32 (0.8mm pitch)
- QFN32 (0.5mm pitch)

Operating Voltage

- 2.2V to 5.5V

Operating temperature

- Commercial grade (-40℃ to +105℃)

Product selection table

Table 1. Device Summary

Device name	Flash	SRAM	UART	SPI	I2C	MPWM	ADC	I/O ports	Package
AC30M1464LBN*	64KB	4KB	2	1	1	1	12 ch.	44	LQFP-48
AC30M1364LBN	64KB	4KB	2	1	1	1	10 ch.	30	LQFP-32
AC30M1364UB*	64KB	4KB	2	1	1	1	10 ch.	30	QFN-32
AC30M1332LBN*	32KB	4KB	2	1	1	1	10 ch.	30	LQFP-32
AC30M1332UB*	32KB	4KB	2	1	1	1	10 ch.	30	QFN-32

* For available options or further information on the devices with "*" marks, please contact the ABOV sales offices.

Contents

List of figures

List of tables

1. Description

The CPU of AC30M1x64/1x32 series is based on ARM powered Cortex-M0 Core, which is composed of the ARMv6M architecture to be optimized for small size and low power system.

1.1 Device overview

In this section, features of AC30M1x64/AC30M1x32 series and peripheral counts are introduced.

Table 2. AC30M1x64/AC30M1x32 Series Features and Peripheral Counts

Peripherals		Description
Core	CPU	Maximum operating frequency: 40MHz 32-bit ARM Cortex-M0 CPU
	Interrupt	NVIC (Nested-Vectored Interrupt Controller)
Memory	Code flash	Capacity: 64Kbytes code flash memory 32Kbytes code flash memory Endurance: 10,000 cycles times at room temperature Retention: 10 years
	BOOT ROM	UART, SPI boot modes In-system programming
	SRM	4 KB
System Control Unit (SCU)	Operating frequency	40kHz ~ 40MHz External 32.768kHz crystal
	Clock	On-Chip RC-Oscillator HSI: 40MHz(±3% @-40 ~ +105℃) LSI: 40kHz(±20% @-40 ~ +105℃) XTAL OSC Fail monitoring Sub-Active mode System used external 32.768kHz crystal or system used internal 40kHz LSI
System Control Unit (SCU)	Clock monitoring	System Fail-Safe function by Clock Monitoring
	Operating mode	IDLE mode STOP1 mode STOP2 mode

Table 2. AC30M1x64/AC30M1x32 Series Features and Peripheral Counts (continued)

Peripherals		Description
System Control Unit (SCU)	Reset	nRESET pin reset Core reset Software reset POR (Power On Reset) LVR (Low Voltage Reset) WDTR (Watch Dog Timer Reset) Reset due to clock oscillating error
	LDO	Low-dropout (LDO) regulator built in for low-voltage operation
	POR	Power On Reset
	LVD	Programmable Low Voltage Detector (Brown-Out Detector)
General Purpose I/O (GPIO)		General Purpose I/O (GPIO) 44Ports (PA[15:0], PB[7:0], PC[15:0], PD[3:0]): 48-Pin 30Ports (PA[9:0], PB[7:0], PC[1:0], PC[8:7], PC[15:10], PD[3:2]): 32-Pin
TIMER	16-bit Timer	4 channels
	FRT	32-bit free-run timer 1 channels
	WDT	1 channels
Serial Interface	UART	2 channels supported
	SPI	1 channels supported
	I2C	1 channels supported
Motor Pulse-Width Modulation	MPWM	3-Phase Motor PWM with ADC triggering function
DIV64		3-Phase Hardware Divider (DIV64)
12-bit A/D Converter	ADC	3-Phase Motor PWM with ADC triggering function 12 analog input channels (48 PIN) 10 analog input channels (32 PIN)
Operating Voltage		2.2V to 5.5V
Operating temperature		Commercial grade (-40℃ to +105℃)
Package		Three types of package options 48-pin LQFP 32-pin LQFP 32-pin QFN

1.2 Block diagram

In this section, the AC30M1x64/AC30M1x32 series with peripherals is described in block diagram.

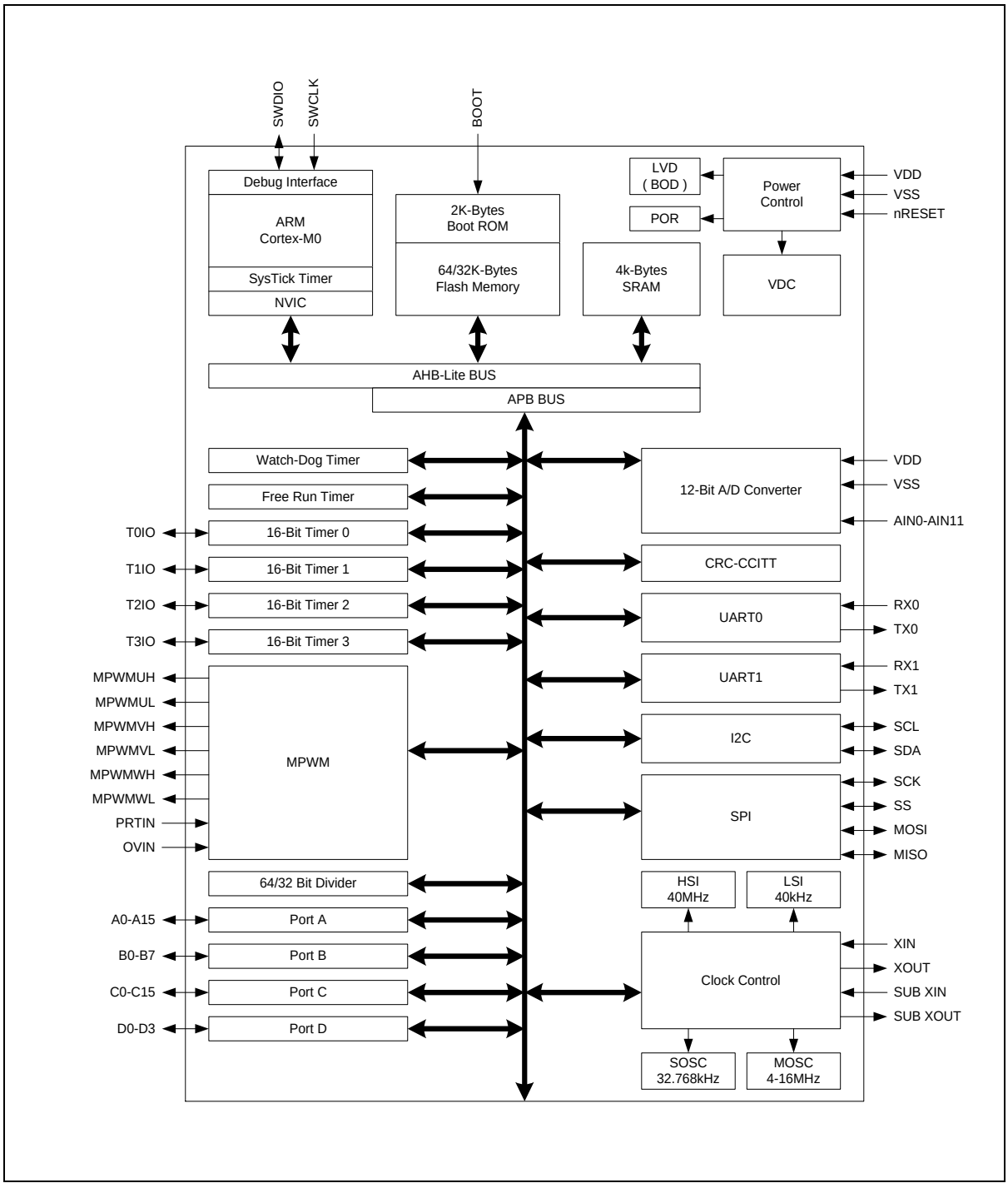


Figure 1. AC30M1x64/AC30M1x32 Block Diagram

2. Pinouts and pin descriptions

In this chapter, pinouts and pin descriptions of the AC30M1x64/AC30M1x32 series are introduced.

2.1 Pinouts

2.1.1 AC30M1464LBN (LQFP-48)

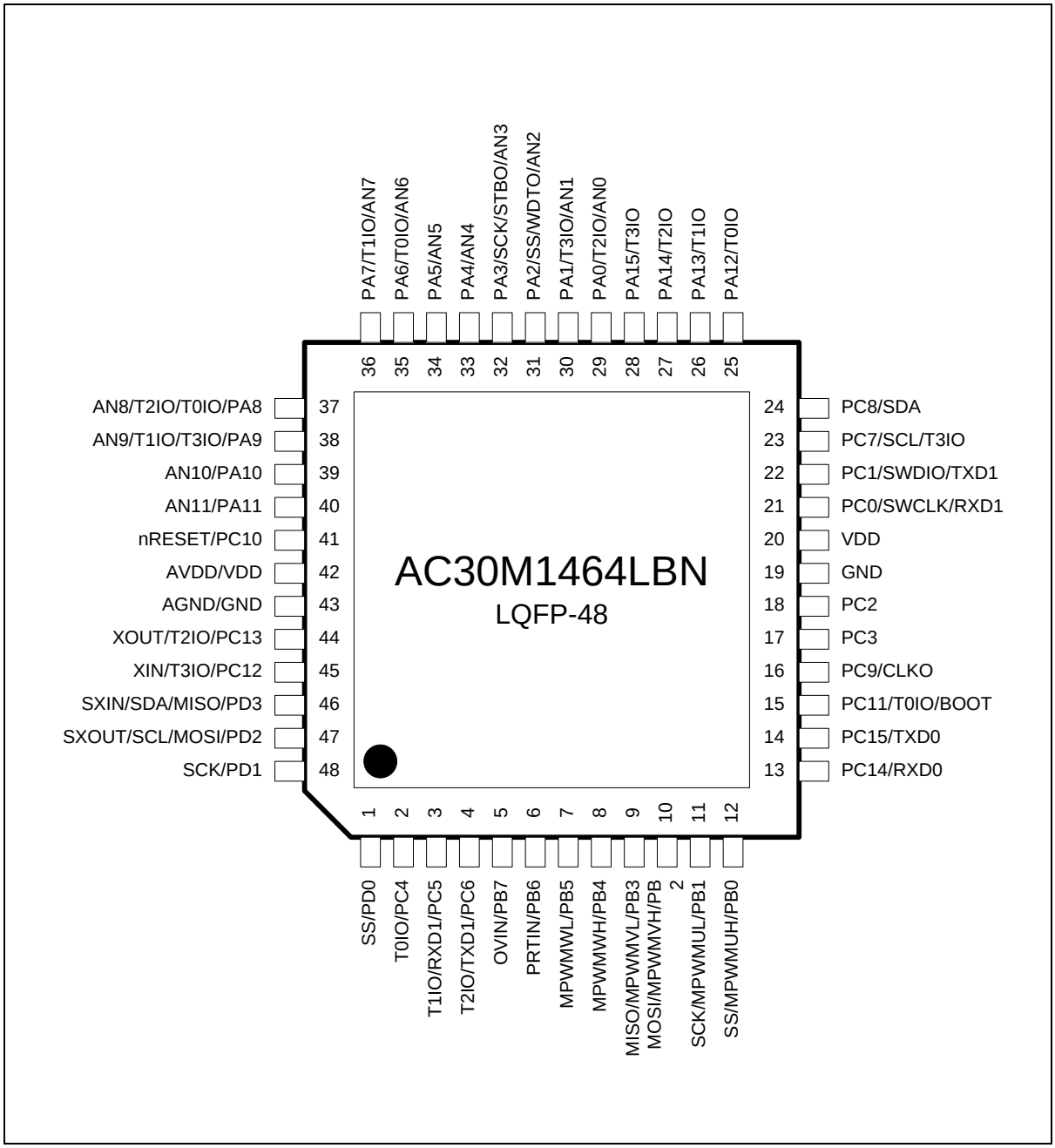


Figure 2. LQFP 48 Pinouts

2.1.2 AC30M1364LBN/AC30M1332LBN (LQFP-32)

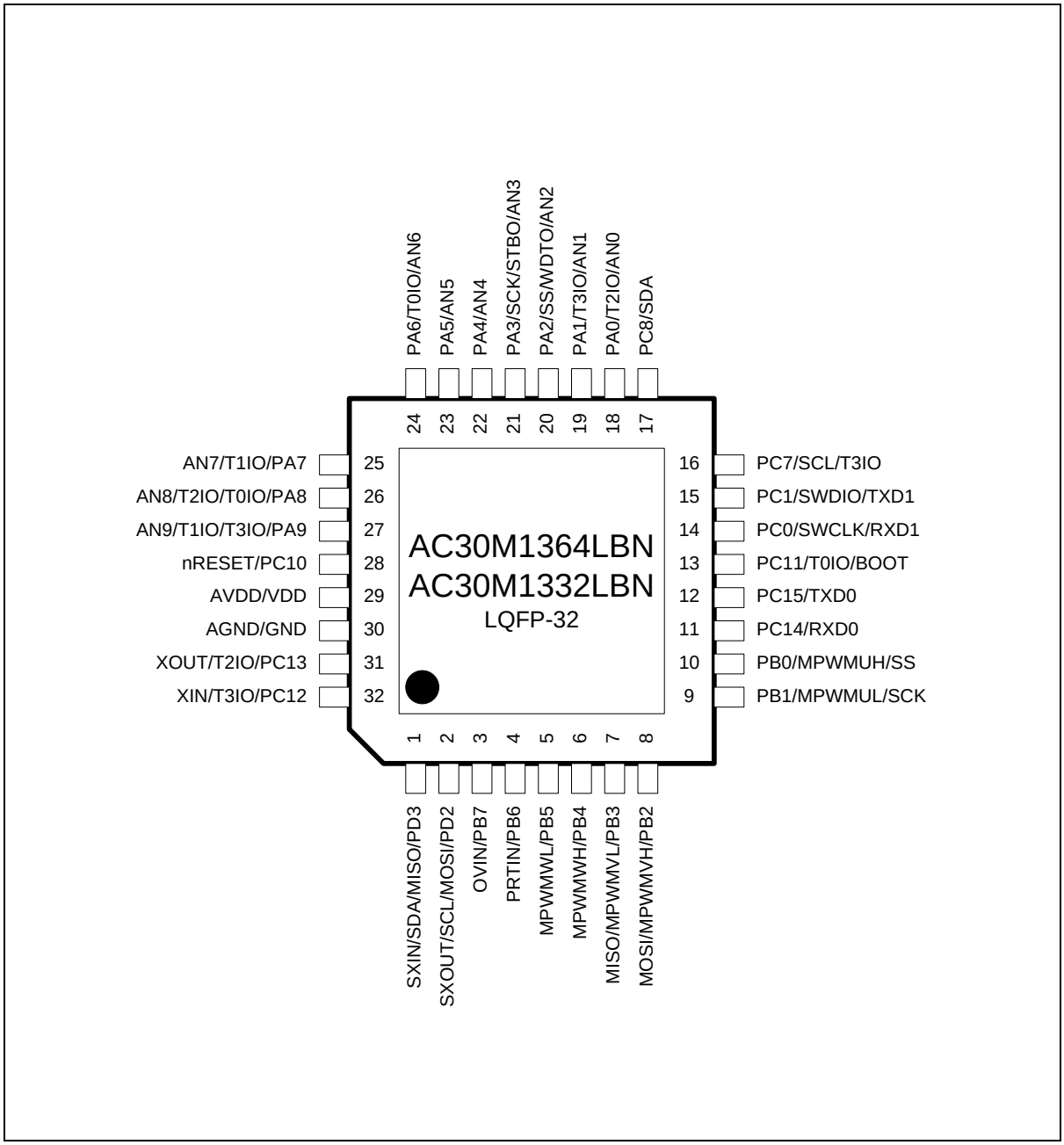


Figure 3. LQFP 32 Pinouts

2.1.3 AC30M1364UB/AC30M1332UB (QFN-32)

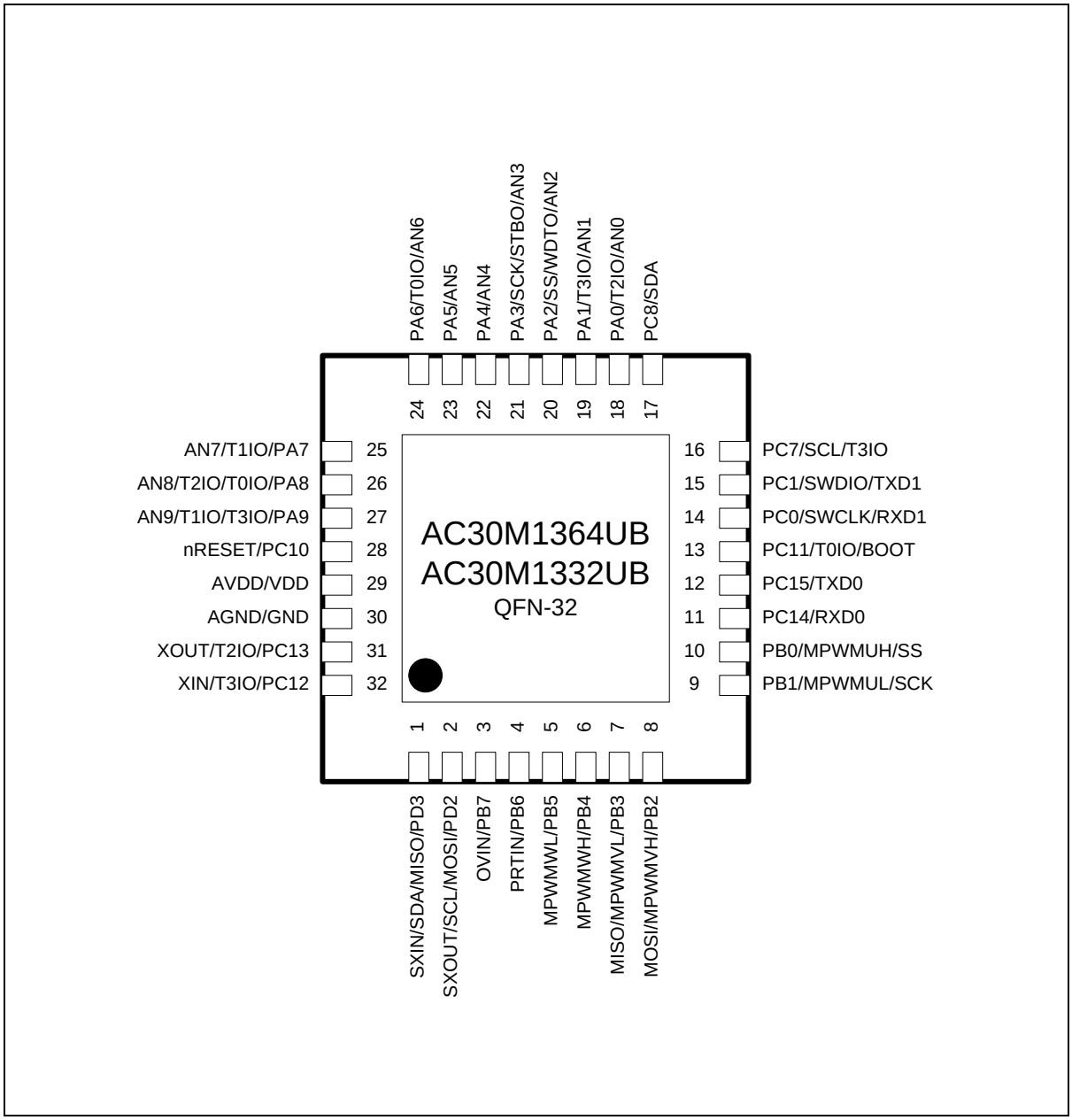


Figure 4. QFN 32 Pinouts

2.2 Pin description

Pin configuration information in Table 3 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to five selections of functions including GPIO. Configuration including pin ordering can be changed without notice.

Table 3. Pin Description

Pin number		Pin name	Type	Description	Remark
LQFP48	LQFP32 QFN32				
1	-	PD0	IOUS	PORT D Bit 0 Input/Output	
		SS	I/O	SPI Channel Slave Select In/Out	
2	-	PC4	IOUS	PORT C Bit 4 Input/Output	
		T0IO	I/O	Timer 0 Input/Output	
3	-	PC5	IOUS	PORT C Bit 5 Input/Output	
		RXD1	I	UART RXD1 Input	
		T1IO	I/O	Timer 1 Input/Output	
4	-	PC6	IOUS	PORT C Bit 6 Input/Output	
		TXD1	O	UART TXD1 Output	
		T2IO	I/O	Timer 2 Input/Output	
5	3	PB7	IOUS	PORT B Bit 7 Input/Output	
		OVIN	I	PWM Over-voltage input signal	
6	4	PB6	IOUS	PORT B Bit 6 Input/Output	
		PRTIN	I	PWM Protection Input signal	
7	5	PB5	IOUS	PORT B Bit 5 Input/Output	
		MPWMWL	O	MPWM WL Output	
8	6	PB4	IOUS	PORT B Bit 4 Input/Output	
		MPWMWH	O	MPWM WH Output	
9	7	PB3	IOUS	PORT B Bit 3 Input/Output	
		MPWMVL	O	MPWM VL Output	
		MISO	I/O	SPI Channel Master In / Slave Out	
10	8	PB2	IOUS	PORT B Bit 2 Input/Output	
		MPWMVH	O	MPWM VH Output	
		MOSI	I/O	SPI Channel Master Out / Slave In	
11	9	PB1	IOUS	PORT B Bit 1 Input/Output	
		MPWMUL	O	MPWM UL Output	
		SCK	I/O	SPI Channel CLK In / Out	

Table 3. Pin Description (continued)

Pin number		Pin name	Type	Description	Remark
LQFP48	LQFP32 QFN32				
12	10	PB0	IOUS	PORT B Bit 0 Input/Output	
		MPWMUH	O	MPWM UH Output	
		SS	I/O	SPI Channel Slave Select In / Out	
13	11	PC14	IOUS	PORT C Bit 14 Input/Output	
		RXD0	I	UART RXD0 Input	
14	12	PC15	IOUS	PORT C Bit 15 Input/Output	
		TXD0	O	UART TXD0 Output	
15	13	PC11	IOUS	PORT C Bit 11 Input/Output	
		BOOT	IU	Boot mode Selection Input	Pull-up
		T0IO	I/O	Timer 0 Input/Output	
16	-	PC9	IOUS	PORT C Bit 9 Input/Output	
		CLKO	O	System Clock Output	
17	-	PC3	IOUS	PORT C Bit 3 Input/Output	
18	-	PC2	IOUS	PORT C Bit 2 Input/Output	
19	-	GND	P	GND	
20	-	VDD	P	VDD	
21	14	PC0	IOUS	PORT C Bit 0 Input/Output	
		SWCLK	I	SWD Clock Input	Pull-up
		RXD1	I	Uart1 RXD1 Input	
22	15	PC1	IOUS	PORT C Bit 1 Input/Output	
		SWDIO	I/O	SWD Data Input/Output	Pull-up
		TXD1	O	Uart1 TXD1 Output	
23	16	PC7	IOUS	PORT C Bit 7 Input/Output	
		SCL	I/O	I2C Channel SCL In/Out	
		T3IO	I/O	Timer 3 Input/Output	
24	17	PC8	IOUS	PORT C Bit 8 Input/Output	
		SDA	I/O	I2C Channel SDA In/Out	
25	-	PA12	IOUS	PORT A Bit 12 Input/Output	
		T0IO	I/O	Timer 0 Input/Output	
26	-	PA13	IOUS	PORT A Bit 13 Input/Output	
		T1IO	I/O	Timer 1 Input/Output	
27	-	PA14	IOUS	PORT A Bit 14 Input/Output	
		T2IO	I/O	Timer 2 Input/Output	

Table 3. Pin Description (continued)

Pin number		Pin name	Type	Description	Remark
LQFP48	LQFP32 QFN32				
28	-	PA15	IOUS	PORT A Bit 15 Input/Output	
		T3IO	I/O	Timer 3 Input/Output	
29	18	PA0	IOUS	PORT A Bit 0 Input/Output	
		T2IO	I/O	Timer 2 Input/Output	
		AIN0	IA	Analog Input 0	
30	19	PA1	IOUS	PORT A Bit 1 Input/Output	
		T3IO	I/O	Timer 3 Input/Output	
		AIN1	IA	Analog Input 1	
31	20	PA2	IOUS	PORT A Bit 2 Input/Output	
		SS	I/O	SPI Channel Slave Select In / Out	
		WDTO	O	Watchdog Timer Overflow Output	
		AIN2	IA	Analog Input 2	
32	21	PA3	IOUS	PORT A Bit 3 Input/Output	
		SCK	I/O	SPI Channel CLK In / Out	
		STBO	O	Power Down Mode Output	
		AIN3	IA	Analog Input 3	
33	22	PA4	IOUS	PORT A Bit 4 Input/Output	
		AIN4	IA	Analog Input 4	
34	23	PA5	IOUS	PORT A Bit 5 Input/Output	
		AIN5	IA	Analog Input 5	
35	24	PA6	IOUS	PORT A Bit 6 Input/Output	
		T0IO	I/O	Timer 0 Input/Output	
		AIN6	IA	Analog Input 6	
36	25	PA7	IOUS	PORT A Bit 7 Input/Output	
		T1IO	I/O	Timer 1 Input/Output	
		AIN7	IA	Analog Input 7	
37	26	PA8	IOUS	PORT A Bit 8 Input/Output	
		T2IO	I/O	Timer 2 Input/Output	
		T0IO	I/O	Timer 0 Input/Output	
		AIN8	IA	Analog Input 8	
38	27	PA9	IOUS	PORT A Bit 9 Input/Output	
		T3IO	I/O	Timer 3 Input/Output	
		T1IO	I/O	Timer 1 Input/Output	

Table 3. Pin Description (continued)

Pin number		Pin name	Type	Description	Remark
LQFP48	LQFP32 QFN32				
		AIN9	IA	Analog Input 9	
39	-	PA10	IOUS	PORT A Bit 10 Input/Output	
		AIN10	IA	Analog Input 10	
40	-	PA11	IOUS	PORT A Bit 11 Input/Output	
		AIN11	IA	Analog Input 11	
41	28	PC10	IOUS	PORT C Bit 10 Input/Output	
		nRESET	IU	External Reset Input	Pull-up
42	29	VDD	P	VDD	
43	30	GND	P	GND	
44	31	PC13	IOUS	PORT C Bit 13 Input/Output	
		T2IO	I/O	Timer 2 Input/Output	
		XOUT	OA	External Crystal Oscillator Output	
45	32	PC12	IOUS	PORT C Bit 12 Input/Output	
		T3IO	I/O	Timer 3 Input/Output	
		XIN	IA	External Crystal Oscillator Input	
46	1	PD3	IOUS	PORT D Bit 3 Input/Output	
		MISO	I/O	SPI Channel Master In / Slave Out	
		SDA	I/O	I2C Channel SDA In/Out	
		SXIN	I	External Crystal Sub Oscillator Input	
47	2	PD2	IOUS	PORT D Bit 2 Input/Output	
		MOSI	I/O	SPI Channel Master Out / Slave In	
		SCL	I/O	I2C Channel SCL In/Out	
		SXOUT	OA	External Crystal Sub Oscillator Output	
48	-	PD1	IOUS	PORT D Bit 1 Input/Output	
		SCK	I/O	SPI Clock Input/Output	

NOTES:

1. I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. Pin order may be changed with revision notice

3. System and memory overview

3.1 System architecture

Main system of AC30M1x64/AC30M1x32 series consists of the following parts:

- ARM® Cortex® -M0 core
- Internal SRAM, Flash memory

3.1.1 Cortex-M0 core

The ARM® powered Cortex-M0 Core is based on ARMv6M architecture which is optimized for small size and low power system. On core system timer (SYSTICK) provides a simple 24-bit timer easy to manage the system operation Thumb-compatible Thumb-2 only instruction set processor core makes code high-density. Hardware division and single-cycle multiplication is present.

Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling. SWD debugging features are provided. Max 40MHz operating frequency has one wait execution.

3.1.2 Interrupt controller

Table 4. Interrupt Vector Map

Priority	Vector address	Interrupt source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Handler
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	MemManage Handler
-11	0x0000_0014	BusFault Handler
-10	0x0000_0018	UsageFault Handler
-9	0x0000_001C	Reserved
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Debug Monitor Handler
-3	0x0000_0034	Reserved
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler
0	0x0000_0040	LVDFAIL

Table 4. Interrupt Vector Map (continued)

Priority	Vector address	Interrupt source
1	0x0000_0044	SYSCLKFAIL
2	0x0000_0048	MOSCFAIL
3	0x0000_004C	SOSCFAIL
4	0x0000_0050	WDT
5	0x0000_0054	TIMER0
6	0x0000_0058	TIMER1
7	0x0000_005C	TIMER2
8	0x0000_0060	TIMER3
9	0x0000_0064	FRT
10	0x0000_0068	GPIOAE
11	0x0000_006C	GPIOAO
12	0x0000_0070	GPIOBE
13	0x0000_0074	GPIOBO
14	0x0000_0078	GPIOCE
15	0x0000_007C	GPIOCO
16	0x0000_0080	GPIODE
17	0x0000_0084	GPIODO
18	0x0000_0088	MPWM
19	0x0000_008C	MPWMPROT
20	0x0000_0090	MPWMOVV
21	0x0000_0094	I2C
22	0x0000_0098	SPI
23	0x0000_009C	UART0
24	0x0000_00A0	UART1
25	0x0000_00A4	ADC
26	0x0000_00A8	Reserved
27	0x0000_00AC	
28	0x0000_00B0	
29	0x0000_00B4	
30	0x0000_00B8	
31	0x0000_00BC	

NOTES:

1. Each interrupt has an associated priority-level register. Each of them is 2 bits wide, occupying the two MSBs of the Interrupt Priority Level Registers. Each Interrupt Priority Level Register occupies 1 byte (8 bits). NVIC registers in the Cortex-M0 processor can only be accessed using word-size transfers, so for each access, four Interrupt Priority Level Registers are accessed at the same time.
2. __NVIC_PRIO_BITS = 2

3.2 Memory organization

Program memory, data memory, registers and I/O ports are organized in the same address space.

3.2.1 Memory map

Figure 5 shows addressable memory space in memory map.

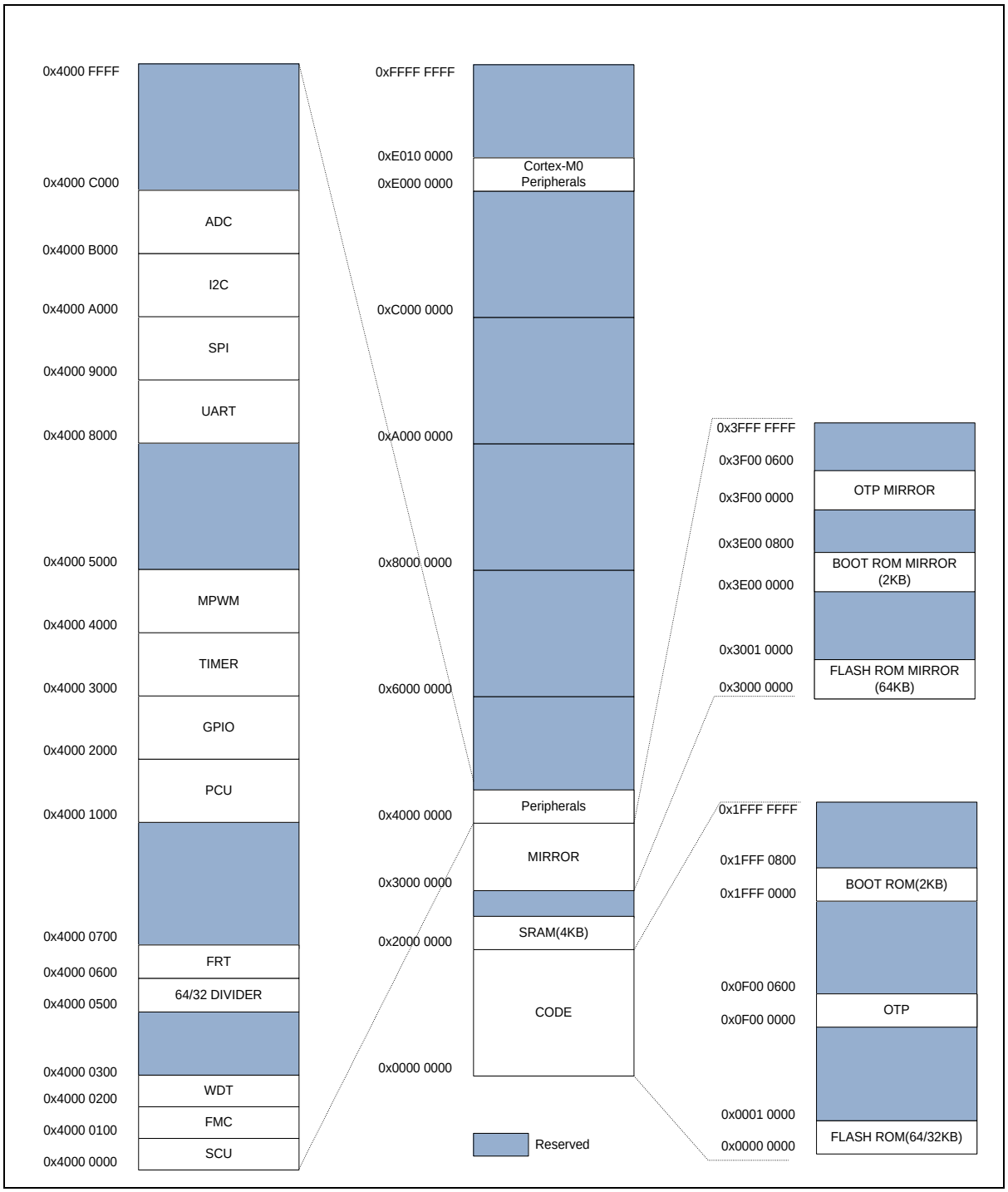


Figure 5. Memory Map

3.2.2 Embedded SRAM

On chip 4KB 0-wait SRAM can be used for working memory space and program code can be loaded on this SRAM.

3.2.3 Flash memory overview

The AC30M1x64/1x32 provides internal 64/32KB code flash memory and its controller. This is enough to program motor algorithm and general control the system. Self-programming is available and ISP and SWD programming is also supported in boot or debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory. The CPU can access flash memory with one wait state up to 40 MHz bus frequency.

3.3 Boot mode

3.3.1 Boot mode pins

The AC30M1x64/AC30M1x32 series has a boot mode option to program internal flash memory. Boot mode can be entered by setting BOOT pin to ‘L’ at reset timing (Normal state is ‘H’).

Boot mode supports both of UART/SPI boot:

- UART boot and SPI boot uses TXD0/RXT0 ports.

Pins for the boot mode are listed in Table 5.

Table 5. Boot Mode Pin List

Block	Pin name	Dir	Description
SYSTEM	nRESET/PC10	I	Reset input signal
	nBOOT/PC11	I	Boot mode setting pin
UART0	RXD0/PC14	I	UART boot receive data
	TXD0/PC15	O	UART boot transmit data
SPI	SS/PA2	I	SPI Boot Slave Select
	SCK/PA3	I	SPI Boot Clock Input
	MOSI/PD2	I	SPI Boot Data Input
	MISO/PD3	O	SPI Boot Data Output

3.3.2 Boot mode connections

Users can design a target board using any of boot mode ports such as UART mode of UART0. Sample connection diagrams of boot mode are introduced in the following figures:

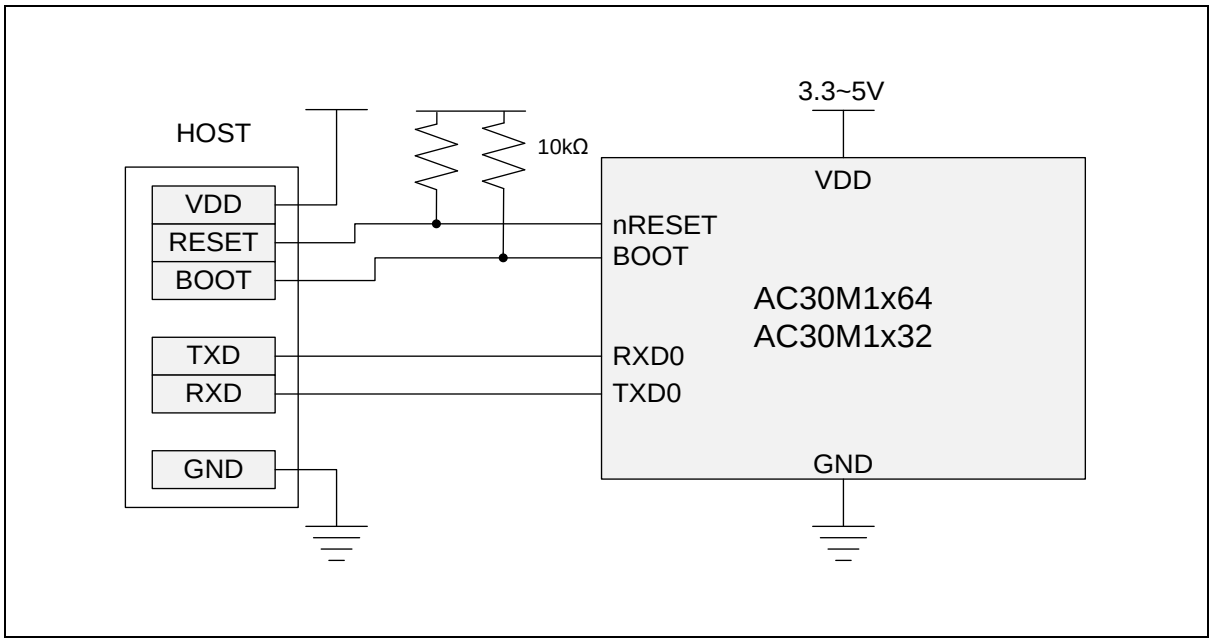


Figure 6. Connection Diagram of UART0 Boot

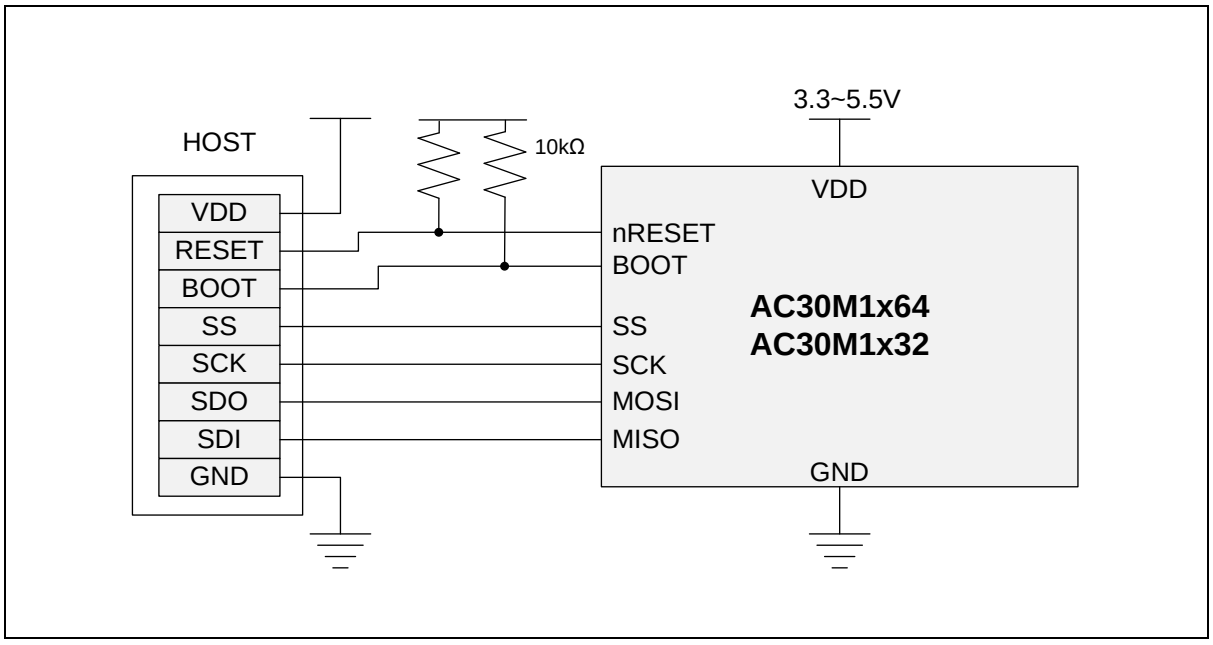


Figure 7. Connection Diagram of SPI Boot

3.3.3 SWD mode connections

Users can use SWD mode for writing with E-PGM+. This mode can be used for writing & debugging.

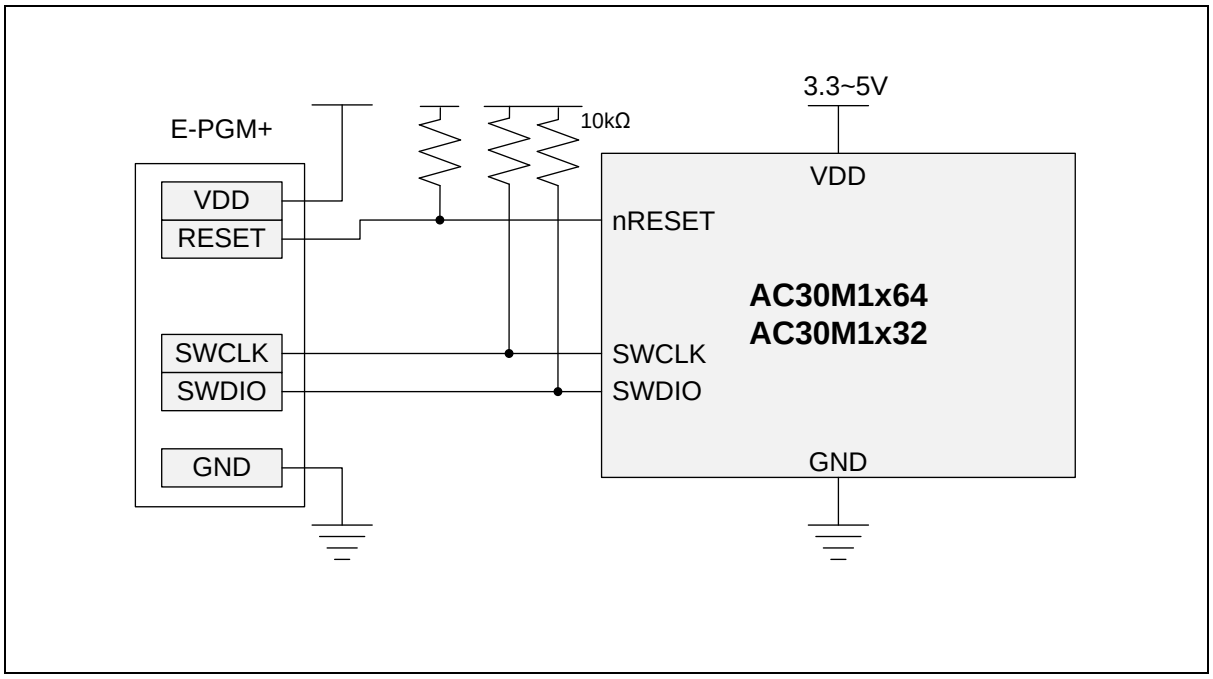


Figure 8. Connection Diagram of E-PGM+ and SWD Port

4. System Control Unit (SCU)

AC30M1x64/AC30M1x32 series has a built-in intelligent power control block which manages system analog blocks and operating modes. System control unit (SCU) block controls an internal reset and clock signals to maintain optimize system performance and power dissipation.

Four pins in Table 6 are assigned for SCU block

Table 6. SCU Pins

Pin name	Type	Description
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator
SXIN/SXOUT	OSC	External sub-Crystal Oscillator
STBO	O	Stand-by Output Signal
CLKO	O	Clock Output Monitoring Signal

4.1 SCU block diagram

In this subsection, SCU block diagram is introduced in Figure 9.

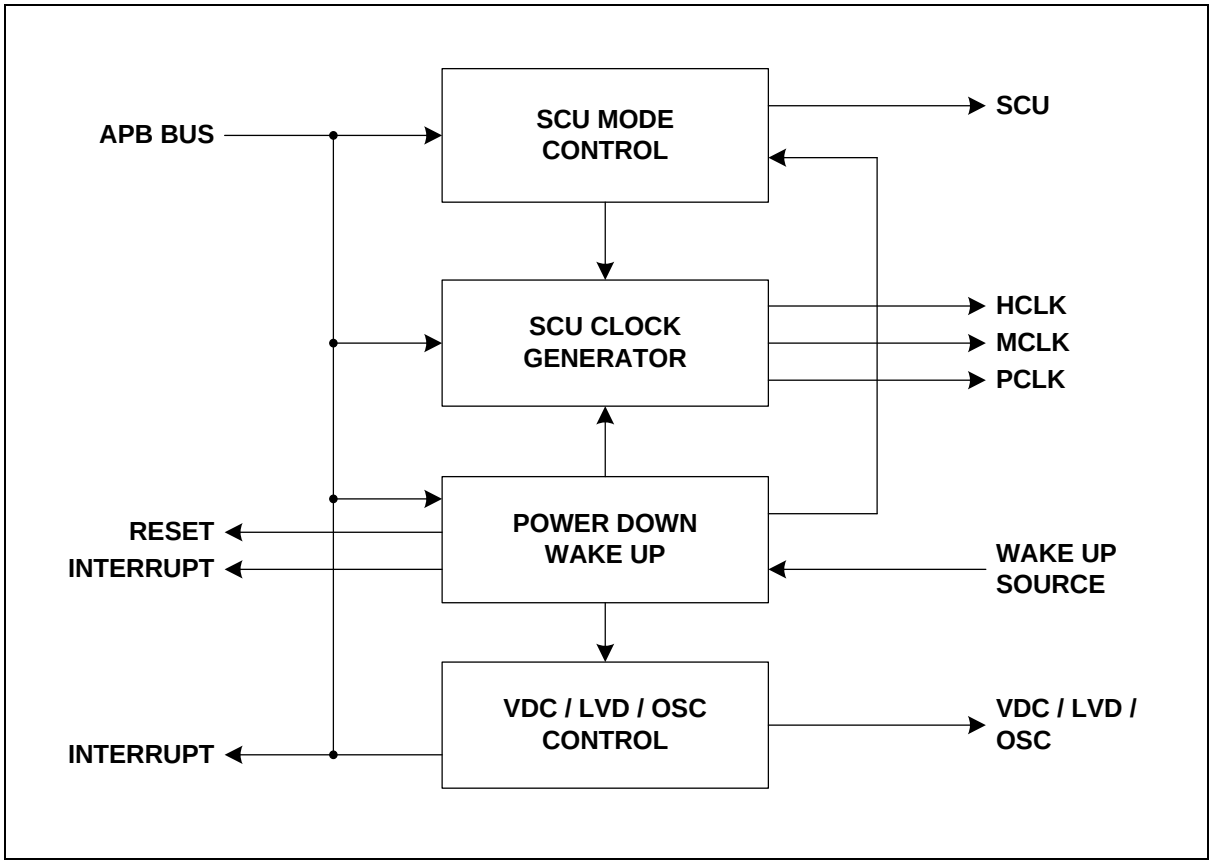


Figure 9. SCU Block Diagram

4.2 Clock system

AC30M1x64/AC30M1x32 series has two main operating clocks. One is HCLK which produces a clock signal both for CPU and AHB bus system. The other is PCLK which produces a clock signal for peripheral systems.

A user can keep the clock system variation under software control. Through Figure 10 and Table 7, users learn about the clock system of AC30M1x64/AC30M1x32 devices and clock sources.

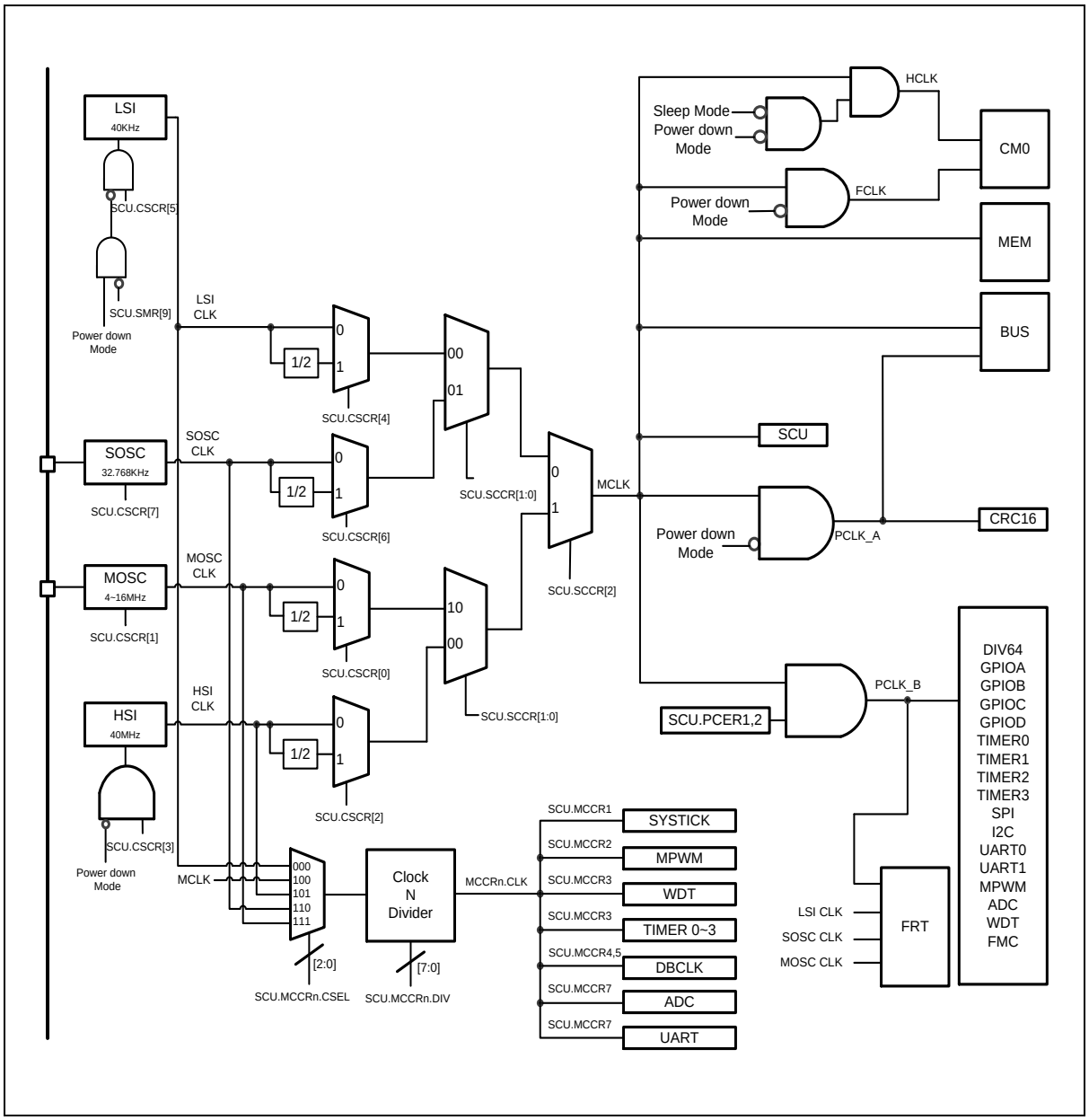


Figure 10. Clock Tree Configuration

All multiplexers switching clock sources have a glitch-free circuit in each. So a clock can be switched without glitch risks. When a user tries to change a clock mux control, both of clock sources must be alive. If one of them is not alive, clock change operation is stopped and system will be halted and not be recovered.

Table 7. Clock Sources

Clock name	Frequency	Description
MOSC	4-16 MHz	External Crystal OSC
SOSC	32.768 kHz	External Sub Crystal OSC
HSI	40 MHz	High Speed Internal OSC
LSI	40 kHz	Low Speed Internal OSC

4.2.1 Configuration of miscellaneous clocks

HCLK clock domain

HCLK clock feeds the clock to the CPU and AHB bus. Cortex-M0 CPU requires 2 clocks related with HCLK clock. FCLK and HCLK. FCLK is free running clock and it is always running except power down mode. HCLK can be stopped in the sleep mode and power down mode.

BUS system and memory systems operated by MCLK clock. Max bus operating clock speed is 40MHz.

PCLK clock domain

PCLK_B is master clock of all the peripheral. Each peripheral clocks enabled by SCU.PCER1 and SCU.PCER2 registers can be used by each peripheral. Before enabling the PCLK_B input clock of each block, it can't be accessible even reading its registers. In the case of FRT, various clocks can be used. But CRC16 uses PCLK_A. It can be stopped in power down mode.

Clock configuration procedure

After power up, the default system clock is feed by LSI (40kHz) clock. LSI is default enabled at power up sequence. The other clock sources will be enabled by user controls with the LSI system clock.

HSI (40MHz) clock can be enabled by SCU.CSCR register.

MOSC (4-16MHz) clock can be enabled by SCU.CSCR register. Before enable MOSC block, the pin mux configuration should be set for XIN, XOUT function. PC12 and PC13 pins are shared with MOSC's XIN and XOUT function – PCC.MR and PCC.CR registers should be configured properly. After enabling the MOSC block, you must wait for more than 5msec time to ensure stable operation of crystal oscillation.

SOSC (32.768kHz) clock can be enabled by SCU.CSCR register. Before enable SOSC block, the pin mux configuration should be set for SXIN, SXOUT function. PD3 and PD2 pins are shared with SOSC's SXIN and SXOUT function – PCD.MR and PCD.CR registers should be configured properly. After enabling the SOSC block, you must wait for more than 10msec time to ensure stable operation of crystal oscillation.

You can change the MCLK by configuring the SCU.SCCR register. In addition, you can find an example flow chart configuring the system clock in Figure 11.

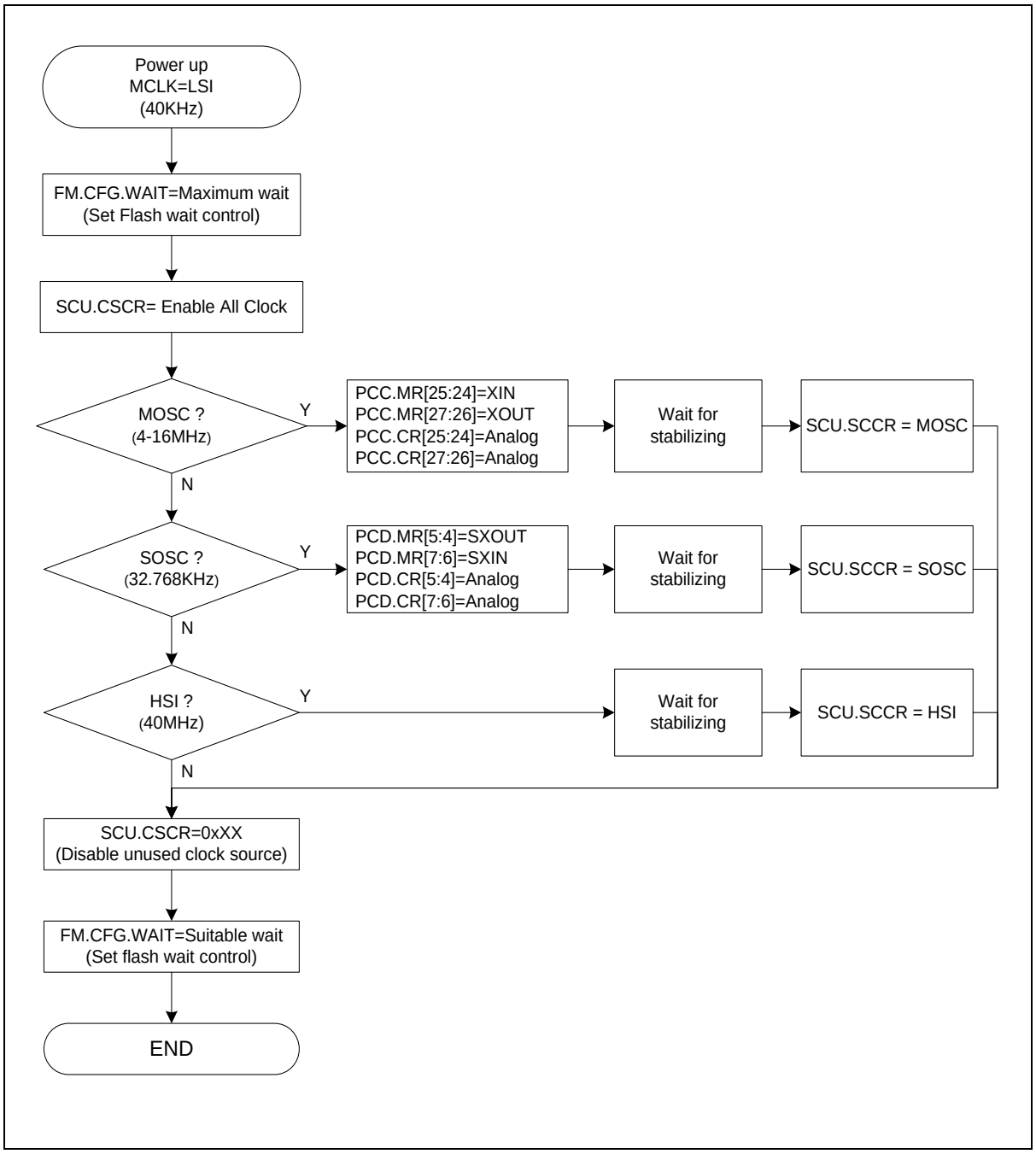


Figure 11. Clock Change Procedure

When you speed up the system clock to the maximum operating frequency, you should check flash wait control configuration. Flash read access time is one of limitation factor for performance. The wait control recommendation is suggested in Table 8.

Table 8. Flash Wait Control Recommendation

FMCONF.WAIT	FLASH access wait	Available max. system clock frequency
00	0-clock wait	Up to 20MHz
01	1-clock wait	Up to 40MHz
11	2-clock wait	Up to 40MHz

4.3 Reset

The AC30M1x64/AC30M1x32 series has two system reset options. One is a cold reset that is effective during power up or down sequence. The other is a warm reset which is generated by several reset sources. A reset event makes a chip to turn to an initial state. Reset sources of the cold reset and the warm reset are listed in Table 9.

Table 9. Reset Sources

	Reset
Reset sources	nRESET pin WDT reset LVD reset MCLK Fail reset MOSC Fail reset S/W reset CPU request reset CPU Lockup reset

4.3.1 Cold reset

The cold reset is important feature of the chip when power is up. This characteristic will globally affect the system boot. Internal VDC is enabled when VDDEXT power is turn on. Internal POR trigger level is 1.4V of VDDEXT voltage out level. At this time, boot operation is started. The LSI clock is enabled and counts 4.25msec time for internal VDC level stabilizing. In this time, VDDEXT voltage level should be over than initial LVD level (1.65V). After 4.25msec counting, the cold reset is released and counts 0.4msec time for warm reset synchronizing. After released cold and warm reset, BOOTROM and CPU are running.

Figure 12 shows the power-up process and the initial reset waveforms.

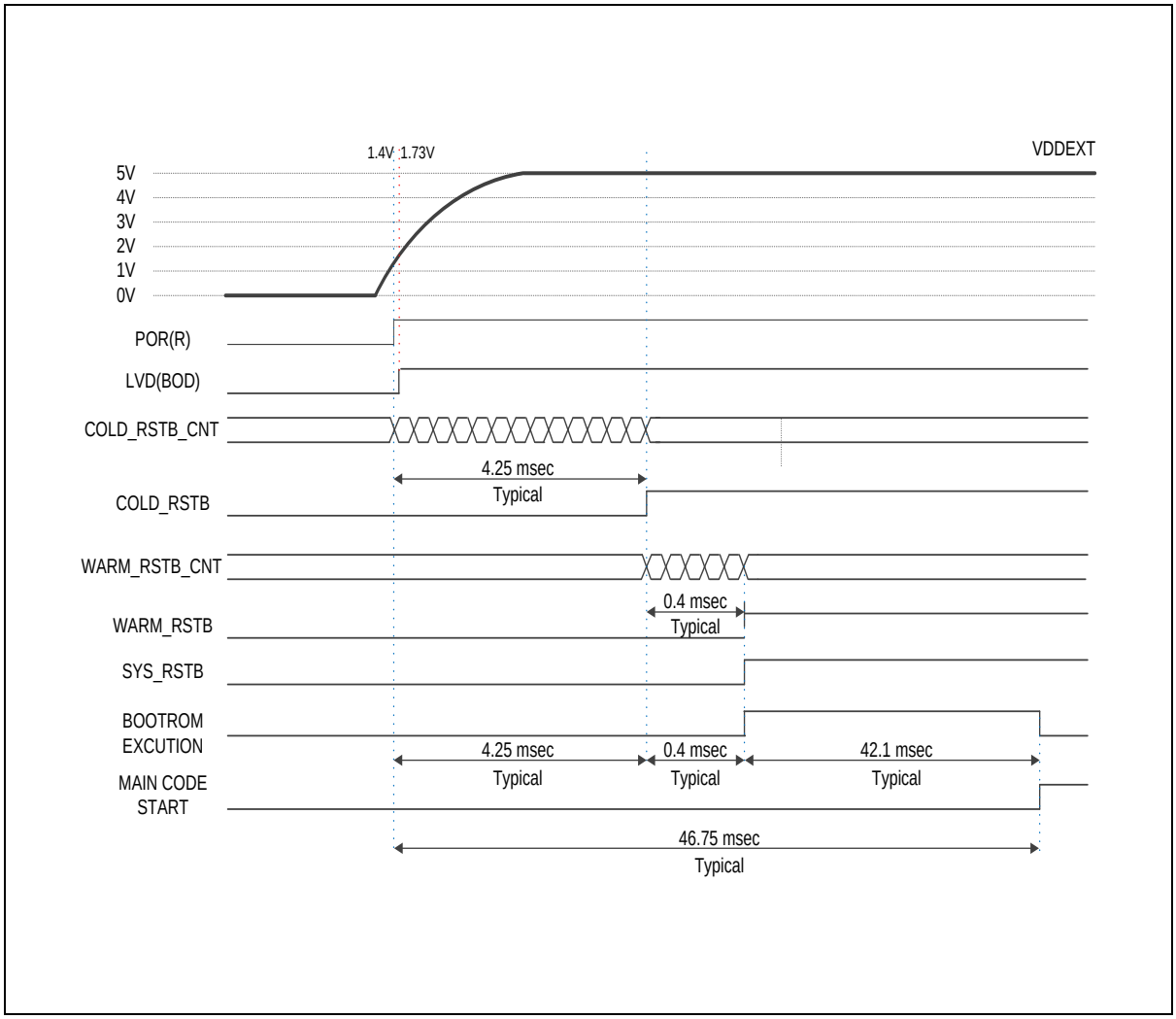


Figure 12. Power-up Procedure

4.3.2 Warm reset

The warm reset event has several reset sources and some parts of chip returns to initial state when warm reset condition is occurred.

The warm reset source is controlled by SCU.RSER register and the status is appeared in SCU.RSSR register. The reset for each peripheral blocks is controlled by SCU.PRER register. The reset can be masked independently.

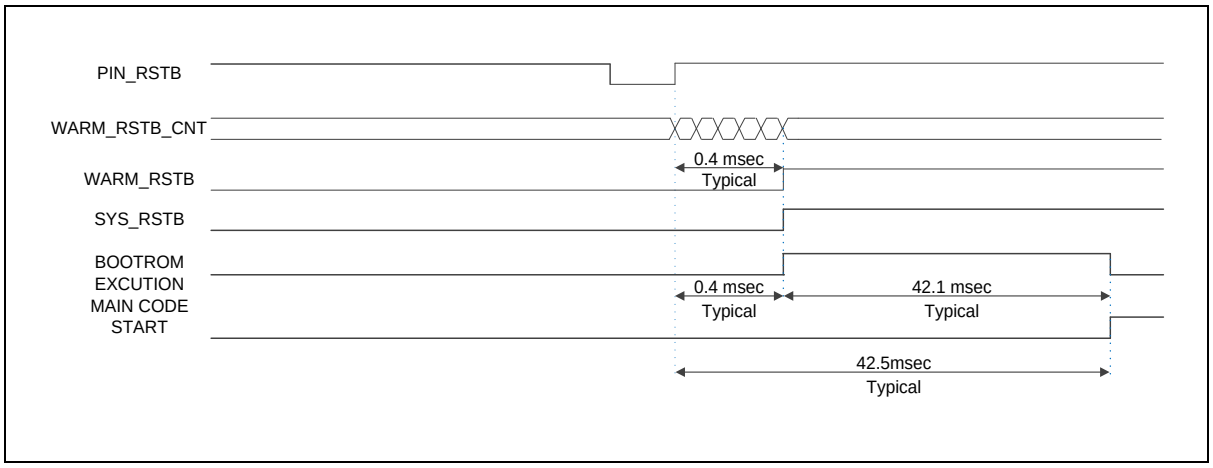


Figure 13. Warm Reset Diagram

4.3.3 LVR reset

An LVR event is triggered when the operating voltage drops below a certain level during the MCU's operation. A user can choose to set the MCU to perform a reset or an interrupt when an LVR event is triggered. This low voltage reset is a warm reset. See the description on warm resetting for details.

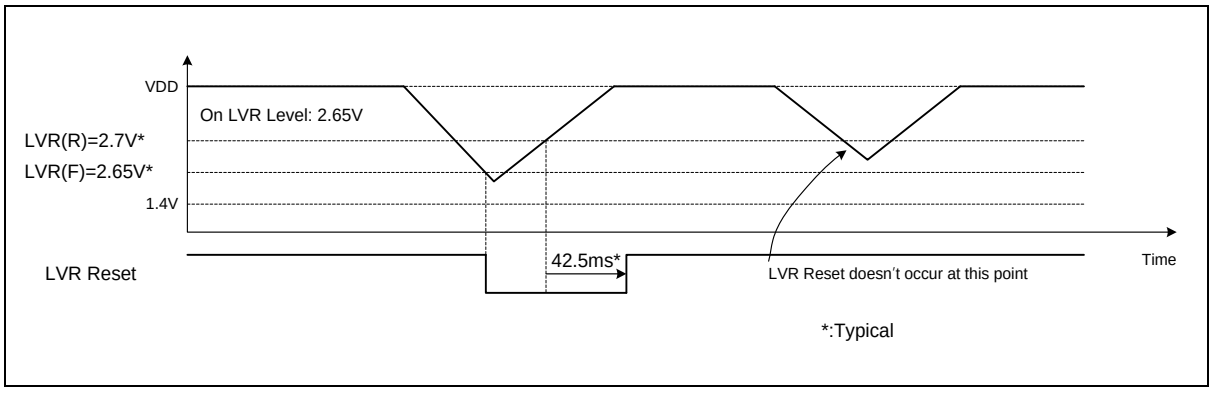


Figure 14. LVR Reset Timing Diagram

4.3.4 Reset tree

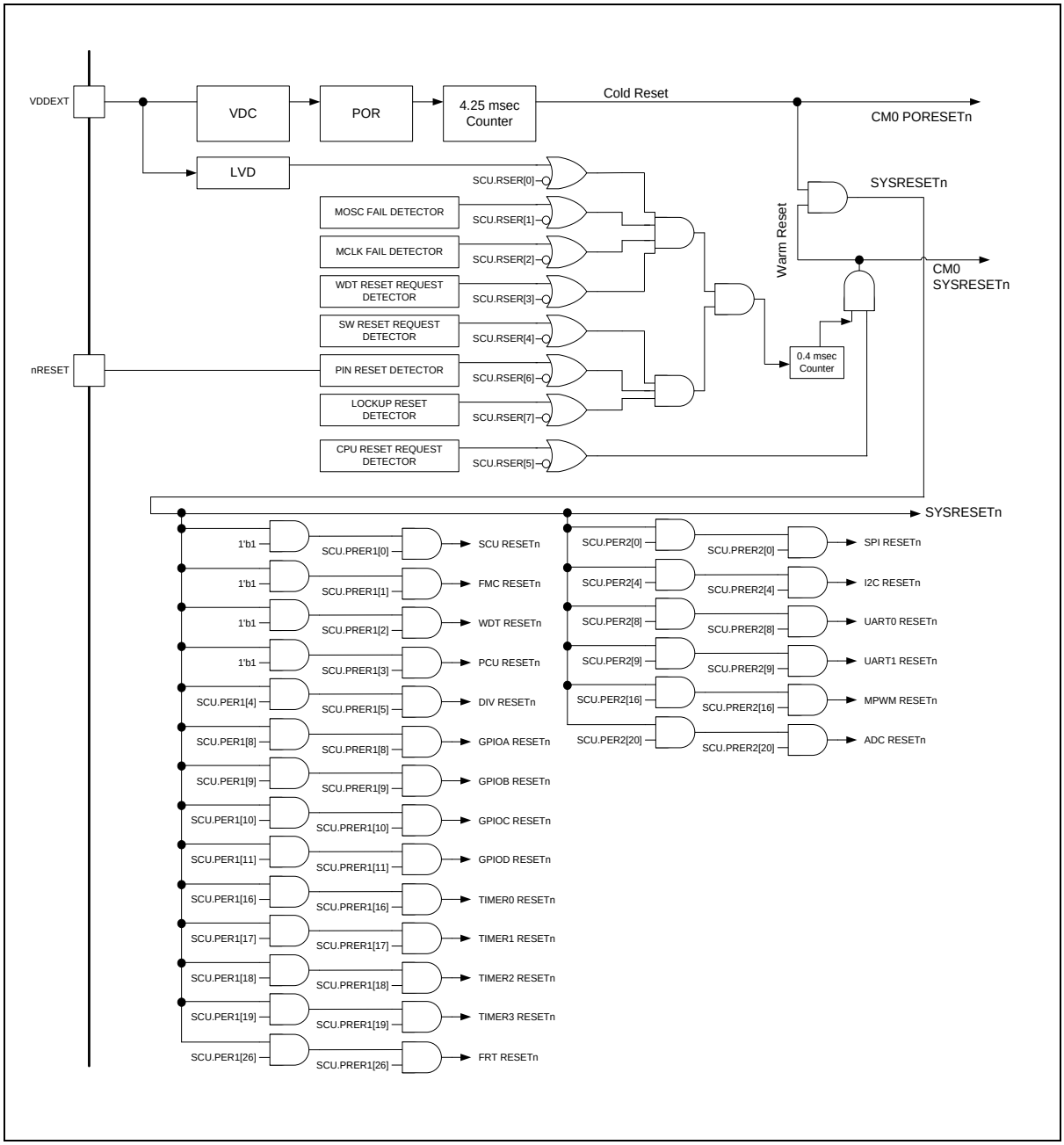
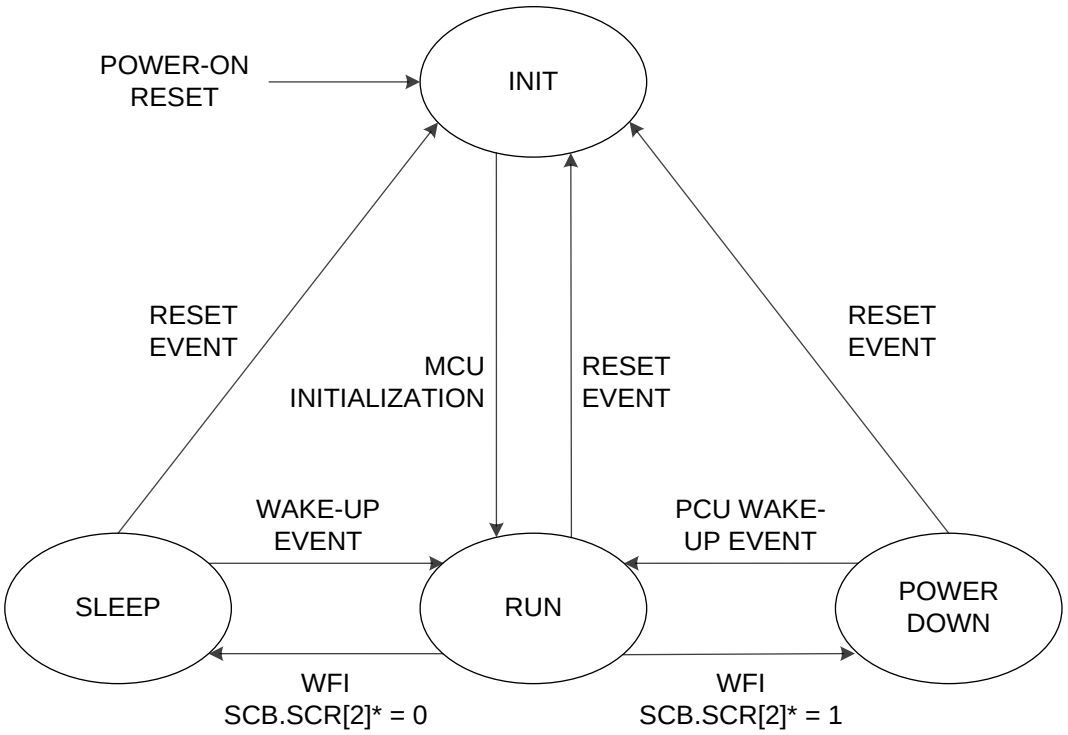


Figure 15. Reset Tree Configuration

4.4 Operation mode

The INIT mode is initial state of the chip when reset is asserted. The RUN mode is max performance of the CPU with high-speed clock system. And the SLEEP and the PD mode can be used as the low power consumption mode. The low power consumption is achieved by halting processor core and unused peripherals.

Figure 16 shows the operation mode transition diagram.



NOTE: SCB.SCR* is System Control Register in System Control Block.

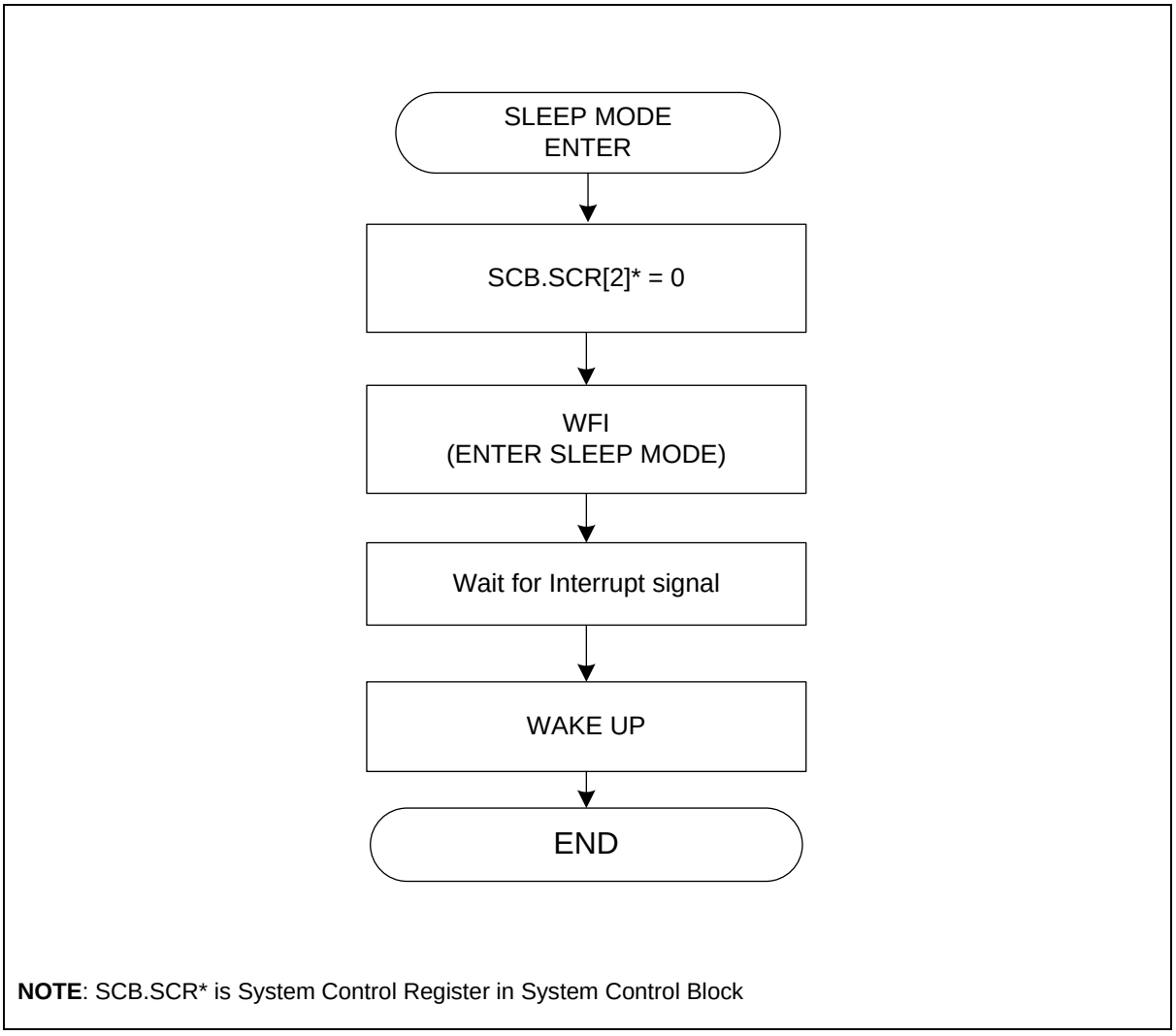
Figure 16. Transition between Operation Modes

4.4.1 RUN mode

In RUM mode, CPU and the peripheral hardware operate with a high-speed clock. After a reset followed by INIT state, the system enters in RUN mode.

4.4.2 SLEEP mode

Only the CPU is stopped in this mode. Each peripheral function can be enabled by the function enable and clock enable bit in the PER and PCER register.

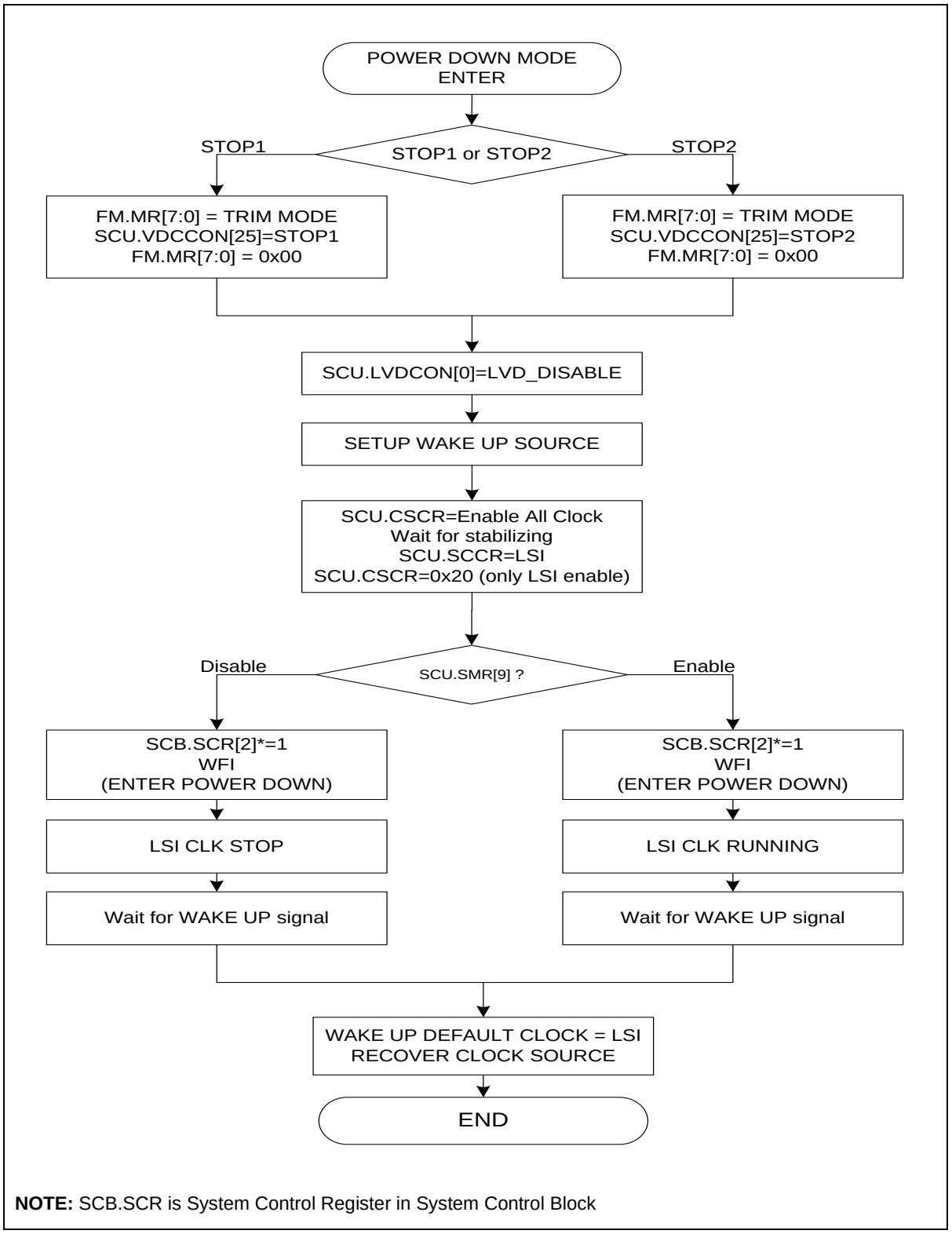


NOTE: SCB.SCR* is System Control Register in System Control Block

Figure 17. SLEEP Mode Operation Sequence

4.4.3 POWER DOWN mode

All the internal circuits are entered the stop state. Power down operation has special power off sequence as below picture.



NOTE: SCB.SCR is System Control Register in System Control Block

Figure 18. Power down Mode Operation Sequence

5. Port Control Unit (PCU)

AC30M1x64/AC30M1x32 MCU's Port Control Unit (PCU) block controls the external input and output (I/O) ports.

The PCU configures and controls external I/Os as listed in the followings:

- Set pin function mux
- Set external signal directions of each pins
- Set interrupt trigger mode for each pins
- Set internal pull-up register control and open drain control

Table 10 are assigned for PCU blocks.

Table 10. PCU Pins

Pin name	Type	Description
PA	IO	PA0 to PA15
PB	IO	PB0 to PB7
PC	IO	PC0 to PC15
PD	IO	PD0 to PD3

5.1 PCU block diagram

In this section, PCU and IP Port are described in block diagrams through Figure 19, Figure 20, and Figure 21.

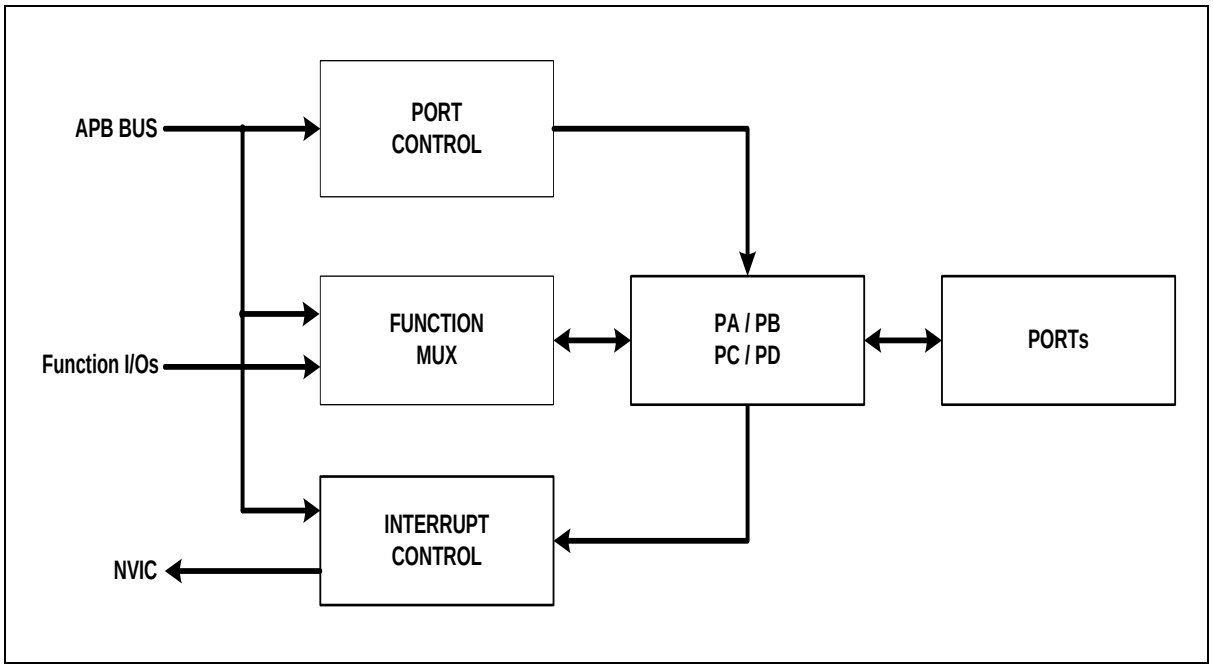


Figure 19. PCU Block Diagram

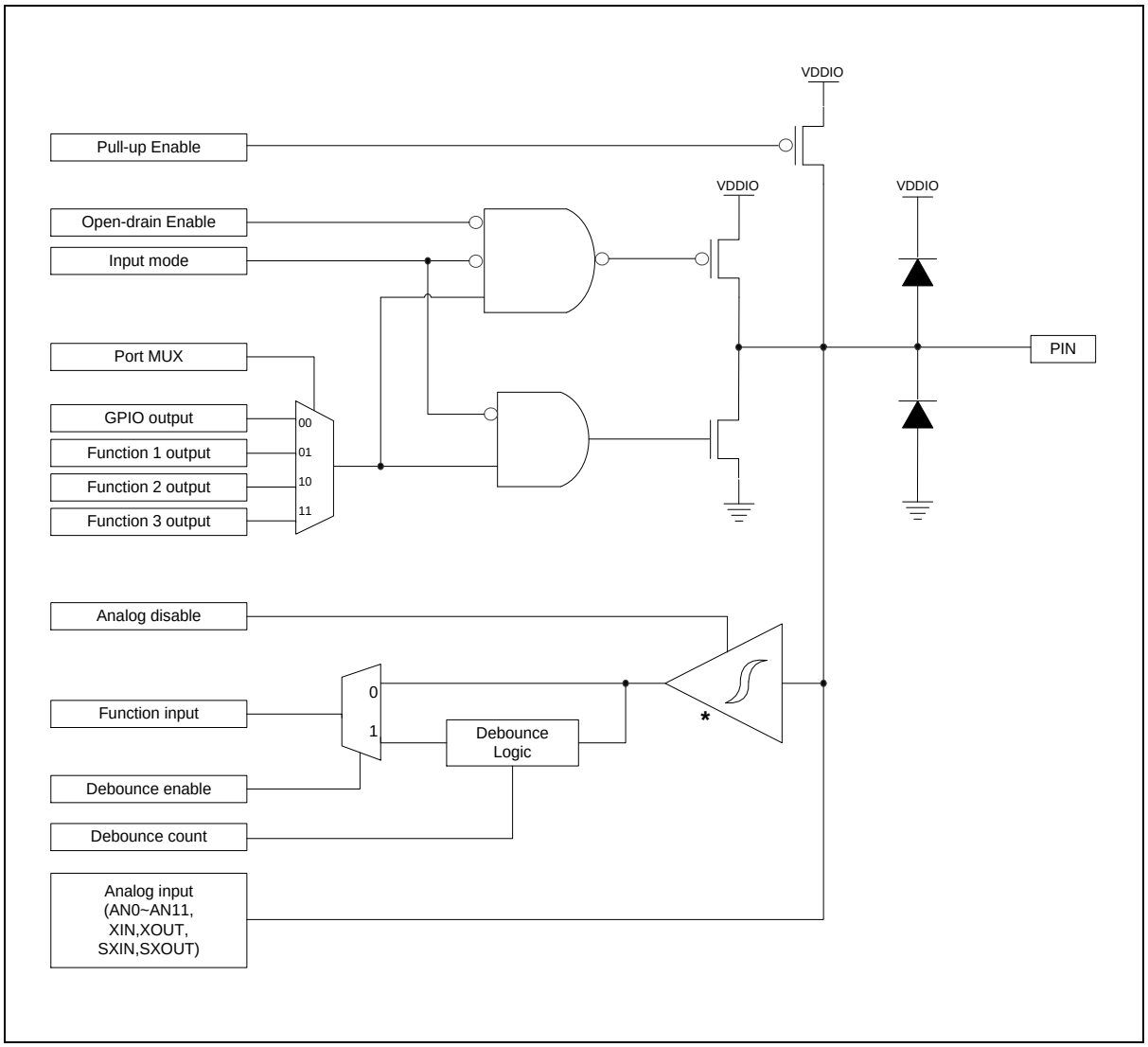


Figure 20. I/O Port Block Diagram (ADC and External Oscillator Pins)

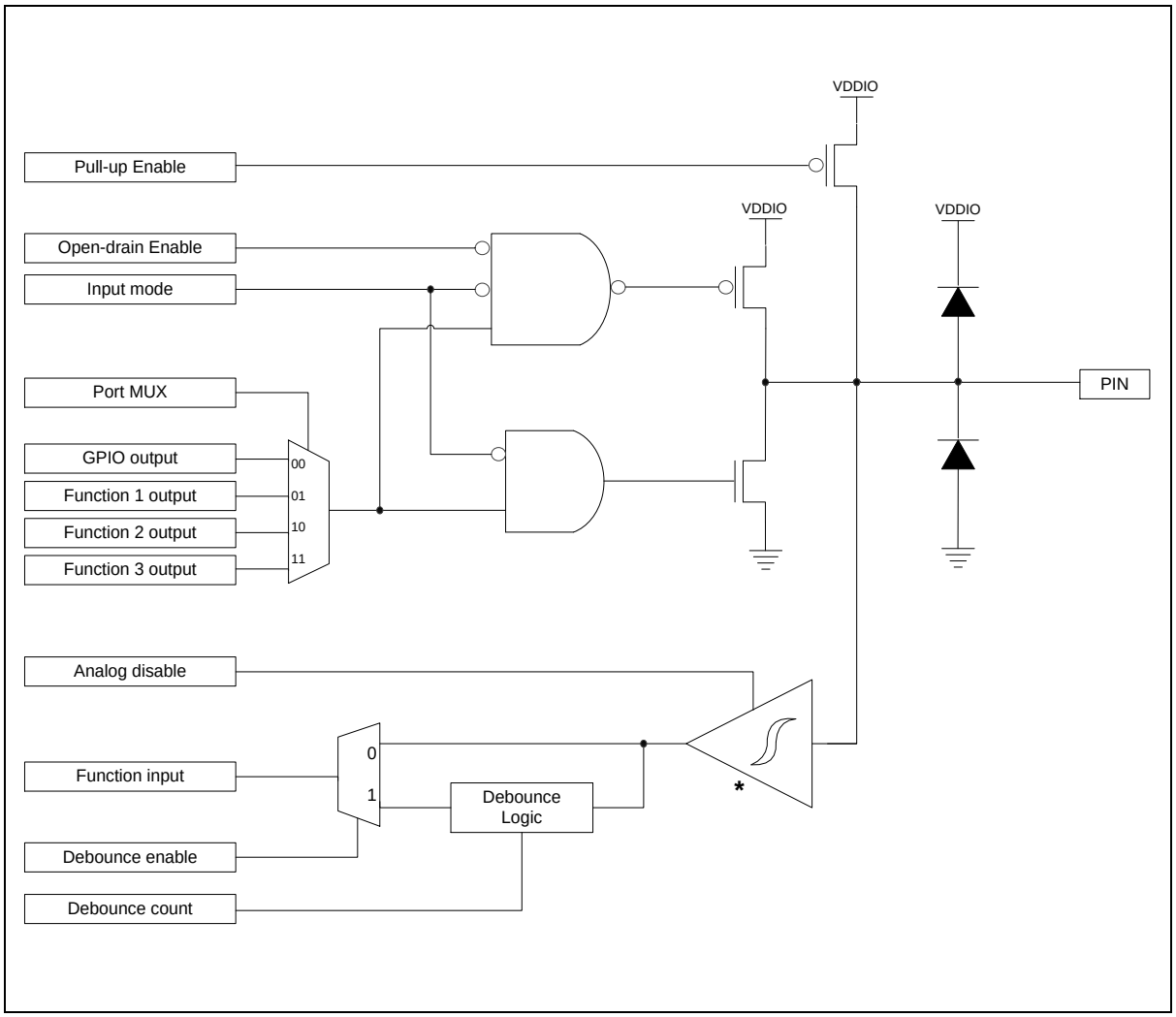


Figure 21. I/O Port Block Diagram (General I/O pins)

5.2 Pin multiplexing

GPIO pins have alternative function pins. Table 11 shows pin multiplexing information.

Table 11. GPIO Alternative Function

Pin name	Alternative function			
	00	01	10	11
PA0	PA0*	T2IO		AIN0
PA1	PA1*	T3IO		AIN1
PA2	PA2*	SS	WDTO	AIN2
PA3	PA3*	SCK	STBO	AIN3
PA4	PA4*			AIN4
PA5	PA5*			AIN5
PA6	PA6*	T0IO		AIN6
PA7	PA7*	T1IO		AIN7
PA8	PA8*	T2IO	T0IO	AIN8
PA9	PA9*	T3IO	T1IO	AIN9
PA10	PA10*			AIN10
PA11	PA11*			AIN11
PA12	PA12*	T0IO		
PA13	PA13*	T1IO		
PA14	PA14*	T2IO		
PA15	PA15*	T3IO		
PB0	PB0*	MPWMUH	SS	
PB1	PB1*	MPWMUL	SCK	
PB2	PB2*	MPWMVH	MOSI	
PB3	PB3*	MPWMVL	MISO	
PB4	PB4*	MPWMWH		
PB5	PB5*	MWMWL		
PB6	PB6*	PRTIN		
PB7	PB7*	OVIN		
PB8				
PB9				
PB10				
PB11				
PB12				
PB13				

Table 14. GPIO Alternative Function (continued)

Pin name	Alternative function			
	00	01	10	11
PB14				
PB15				
PC0	PC0	SWCLK*	RXD1	
PC1	PC1	SWDIO*	TXD1	
PC2	PC2*			
PC3	PC3*			
PC4	PC4*		T0IO	
PC5	PC5*	RXD1	T1IO	
PC6	PC6*	TXD1	T2IO	
PC7	PC7*	SCL	T3IO	
PC8	PC8*	SDA		VMRG
PC9	PC9*	CLKO		
PC10	PC10	nRESET*		
PC11	PC11	BOOT*	T0IO	
PC12	PC12*	T3IO		XIN
PC13	PC13*	T2IO		XOUT
PC14	PC14*	RXD0		
PC15	PC15*	TXD0		
PD0	PD0*	SS		
PD1	PD1*	SCK		
PD2	PD2*	MOSI	SCL	SXOUT
PD3	PD3*	MISO	SDA	SXIN

NOTE:An (*) mark indicates default pin settings.

6. General Purpose I/O (GPIO)

Most of pins except dedicated function pins can be used general I/O ports. General input/output ports are controlled by GPIO block.

GPIO ports are controlled by GPIO block as listed in the followings:

- Output signal level (H/L) selection
- Read Input signal level

Table 12 are assigned for GPIO blocks.

Table 12. GPIO Pins

Pin name	Type	Description
PA	IO	PA0 to PA15
PB	IO	PB0 to PB7
PC	IO	PC0 to PC15
PD	IO	PD0 to PD3

6.1 GPIO block diagram

Figure 22 describes GPIO in block diagram.

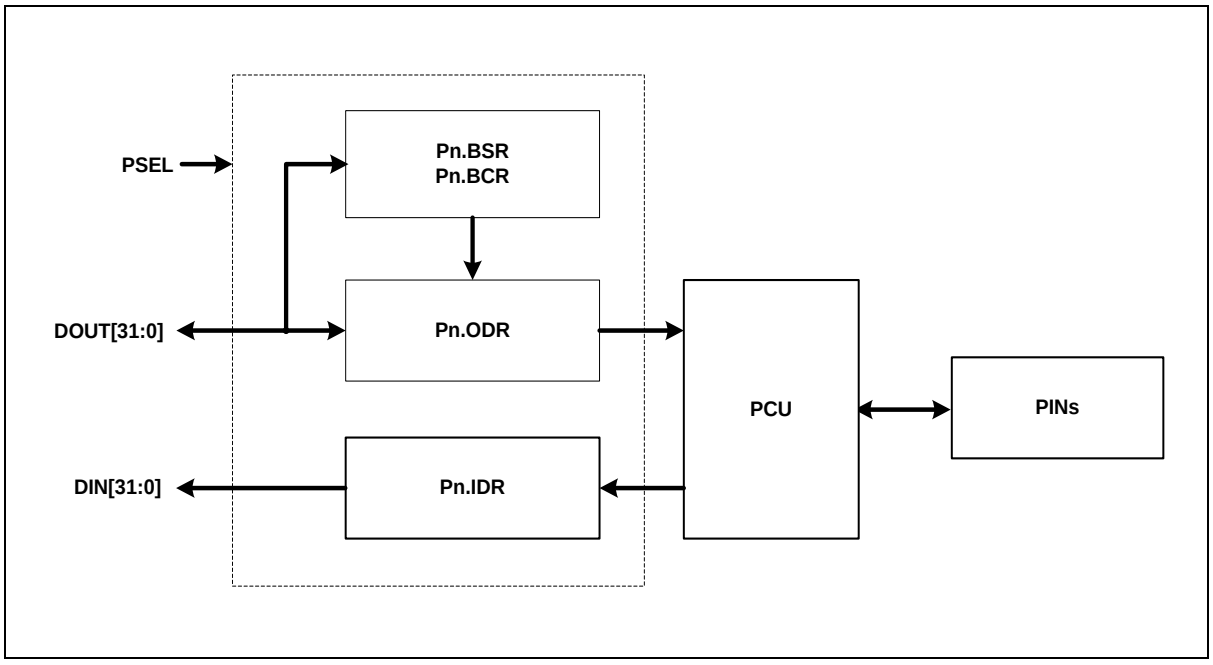


Figure 22. GPIO Block Diagram

7. Flash Memory Controller (FMC)

The flash memory controller (FMC) is an interface controller of internal flash memories:

- 64/32KB flash memory with protection bits
- 32-word length program or erase at a time
- Bulk erase for 64/32KB memory at a time
- 32-word size OTP area
- 50ns flash access time of read
- wait(under 20MHz), 1-wait, 2-wait, and pre-fetch(read acceleration) access support
- Use internal 40MHz OSC clock to make timing control for Erase/Program

7.1 Flash memory map

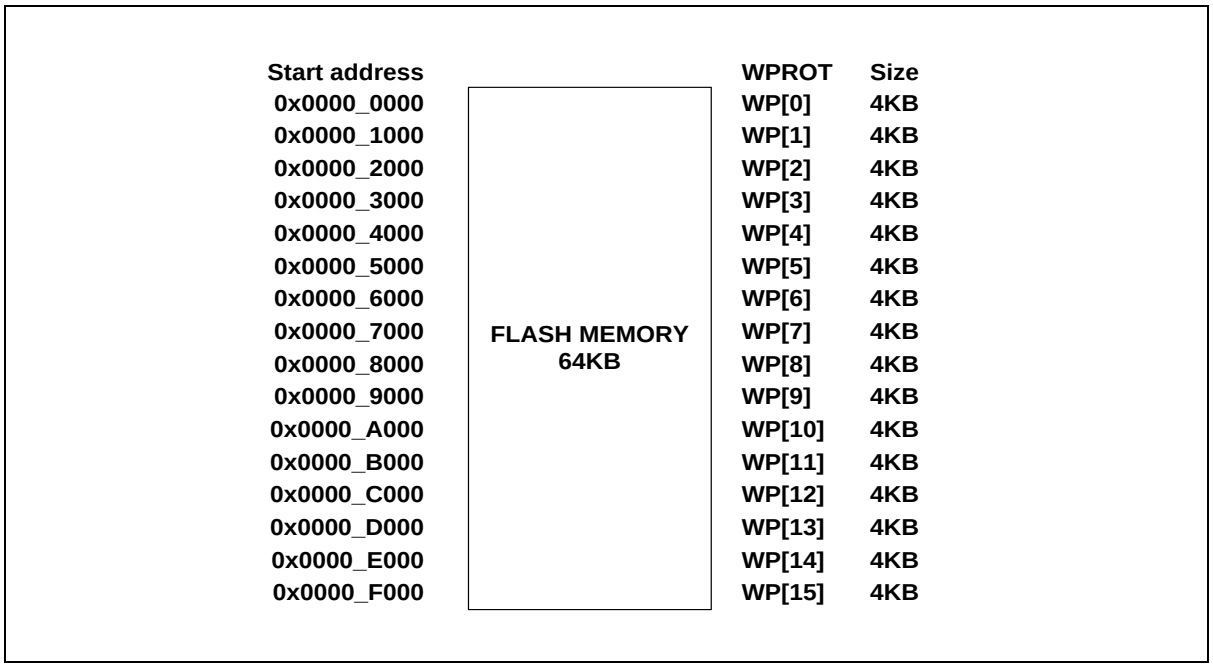


Figure 23. Code Flash Memory Map (64 KB Code Flash)

8. Watchdog Timer (WDT)

Watchdog Timer (WDT) monitors the operation of an MCU and is typically used to detect software errors. When the MCU becomes uncontrollable due to a malfunction, the WDT resets the MCU to recover it.

AC30M1x64/AC30M1x32 series has one WDT module built in, which functions as a 32-bit down-counter. Once the WDT counts down to zero while set as a reset source, the MCU gets reset. When it is not used to monitor the MCU, it can be used as a cycle timer along with an interrupt.

WDT of AC30M1x64/AC30M1x32 series features the followings:

- 32-bit down counter
- Select reset or periodic interrupt
- Count clock selection
- Dedicated pre-scaler
- Watchdog underflow output signal

8.1 WDT block diagram

In this section, WDT block diagram is introduced in Figure 24.

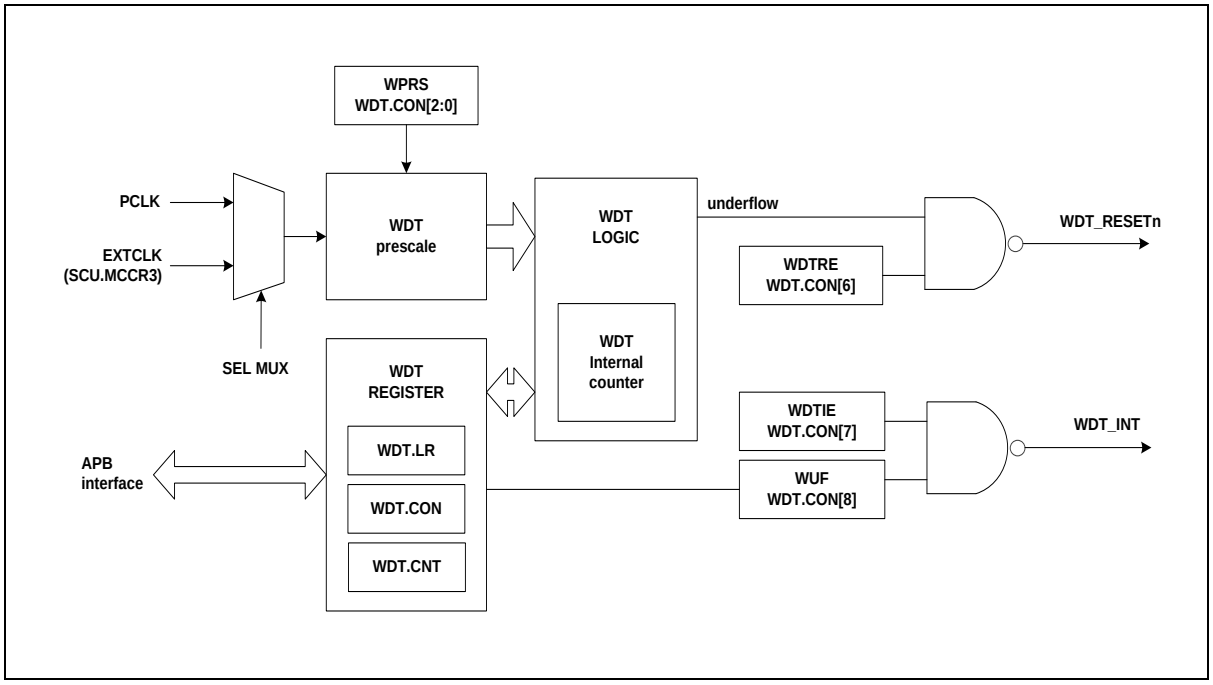


Figure 24. WDT Block Diagram

9. 16-bit timer

The timer block is consisted with 4 channels of 16 bit General purpose timers. They have independent 16 bit counter and dedicated prescaler feeds counting clock. They can support periodic timer, PWM pulse, one-shot timer and capture mode. They can be synchronized together.

One more optional free-run timer is provided. The main purpose of this timer is a periodical tick timer or a wake-up source.

16-bit timer of A33M1x series features the followings:

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 10-bit prescaler
- Synchronous start and clear function

Table 13 introduces pins assigned for 16-bit timer.

Table 13. Pin Assignment of 16-bit Timer: External Pins

Pin name	Type	Description
TnIO	I/O	External clock / capture input and PWM/one-shot output

9.1 16-bit timer block diagram

In this section, 16-bit timer is described in a block diagram in Figure 25.

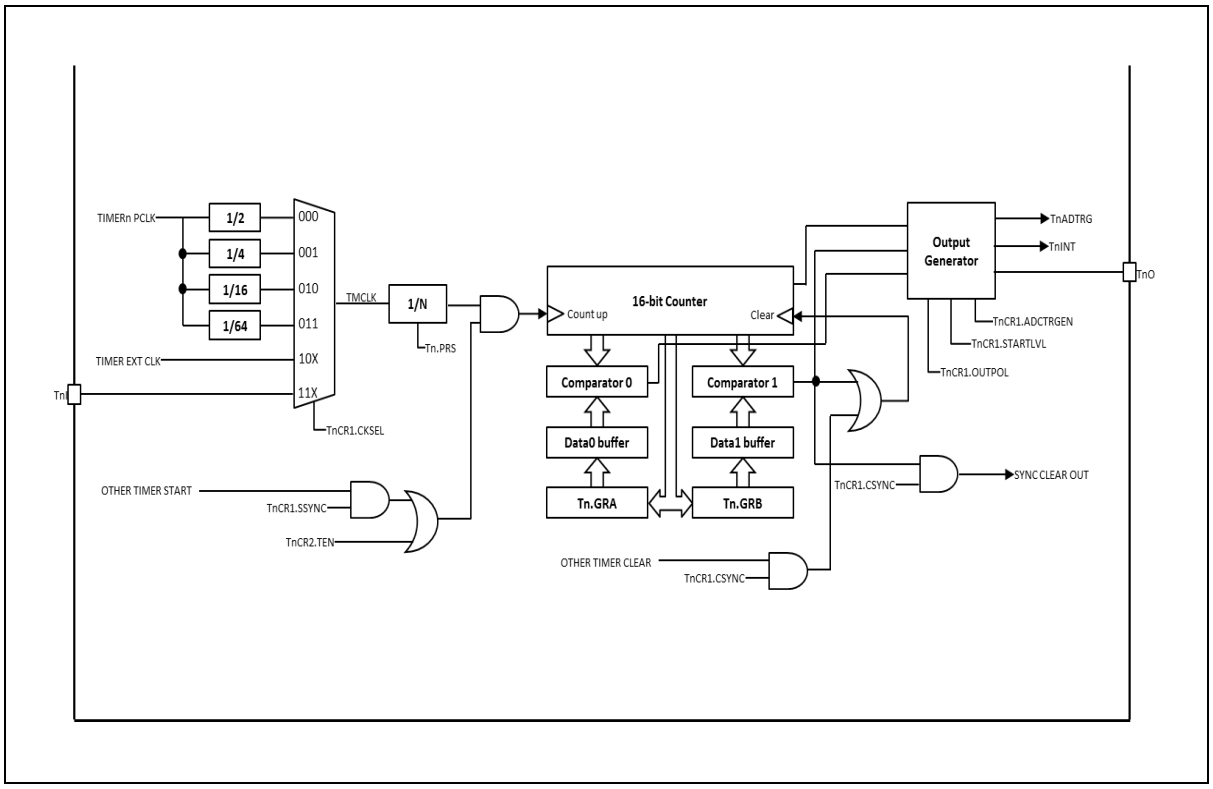


Figure 25. 16-bit Timer Block Diagram

10. Free Run Timers (FRT)

The AC30M1x64/AC30M1x32 series has one free-run timers (FRTs) built in, which are 32-bit up-count timers. These timers can run with the overflow or match interrupt according to their uses and can remain active in stop mode.

FRT of AC30M1x64/AC30M1x32 series features the followings:

- 32-bit up-count timers
- FRT match interrupts supported

10.1 FRT block diagram

In this section, FRT block diagram is introduced in Figure 26.

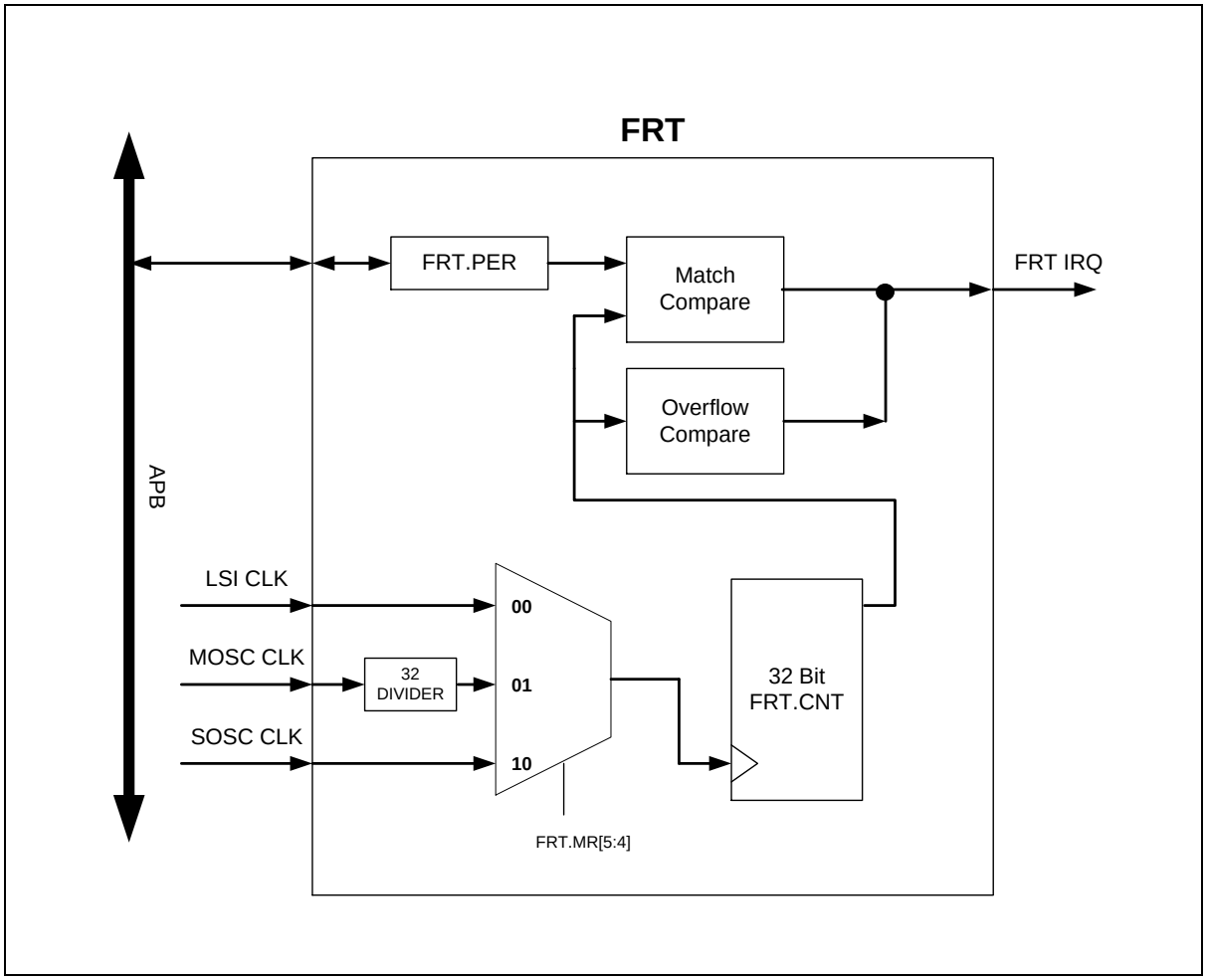


Figure 26. FRT Block Diagram

11. Universal Asynchronous Receiver/Transmitter (UART)

2-channel UART (Universal Asynchronous Receiver/Transmitter) modules are provided. UART operation status including error status can be read from status register. The prescaler which generates proper baud rate, is exist for each UART channel. The prescaler can divide the UART clock source which is PCLK, from 1 to 65535. And baud rate generation is by clock which internally divided by 16 of the prescaled clock and 8-bit precision clock tuning function.

Programmable interrupt generation function will help to control the communication via UART channel.

The UART of AC30M1x64/AC30M1x32 series features the followings:

- Compatible with 16450
- Standard asynchronous control bit (start, stop, and parity) configurable
- Programmable 16-bit fractional baud generator
- Programmable serial communication/
  5-, 6-, 7- or 8- bit data transfer/
  Even, odd, or no-parity bit insertion and detection/
  1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register

Table 14 introduces pins assigned for the UART.

Table 14. Pin Assignment of UART: External Pins

Pin name	Type	Description
TXD0	O	UART Channel 0 transmit output
RXD0	I	UART Channel 0 receive input
TXD1	O	UART Channel 1 transmit output
RXD1	I	UART Channel 1 receive input

11.1 UART block diagram

In this section, UART is introduced in block diagrams.

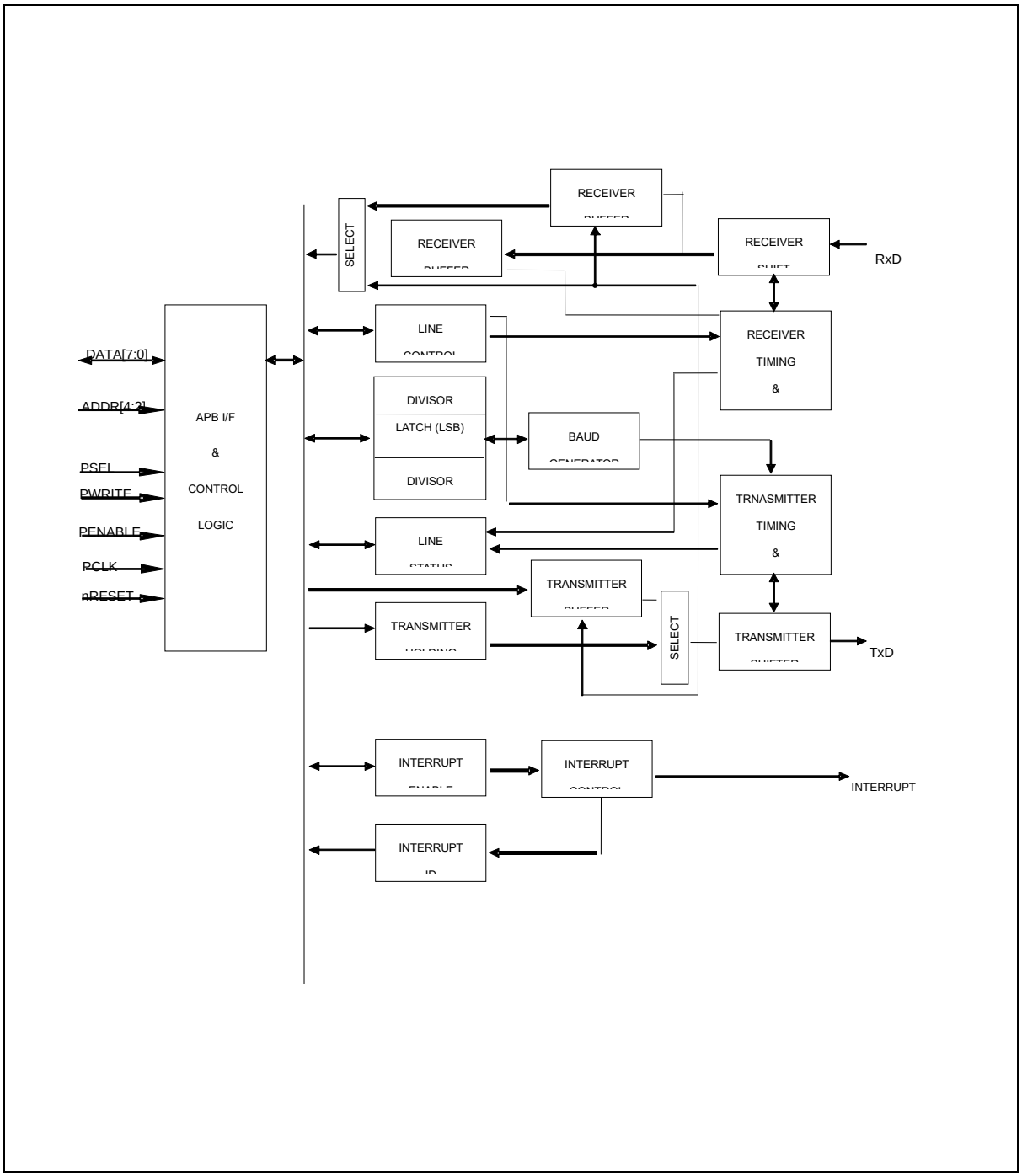


Figure 27. UART Block Diagram

12. Serial Peripheral Interface (SPI)

One Channel serial Interface is provided for synchronous serial communications with external peripherals. SPI block support both of master and slave mode. 4 signals will be used for SPI communication – SS, SCK, MOSI, and MISO.

- Master or Slave operation.
- Programmable clock polarity and phase
- 8, 9, 16, 17-bit wide transmit/receive register.
- 8, 9, 16, 17-bit wide data frame.
- Loop-back mode.
- Programmable start, burst, and stop delay time.

Table 15. Pin Assignment of SPI: External Pins

Pin name	Type	Description
SS	I/O	SPI Slave select input / output
SCK	I/O	SPI Serial clock input / output
MOSI	I/O	SPI Serial data (Master output, Slave input)
MISO	I/O	SPI Serial data (Master input, Slave output)

12.1 SPI block diagram

In this section, SPI is described in a block diagram in Figure 28.

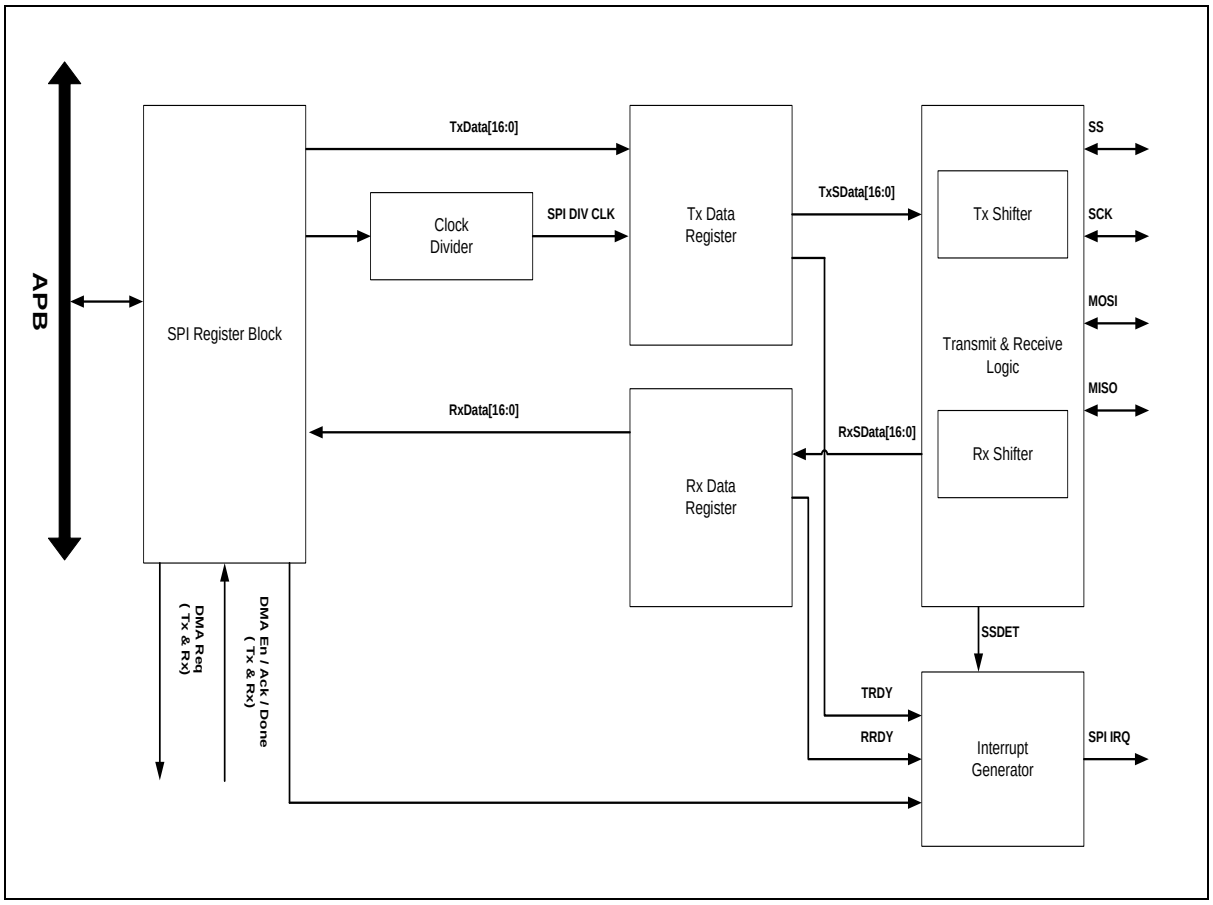


Figure 28. SPI Block Diagram

13. Inter Integrated Circuit (I2C)

I2C (Inter-Integrated Circuit) bus serves as an interface between the microcontroller and the serial I2C bus. It provides two wires, serial bus interface to a large number of popular devices and allows parallel-bus systems to communicate bidirectional with the I2C-bus.

I2C features the followings:

- Master and slave operation
- Programmable communication speed
- Multi-master bus configuration
- 7-bit addressing mode
- Standard data rate of 100/400 Kbps
- STOP signal generation and detection
- START signal generation
- ACK bit generation and detection

Table 16. Pin Assignment of I2C: External Pins

Pin name	Type	Description
SCL	I/O	I^2C channel Serial clock bus line (open-drain)
SDA	I/O	I^2C channel Serial data bus line (open-drain)

13.1 I2C block diagram

In this section, I2C interface block is described in a block diagram.

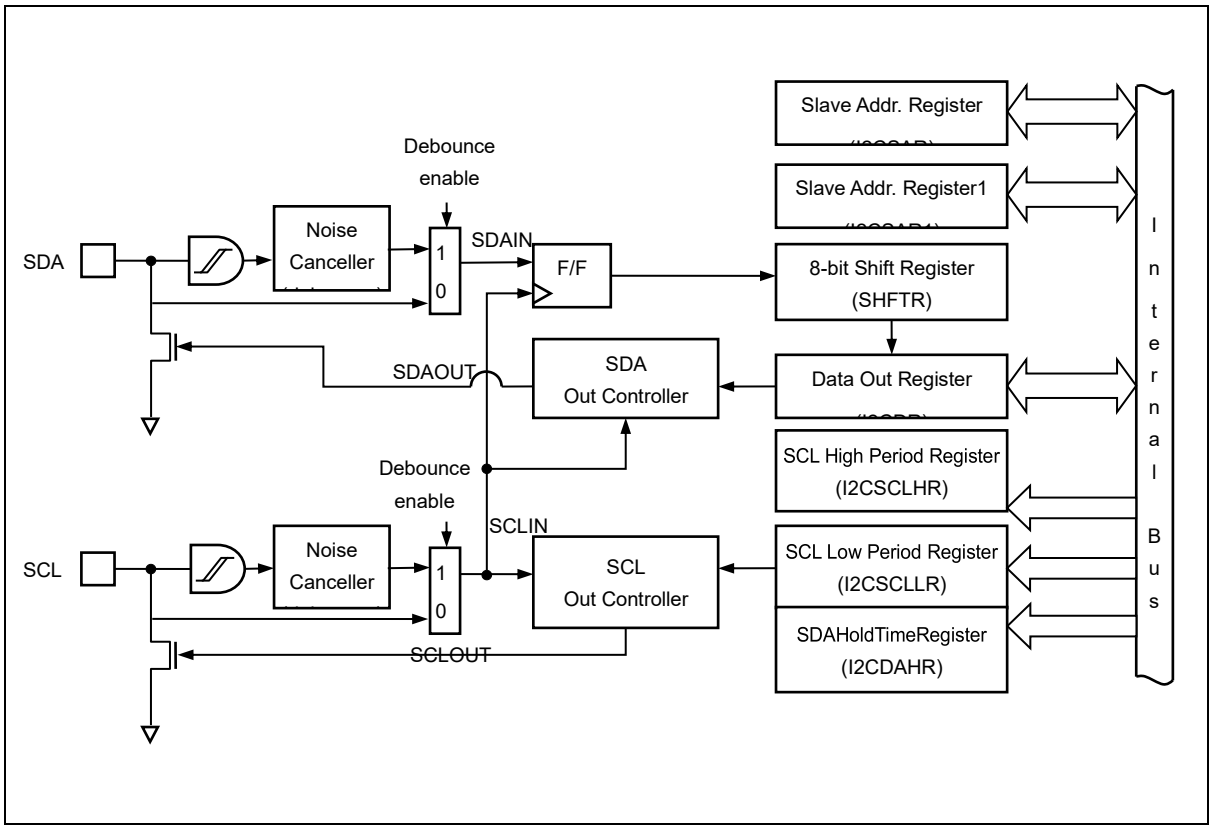


Figure 29. I2C Block Diagram

14. Motor Pulse Width Modulation (MPWM)

The MPWM is Programmable Motor controller which is optimized for 3-phase AC and DC motor control application. It can be used in many other application that need timing, counting and comparison.

The MPWM includes 3 channels, each of which controls a pair of outputs that is turn can control a motor.

MPWM Normal Mode of AC30M1x64/AC30M1x32 series features the followings:

- 16-bit Counter
- 6-channel outputs for motor control
- Dead-time supports
- Protection event and over voltage event handling
- 6 ADC trigger outputs
- Interval interrupt mode (period interrupt only)
- Up-down count mode

The MPWM clock source which is MPWM counter clock source will be provided from SCU block. The MPWM resolution and period will be defined by this MPWM clock configuration. The default MPWM clock is same as RINGOSC clock. Before enable MPWM module, the proper MPWM clock selection should be required.

Table 17 introduces pins assigned for MPWM.

Table 17. Pin Assignment of MPWM: External Pins

Pin name	Type	Description
MPWMUH	O	MPWM Phase-U H-side output
MPWMUL	O	MPWM Phase-U L-side output
MPWMVH	O	MPWM Phase-V H-side output
MPWMVL	O	MPWM Phase-V L-side output
MPWMWH	O	MPWM Phase-W H-side output
MPWMWL	O	MPWM Phase-W L-side output
PRTIN	I	MPWM Protection Input
OVIN	I	MPWM Over-voltage Input

14.1 MPWM block diagram

Figure 30 describes normal mode of MPWM in block diagram.

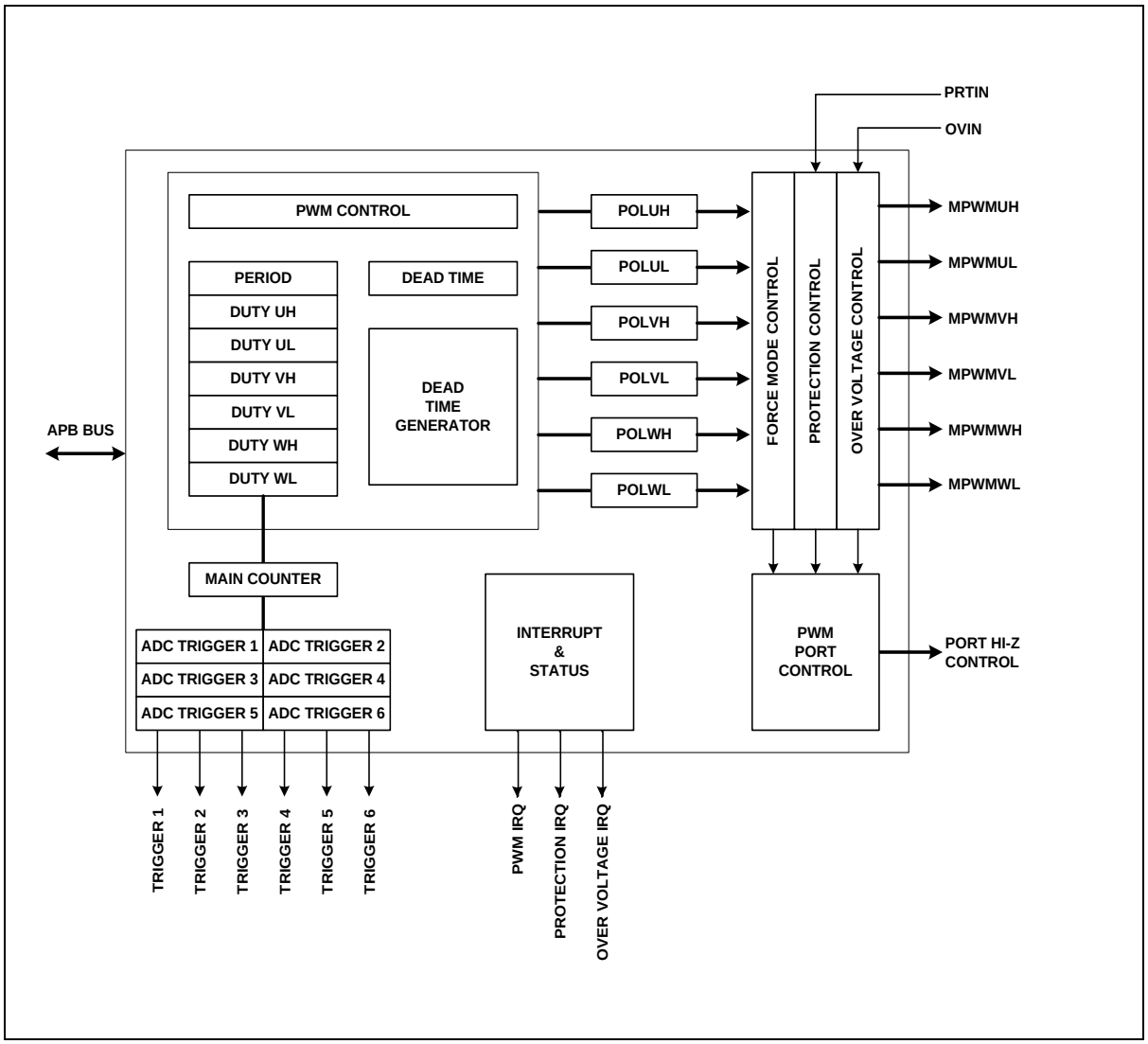


Figure 30. MPWM Block Diagram

15. Divider (DIV64)

Divider module (DIV64) provides hardware divider ability to accelerate complicated calculation. This divider is sequential 64bit/32bit divider, and requires 32 clock cycles for one operation.

The equation of the operation is shown below:

(AREGH,AREGL) / BREG = (QREGH,QREGL)

The DIV64 supports division of the following dividends:

- Unsigned 64bit dividend
- Unsigned 32bit divisor
- Unsigned 64bit quotient
- Unsigned 32bit remainder
- Unsigned 32 cycle operating time.

15.1 Divider block diagram

Figure 31 describes normal mode of Divider in block diagram.

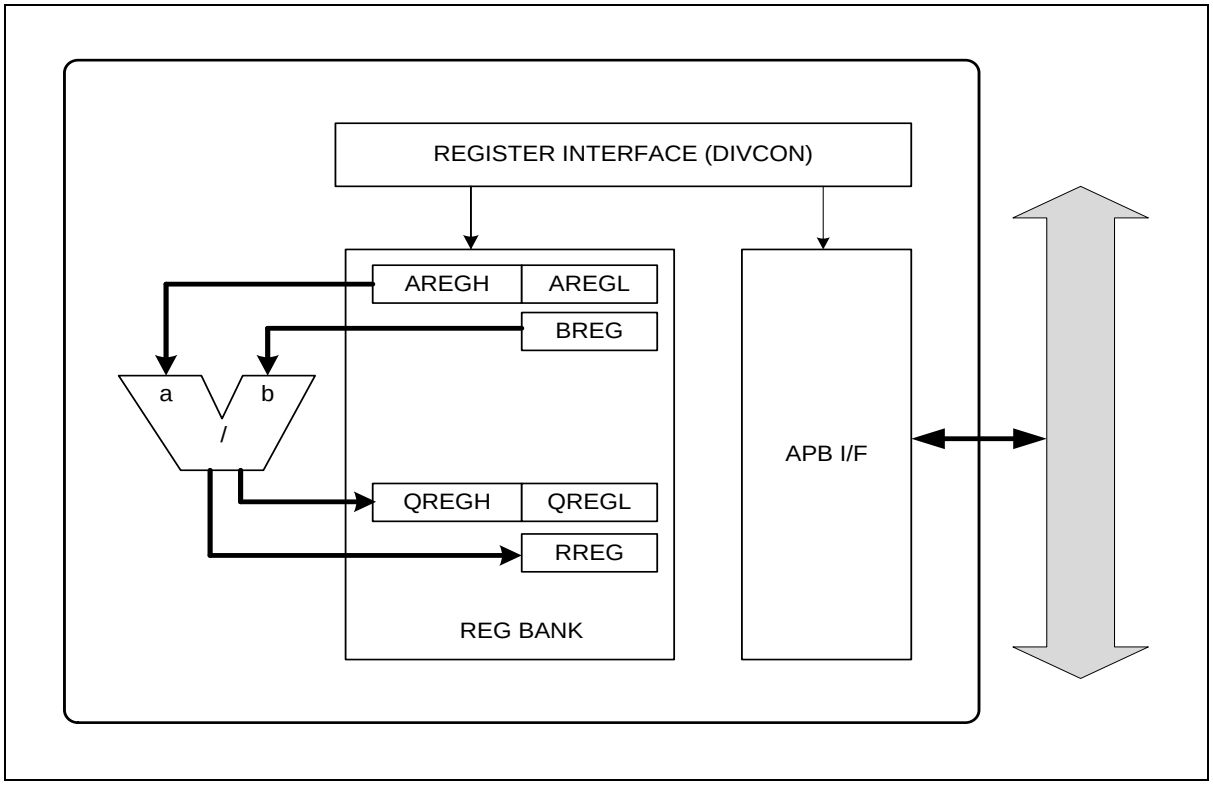


Figure 31. Divider Block Diagram

16. 12-bit Analog-to-Digital Converter (ADC)

ADC block of AC30M1x64/AC30M1x32 series consists of an independent ADC unit featuring the followings:

- 12 channels of analog inputs
- Single and Continuous conversion mode
- Up to 8 times sequential conversion supports
- Software trigger supports
- 3 internal trigger sources supports (Soft-trig, MPWM, Timers)
- Adjustable sample and hold time

Table 18 introduces pins assigned for ADC.

Table 18. Pin Assignment of ADC: External Pins

Pin name	Type	Description
VDD	P	Analog Power(2.4V~5V)
VSS	P	Analog GND
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10
AN11	A	ADC Input 11

16.1 12-bit ADC block diagram

In this section, 12-bit ADC is described in a block diagram in Figure 32.

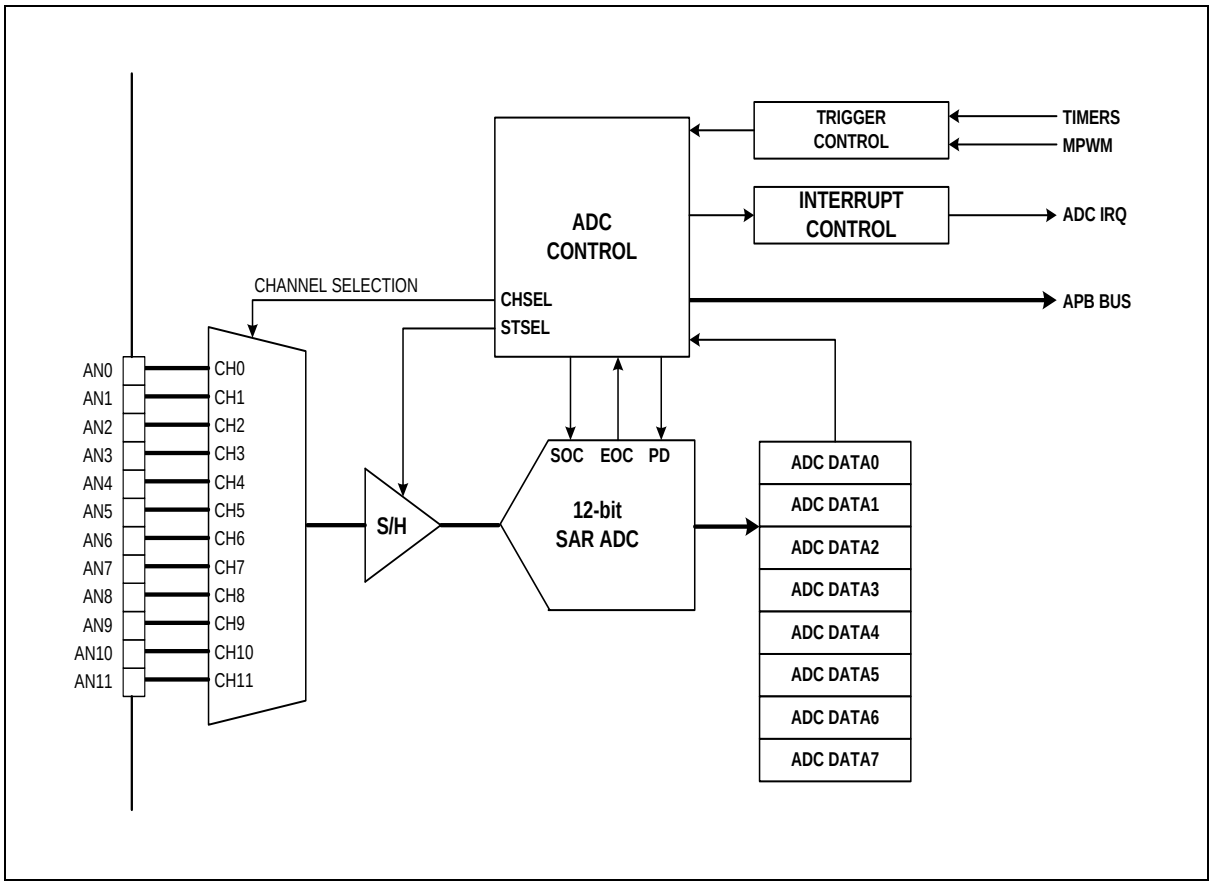


Figure 32. 12-bit ADC Block Diagram

17. Electrical characteristics

17.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions.

Table 19. Absolute Maximum Rating

Parameter	Symbol	min	max	unit
Power supply (VDD)	VDD	-0.5	+6	V
Analog power supply (AVDD)	AVDD	-0.5	+6	V
VDC output voltage	VDD18			V
Input high voltage		-	VDD+0.5	V
Input low voltage		VSS – 0.5	-	V
Output low current per pin	I_{OL}		5	mA
Output low current total	$\sum I_{OL}$		40	mA
Output high current per pin	I_{OH}		5	mA
Output high current total	$\sum I_{OH}$		40	mA
Power consumption				mW
Input main clock range		4	16	MHz
Operating frequency		-	40	MHz
Storage temperature	Tst	-55	+125	℃
Operating temperature	Top	-40	+105	℃

17.2 DC characteristics

Table 20. Recommended Operating Condition

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Supply voltage	VDD		2.2	-	5.5	V
Supply voltage	AVDD		2.2	-	5.5	V
Operating frequency	FREQ	MOSC	4	-	16	MHz
		SOSC	-	32.768	-	kHz
		HSI	38.8	40	41.2	MHz
		LSI	32	40	48	kHz
Operating temperature	Top	Top	-40	-	+105	℃

Table 21. DC Electrical Characteristics

(VDD = +5V, Ta = 25 ℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Input low voltage	V_{IL}	Schmitt input	-	-	0.2VDD	V
Input high voltage	V_{IH}	Schmitt input	0.8VDD	-	-	V
Output low voltage	V_{OL}	I_{OL} = 3mA	-	-	VSS+1.0	V
Output high voltage	V_{OH}	I_{OH} = -3mA	VDD–1.0	-	-	V
Input high leakage	I_{IH}				4	uA
Input low leakage	I_{IL}		-4			
Pull-up resister	R_{PU}	VDD=5V	30	-	90	kΩ

17.3 Current consumption

Table 22. Current Consumption in Each Mode

(Temperature: +25℃ Only)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Normal operation	IDD_{NORMAL}	LSIOSC=RUN, HSIOSC=RUN MXOSC=RUN, SXOSC=RUN HCLK=LSIOSC	-	2.6	-	mA
		LSIOSC=RUN, HSIOSC=OFF MXOSC=OFF, SXOSC=OFF HCLK=LSIOSC	-	0.7	-	mA
		LSIOSC=RUN, HSIOSC=RUN MXOSC=RUN, SXOSC=RUN HCLK=HSIOSC	-	10.3	-	mA
		LSIOSC=OFF, HSIOSC=RUN MXOSC=OFF, SXOSC=OFF HCLK=HSIOSC	-	9.4	-	mA
		LSIOSC=RUN, HSIOSC=RUN MXOSC=RUN, SXOSC=RUN HCLK=MXOSC	-	4.2	-	mA
		LSIOSC=OFF, HSIOSC=OFF MXOSC=RUN, SXOSC=OFF HCLK=MXOSC	-	3.2	-	mA
		LSIOSC=RUN, HSIOSC=RUN MXOSC=RUN, SXOSC=RUN HCLK=SXOSC	-	2.6	-	mA
		LSIOSC=OFF, HSIOSC=OFF MXOSC=OFF, SXOSC=RUN HCLK=SXOSC	-	0.7	-	mA
SLEEP mode	IDD_{SLEEP}	LSIOSC=RUN, HSIOSC=RUN SXOSC=RUN, MXOSC=RUN HCLK =LSIOSC	-	2.5	-	mA
		LSIOSC=RUN, HSIOSC=OFF SXOSC=OFF, MXOSC=OFF HCLK =LSIOSC		0.6		mA
		LSIOSC=RUN, HSIOSC=RUN SXOSC=RUN, MXOSC=RUN HCLK =HSIOSC		7.6		mA

Table 25. Current consumption in each mode (continued)

(Temperature: +25℃ Only)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
SLEEP mode	IDD_{SLEEP}	LSIOSC=OFF, HSIOSC=RUN SXOSC=OFF, MXOSC=OFF HCLK =HSIOSC		6.8		mA
		LSIOSC=RUN, HSIOSC=RUN SXOSC=RUN, MXOSC=RUN HCLK =MXOSC		3.5		mA
		LSIOSC=OFF, HSIOSC=OFF SXOSC=OFF, MXOSC=RUN HCLK =MXOSC		2.5		mA
		LSIOSC=RUN, HSIOSC=RUN SXOSC=RUN, MXOSC=RUN HCLK =SXOSC		2.5		mA
		LSIOSC=OFF, HSIOSC=OFF SXOSC=RUN, MXOSC=OFF HCLK =SXOSC		0.6		mA
POWER DOWN mode	IDD_{STOP}	LSIOSC=STOP, SIOSC=STOP SXOSC=STOP, MXOSC=STOP HCLK=STOP	-	5	10	uA

NOTES:

1. uart en, 1 port toggle @5VLSIOSC (40KHz)
2. HSIOSC (40MHz), MXOSC (8MHz), SXOSC (32.768KHz)

17.4 POR electrical characteristics

Table 23. POR Electrical Characteristics

(Temperature: -40 ~ +105℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	VDD18		1.6	1.8	2.0	V
Operating current	IDD_{PoR}	Typ. <6uA, If always on	-	60	-	nA
POR set level	VR_{PoR}	VDD rising (slow)	1.3	1.4	1.55	V
POR reset level	VF_{PoR}	VDD falling (slow)	1.1	1.2	1.4	V

17.5 LVD electrical characteristics

Table 24. LVD Electrical Characteristics

(Temperature: -40 ~ +105℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	VDD		1.7		5	V
Operating current	IDD_{LVD}	Typ. <6uA when always on	-	1	-	mA
LVD set level 0	VLVD0	VDD falling (slow)	1.58	1.73	2.2	V
LVD set level 1	VLVD1	VDD falling (slow)	2.4	2.65	3.1	V
LVD set level 2	VLVD2	VDD falling (slow)	3.55	3.7	4.15	V

17.6 VDC electrical characteristics

Table 25. VDC Electrical Characteristics

(Temperature: -40 ~ +105℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	VDD_{VDC}		2.2	-	5.5	V
Current consumption	IDD_{NORM}	@RUN	-	100	150	uA
	IDD_{STOP}	@STOP	-	1	2	uA

17.7 External OSC characteristics

Table 26. External OSC Characteristics

(Temperature: -40 ~ +105℃)

Parameter	Symbol	Condition	Min	Typ	Max	unit
Operating voltage	VDD		2.2	-	5.5	V
IDD		@4MHz/5V	-	240		uA
Frequency	$OSCF_{req}$		4	-	16	MHz
Output voltage	OSC_{VOUT}		1.2	2.4	-	V
Load capacitance	$LOAD_{CAP}$		5	22	35	pF

17.8 ADC electrical characteristics

Table 27. ADC Electrical Characteristics

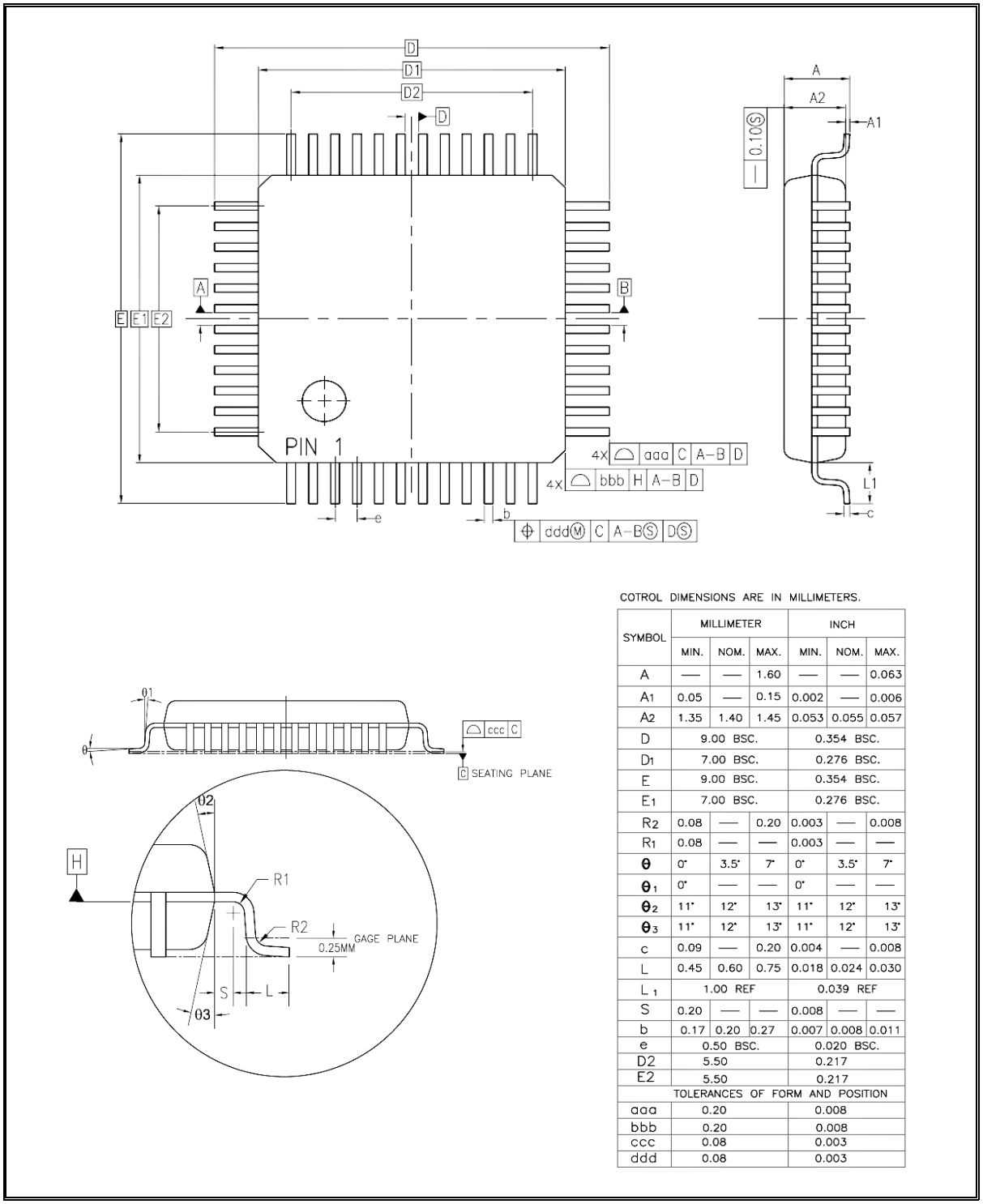
(Temperature: -40 ~ +105℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	AVDD		2.4	5	5.5	V
Resolution				12		Bit
Operating current	IDDA				2.8	mA
Analog input range			0		AVDD	V
Conversion rate				-	1.0	MSPS
Operating frequency	ACLK				16	MHz
DC accuracy	INL			±3.5		LSB
	DNL			±2.5		LSB
Offset error				±1.5		LSB
Full scale error				±1.5		LSB
SNDR	SNDR			68		dB
THD				-70		dB

18. Package information

This chapter provides AC30M1x64/AC30M1x32 series package information.

18.1 48 LQFP package information

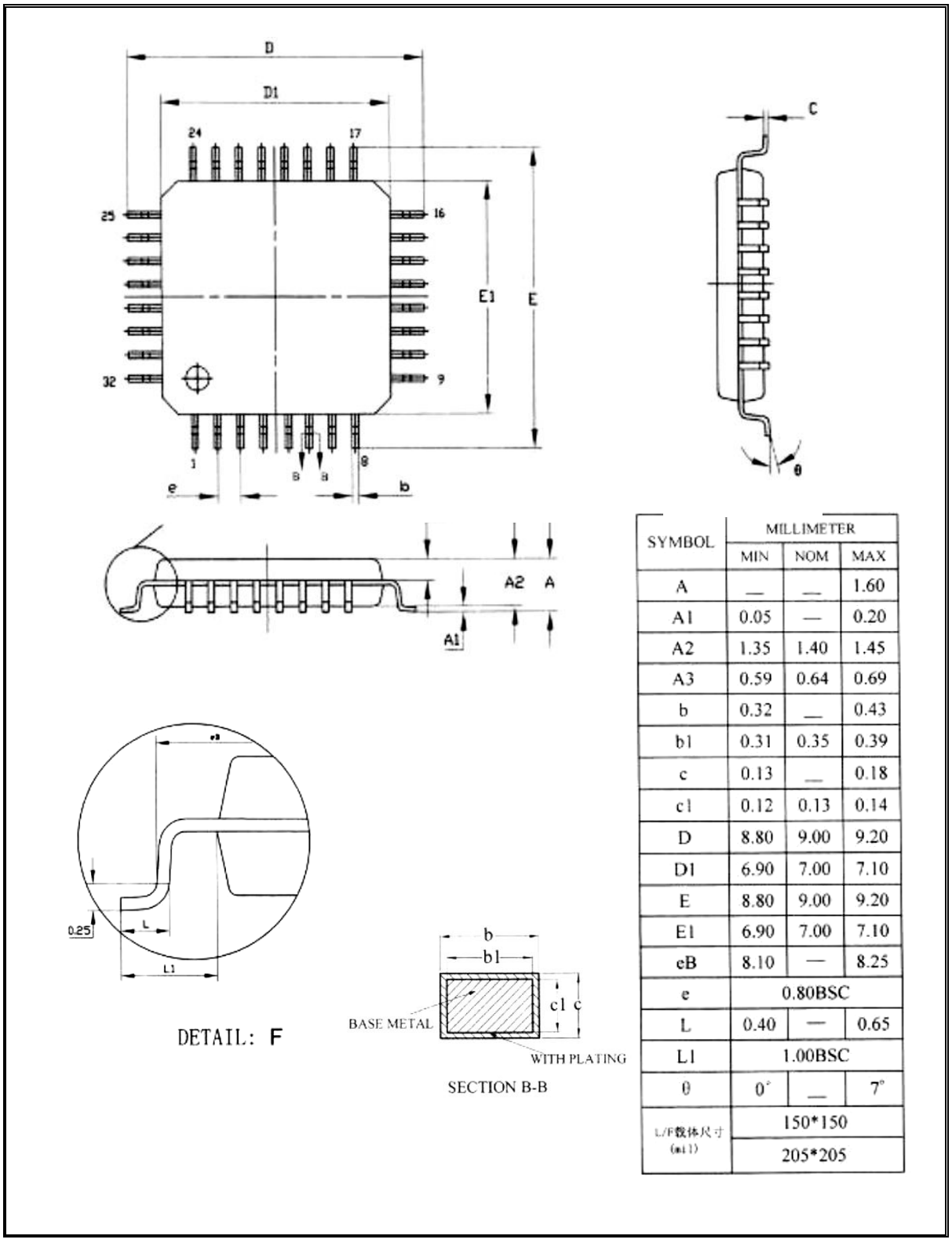


COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 33. 48 LQFP Package Outline

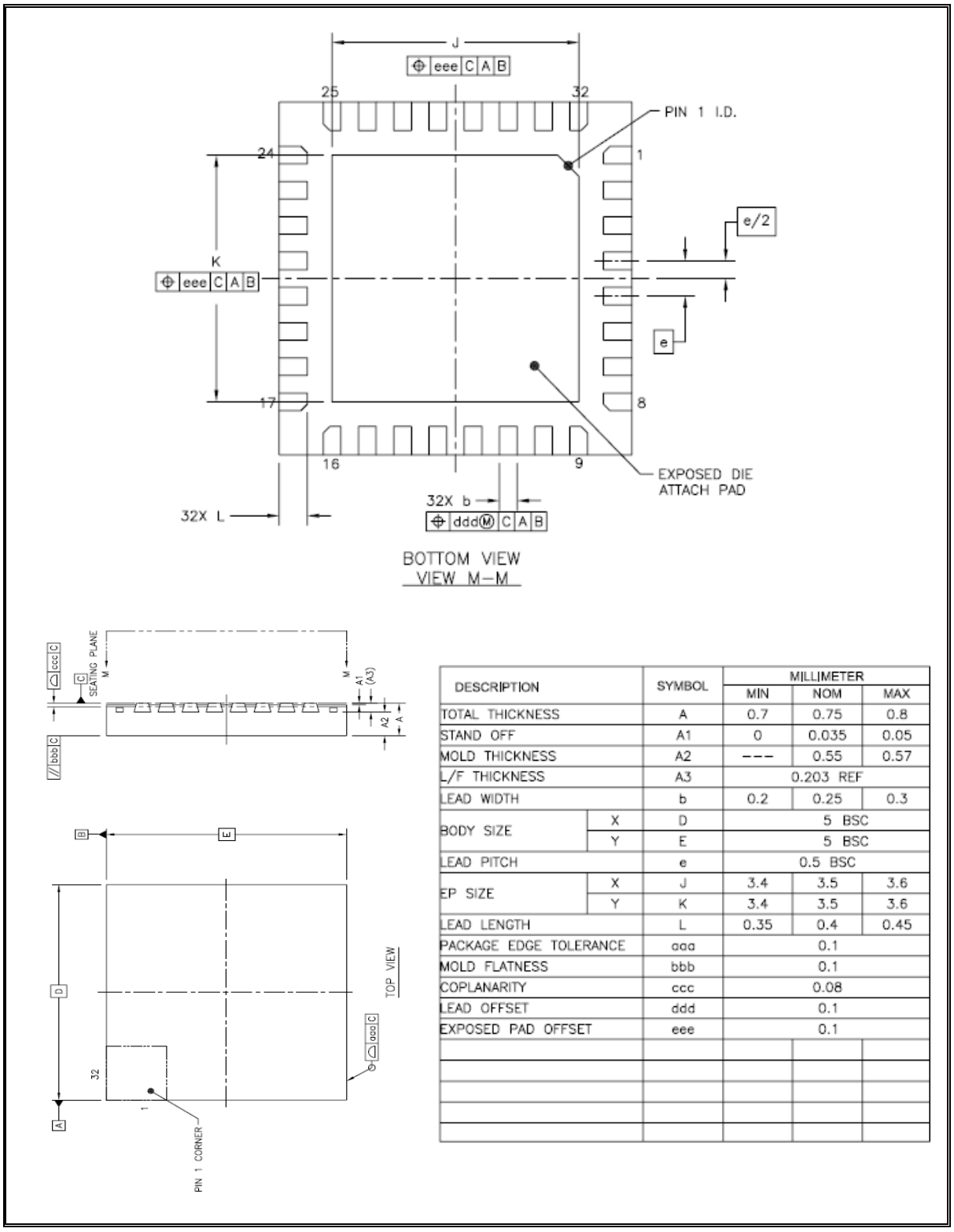
18.2 32 LQFP package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	—	0.43
b1	0.31	0.35	0.39
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.80BSC		
L	0.40	—	0.65
L1	1.00BSC		
θ	0°	—	7°
L/F载体尺寸 (note1)	150*150		
	205*205		

Figure 34. 32 LQFP Package Outline

18.3 32 QFN package information



DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 35. 32 QFN Package Outline

19. Ordering information

Table 28. AC30M1x64/AC30M1x32 Series Device Ordering Information

Device name	Flash	SRAM	UART	SPI	I2C	MPWM	ADC	I/O ports	Package
AC30M1464LBN*	64KB	4KB	2	1	1	1	12 ch.	44	LQFP-48
AC30M1364LBN	64KB	4KB	2	1	1	1	10 ch.	30	LQFP-32
AC30M1364UB*	64KB	4KB	2	1	1	1	10 ch.	30	QFN-32
AC30M1332LBN*	32KB	4KB	2	1	1	1	10 ch.	30	LQFP-32
AC30M1332UB*	32KB	4KB	2	1	1	1	10 ch.	30	QFN-32

: For available options or further information on the devices with an “” mark, please contact the ABOV sales office.

20. Development tools

This chapter introduces wide range of development tools for AC30M1x64/AC30M1x32. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

20.1 Compiler

ABOV semiconductor does not provide any compiler for AC30M1x64/AC30M1x32. However, since AC30M1x64/AC30M1x32 have ARM's high-speed 32-bit Cortex-M0 Cores for their CPU, you can use all kinds of third party's standard compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our A-Link and A-Link Pro. Please visit our website www.abovsemi.com for more information regarding the A-Link and A-Link Pro.

20.2 Debugger

The A-Link and A-Link Pro support ABOV Semiconductor's AC30M1x64/AC30M1x32 MCU emulation in SWD Interface. The A-Link and A-Link Pro use two wires interfacing between PC and MCU, which is attached to user's system. The A-Link and A-Link Pro can read or change the value of MCU's internal memory and I/O peripherals. In addition, the A-Link and A-Link Pro control MCU's internal debugging logic. This means A-Link and A-Link Pro control emulation, step run, monitoring and many more functions regarding debugging.

The A-Link and A-Link Pro run underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the A-Link and A-Link Pro are provided in Figure 36. More detailed information about the A-Link and A-Link Pro, please visit our website www.abovsemi.com and download the debugger S/W and documents.

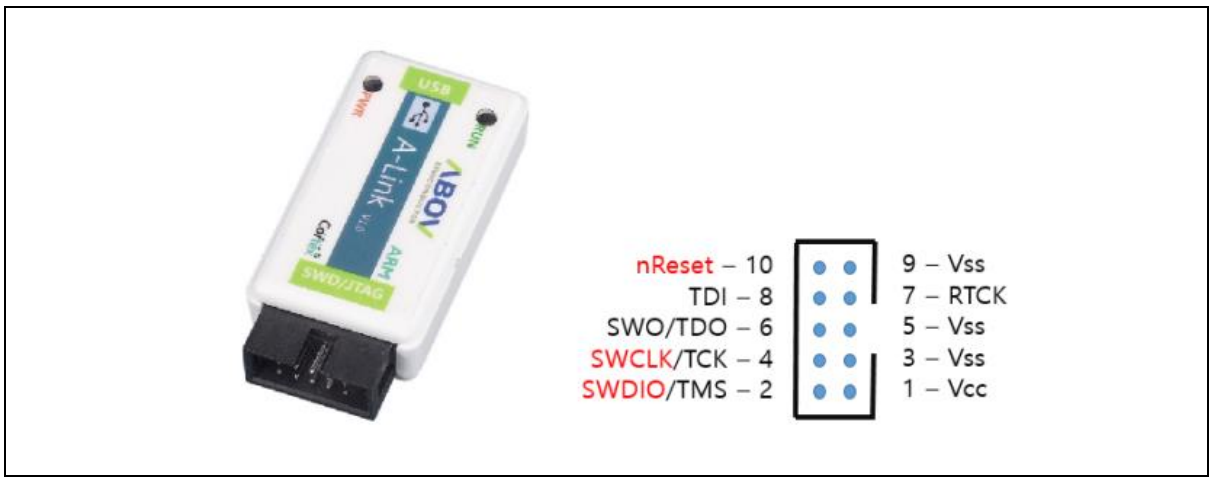


Figure 36. A-Link and Pin Descriptions

20.3 Programmer

20.3.1 E-PGM+

E-PGM+ is a single programmer, and allows a user to program on the device directly.

- Support ABOV devices
- 2~5 times faster than S-PGM+
- Main controller: 32-bit MCU @ 72MHz
- Buffer memory: 1MB

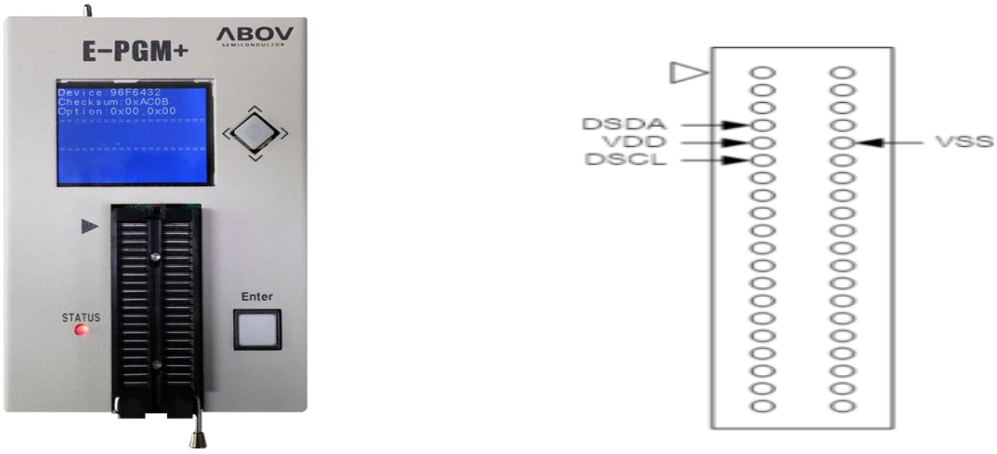


Figure 37. E-PGM+ (Single Writer) and Pin Descriptions

20.3.2 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

Figure 38. E-Gang4 and E-Gang6 (for Mass Production)

Revision history

Date	Version	Description
2016/7/22	1.0.0	File created
2016/8/17	1.1.0	32pin map diagram changed
2016/10/10	1.1.1	description errors were corrected Explanation of Un.IER was modified.
2016/10/17	1.1.2	Modified MP.Duty, MP.SR, MP.OLR Explanation. Modified figure of MPWM functional description.
2016/10/26	1.1.3	Modified LVD Voltage Level. Delete 4.35V
2016/11/18	1.1.4	Add Low Voltage Reset (chapter1.3.3)
2016/11/23	1.1.5	Electrical Characteristic Output High/Low Current Total Value Modified, Current Consumption Condition Addition.
2017/01/16	1.1.6	Modified SWD mode description.
2020/6/09	1.00	1st creation(PMO)
2022/10/17	1.01	Update the template of this document

Korea

Regional Office, Seoul
R&D, Marketing & Sales
8th Fl., 330, Yeongdong-daero,
Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200
Fax: +82-2-508-6903
www.abovsemi.com

HQ, Ochang
R&D, QA, and Test Center
93, Gangni 1-gil, Ochang-eup,
Cheongwon-gun,
Chungcheongbuk-do,
28126, Korea

Tel: +82-43-219-5200
Fax: +82-43-217-3534
www.abovsemi.com

Domestic Sales Manager
Tel: +82-2-2193-2206
Fax: +82-2-508-6903
Email: sales_kr@abov.co.kr

Global Sales Manager
Tel: +82-2-2193-2281
Fax: +82-2-508-6903
Email: sales_gl@abov.co.kr

China Sales Manager
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
Email: sales_cn@abov.co.kr

ABOV Disclaimer

IMPORTANT NOTICE – PLEASE READ CAREFULLY

ABOV Semiconductor ("ABOV") reserves the right to make changes, corrections, enhancements, modifications, and improvements to ABOV products and/or to this document at any time without notice. ABOV does not give warranties as to the accuracy or completeness of the information included herein. Purchasers should obtain the latest relevant information of ABOV products before placing orders. Purchasers are entirely responsible for the choice, selection, and use of ABOV products and ABOV assumes no liability for application assistance or the design of purchasers' products. No license, express or implied, to any intellectual property rights is granted by ABOV herein. ABOV disclaims all express and implied warranties and shall not be responsible or liable for any injuries or damages related to use of ABOV products in such unauthorized applications. ABOV and the ABOV logo are trademarks of ABOV. All other product or service names are the property of their respective owners. Information in this document supersedes and replaces the information previously supplied in any former versions of this document.

© 2020 ABOV Semiconductor – All rights reserved