ABOV SEMICONDUCTOR

A33G53x Datasheet

Cortex®-M3 32-bit General-Purpose Microcontroller, 75 MHz, Up to 768 KB Code Flash, 32 KB Data Flash, 24 KB SRAM, 12-bit ADC, Flash Memory ECC for Household Application

DS Rev. 1.01

Features

Core and Memory

- Arm® 32-bit Cortex®-M3 Core
- Up to 75 MHz

Memories

- Up to 768 KB Code Flash Memory
- Dual Bank Code Flash Memory
- 32 KB of Data Flash Memory
- Up to 24 KB SRAM
- Support Read-While-Write (RWW)
- ECC (Error Correction Code)

Reset and Power Management

- Power-on/power-down reset (POR/LVR/LVI)
- Low-power modes: SLEEP, DEEP-SLEEP

Clock Management

- Internal oscillator (IOSC16) 16 MHz
  - ±3.0% @ −20°C to 70°C
  - ±40% @ −40°C to 85°C
- Internal Ring oscillator (RINGOSC) 1 MHz
  - ±50% @ −40°C to 85°C
- External Main Oscillator (MXOSC)
  - 4 MHz to 10 MHz
- Sub Crystal oscillator (SXOSC)
  - 32.768 kHz
- Phase-locked loop (PLL) frequency generator
  - Up to 75 MHz

Port Map Controller (PMC)

General-purpose Input/Output (GPIO)

- Up to 90 I/O pins with interrupt capability
- All mappable on external interrupt vectors
- Multi-function pins have up to four selections of functions, including PMC

12-bit ADC

- Single SAR ADC
- Up to 16 analog input channels
- Input voltage for ADC conversion
  - AGND ~ AVDD
- 70 ksps A/D conversion time
  - Max 15 µs per channel (@AVDD: 5 V, ADC clock: 4 MHz)
- Single conversion
- A/D conversion by internal Start bit or external trigger source (Timer 0 ~ 9)

Low-Voltage Detector (LVD)

- Eight-step voltage detection level
- LVD (Low-Voltage Detector) reset
- LVD (Low-Voltage Detector) interrupt
- Wake-up by LVD function after SLEEP or DEEP-SLEEP mode.

16-bit Timer

- Ten channels
  - Ten input capture channels
  - Ten output channels
- Timer operating modes:
  - Periodic timer mode
  - One-shot mode
  - PWM mode
  - Capture mode
- 10-bit prescaler

Watchdog Timer (WDT)

- 32-bit down-count timer
- Reset and periodic interrupts
- Eight different prescalers

Free-Run Timer (FRT)

- 32-bit free-run timer

Pulse Width Modulation (PWM)

- Eight PWM generators
- PWM signal with 16-bit independent counter

Serial Interfaces

- UART
  - Two 16450 asynchronous serial communication ports
  - Two 16550 asynchronous serial communication ports
- SPI
  - Two synchronous serial communication ports
- I2C
  - Two communication ports

Development Support

- Serial Wire Debug (SWD), JTAG interfaces

Package

- 100-MQFP-1420 (0.65 mm pitch)
- 100-LQFP-1414 (0.5 mm pitch)
- 80-LQFP-1414 (0.65 mm pitch)
- 64-LQFP-1212 (0.65 mm pitch)

Applications

- Home Appliances (HA) controller

Operating Voltage

- 3.0 V to 5.5 V

Operating Temperature

- Commercial grade (−40°C to 85°C)

Product Selection Table

Table 1. Device Summary

Device Name	Code Flash	Data Flash	SRAM	SPI	UART	I2C	PWM	ADC	I/O Ports	Package
A33G539VQ*	768 KB	32 KB	24 KB	2	4	2	8	16	90	100-MQFP
A33G539VL	768 KB	32 KB	24 KB	2	4	2	8	16	90	100-LQFP14
A33G539MM*	768 KB	32 KB	24 KB	2	4	2	8	15	71	80-LQFP14
A33G539RL*	768 KB	32 KB	24 KB	2	4	2	8	10	60	64-LQFP12
A33G538VQ*	512 KB	32 KB	24 KB	2	4	2	8	16	90	100-MQFP
A33G538VL*	512 KB	32 KB	24 KB	2	4	2	8	16	90	100-LQFP14
A33G538MM*	512 KB	32 KB	24 KB	2	4	2	8	15	71	80-LQFP14
A33G538RL*	512 KB	32 KB	24 KB	2	4	2	8	10	60	64-LQFP12

: For available options or further information on the device with “” marks, please contact the ABOV sales office.

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1. Descriptions

A33G53x series is a 32-bit high-performance microcontroller with up to 768 KB of flash memory. The A33G53x series is a powerful microcontroller that provides effective solutions to various electrical appliances requiring various peripheral devices and large amounts of Flash memory.

A 32-bit microcontroller based on the high-performance Arm Cortex-M3 core, the A33G53x series features up to 768 KB of code flash memory, 32 KB of data flash memory, and 24 KB of SRAM for a wide range of home appliances, including refrigerators, washing machines, dryers, dishwashers, water purifiers, and blenders.

1.1 Product Category Definition

Table 2 gives an overview of the memory capacity of the available devices in the A33G53x series.

Table 3 lists the features supported in each product category in the following section.

Table 2. A33G53x Series Memory Density

Memory Density		Category
Flash	RAM	
768 KB	24 KB	A33G539
512 KB	24 KB	A33G538

1.2 Availability of Peripherals

Table 3 summarizes the product-specific features in the A33G53x series, assuming the largest package is used for the A33G53x series microcontroller.

Table 3. A33G53x Series Features

Peripherals		Description
Core	CPU	• Maximum operating frequency: 75 MHz • 32-bit Arm Cortex-M3 Core - 32-bit Thumb®-2 instruction set • Register settings in CPU: - General-purpose registers specified - Main Stack Pointer (MSP) and Process Stack Pointer (PSP): R13 - Link register (LR): R14 - Program counter (PC): R15 • Data ordering format: Little-Endian • Harvard Architecture • AHB/ APB
	Interrupt	• NVIC (Nested Vectored Interrupt Controller) • Up to 64 peripheral interrupts supported • 3-bit width of Group Priority: 8-step priority.

Table 3. A33G53x Series Features (continued)

Peripherals		Description
Memory	Code Flash	• Capacity: - A33G539: 768 KB Code Flash memory - A33G538: 512 KB Code Flash memory • A high-capacity Code Flash memory built-in • Max 25 MHz Flash access speed • One-word (4 bytes) programs • 512 bytes, 2 KB erases • Bulk erase • Read protection • Self-programming (Supports updating data in some Code Flash memory region during the execution of user program in the code area.) • CRC code generation and verification for the Flash memory • Endurance: 10,000 cycles • Lifetime: 10 years
	Data Flash	• Capacity: 32 KB • Max 25 MHz access speed • 1 byte program • One-word (4 bytes) programs (for use ECC) • 512 bytes, 2 KB erases • CRC code generation and verification for the Flash memory • Endurance: 100,000 cycles • Lifetime: 10 years
	BootROM	• Executes the processor's boot mode when receiving an input at the nBOOT pin from an external circuit • SPI and UART boot modes • In-system programming • Users can program data into the internal Flash memory by setting up an application board.
	SRAM	• Capacity: 24 KB • Usable as a program's work area • High-speed execution enables the execution of time-critical codes • Part of the SRAM can be remapped into an interrupt vector area

Table 3. A33G53x Series Features (continued)

Peripherals		Description
Power Management Unit (PMU)	Operation Modes	• Run mode (Run) • SLEEP mode (Idle) • DEEP-SLEEP mode (Power-Down)
	Clock	• Internal oscillator (IOSC16) 16 MHz - ±3.0% @ −20°C to 70°C - ±40% @ −40°C to 85°C • Internal Ring oscillator (RINGOSC) 1 MHz - ±50% @ −40°C to 85°C • External Main Oscillator (MXOSC) - 4 MHz to 10 MHz • Sub Crystal oscillator (SXOSC) - 32.768 kHz • Phase-locked loop (PLL) frequency generator - Up to 75 MHz
	Reset	• Main Clock Fail • External nRESET Pin • Core reset • Software Reset • POR (Power-On Reset) • LVD (Low-Voltage Detector) Reset • External Main Oscillation error

Table 3. A33G53x Series Features (continued)

Peripherals		Description
Power Management Unit (PMU)	LDO	• Integrated LDO (Low-DropOut) for low-power operation
	POR	• Internal core voltage monitoring and reset signal generation
	LVD	• 8-step voltage detection level • LVD (Low-Voltage Detector) reset • LVD interrupt • Wake-up by LVD function after SLEEP or DEEP-SLEEP mode.
	Low-power Consumption	• Low-power operation mode • SLEEP mode (Idle) • DEEP-SLEEP mode (Power-down)
	Wake-up Event	• GPIOA~GPIOF • FRT • Failure of the External Main Oscillation • WDT • LVD • Rapid wake-up operation with internal oscillator and external clock source
Port Map Controller (PMC) General Purpose I/O (GPIO)		• General purpose I/O Ports • 100-LQFP / MQFP - I/O pins: 90 • 80-MQFP - I/O pins: 71 • 64-LQFP - I/O pins: 60 • Configuration of pin mode - Push-Pull Output - Open-Drain - Logic Input - Analog Input • Setting pin function using MUX • High/Low-level detection and interrupt • Rising/Falling edge detection and interrupt • Setting pull-up/pull-down/debounce • Large-current Port (Port D) • Separate bit set/reset function • Wake-up event by external asynchronous input

Table 3. A33G53x Series Features (continued)

Peripherals		Description
TIMER	16-bit timer	• General-purpose 16-bit up-count timer • Ten channels - TnC: Timer input 10-ch - TnO: Timer output 10-ch • Timer operating modes - Periodic timer mode - One-shot mode - PWM mode - Capture mode • Interrupt events - Timer/counter match interrupt - Timer overflow interrupt • Timer Input clock - MXOSC / IOSC16 / SXOSC / RINGOSC - Timer input by external TnC pin in capture mode • Output timer clock signal by external TnO pin • 10-bit prescaler
	WDT	• 32-bit down-count timer • Reset and periodic interrupts • MXOSC / IOSC16 / SXOSX / RINGOSC clock source selection • Eight different prescalers are selectable
	FRT	• 32-bit Free-Run Timer - Capable of calculating the internal system time - 32-bit up-count timer • Interrupt events - Period interrupt: Occurred timer interrupt according to the time interval set by the user. Integrated comparator for match interrupt - Overflow interrupt • Eight different prescalers are selectable

Table 3. A33G53x Series Features (continued)

Peripherals		Description
Pulse-Width Modulation	PWM	• PWM generator with eight channels • PWM signal with 16-bit independent counter • consists of 1 unit per 4 channels. • 8-bit prescaler per 1 unit • Configuration of duty and period of PWM output signal • 1/2, 1/4, 1/8, 1/16 clock divider • 16-bit period and count value set • built-in channels that output inverted PWM signal
Serial interface	UART	• 16550/16450 compatible asynchronous serial communication port four channels - A 16550-compliant device with 2-channel FIFO - A 16450-compliant device with a two-channel double buffer • Built-in fractional point divider to improve baud rate accuracy. • Supports UART0 channel when entering BOOT mode. • Single or multi-sampling of receiving data
	SPI	• Two synchronous serial communication port channels • Double buffer structure for high-speed transmission • Master / Slave selection function of communication channel • Setting function for transmission data • 8-/ 9-/ 16-/ 17-bit data transmission and reception - SPI clock speed - Both least significant bit (LSB)-first and most significant bit (MSB)-first modes available - The SPI0 channel is used when boot mode is entered.
	I2C	• Standard I2C communication protocol • Two channels supported • Master and Slave modes supported for each channel • 7-bit addressing supported for Slave mode • SCL signal's high/ low periods and SDA signal's hold time settable • Byte-by-byte data communication by interrupt and polling type • I2C Max. transfer rate: 400 kbps • Configuring I2C clock and data signal latency

Table 3. A33G53x Series Features (continued)

Peripherals		Description
12-bit A/D Converter	ADC	• 12-bit resolution • Single SAR A/D converter • Built-in Analog MUX for multiple input • Input voltage for ADC conversion • AGND ~ AVDD • 70 KSPS A/D conversion time • Max. 15 μs/channel (AVDD=5.0 V, A/D conversion clock=4 MHz) • Interrupt of end of A/D conversion • Trigger source of A/D conversion: Timer 7-channels • A/D conversion by internal START bit or external trigger source channels • 100-pin: 16-ch × 1-unit • 80 / 64 pin: 10-ch × 1-unit
Operating Voltage		• 3.0 V to 5.5 V
Operating temperature		• Commercial grade (−40°C to 85°C)
Package		• Three types of package options - 100-pin MQFP/ LQFP (Trace/ JTAG/ SWD) - 80-pin LQFP (JTAG/ SWD) - 64-pin LQFP (JTAG/ SWD)

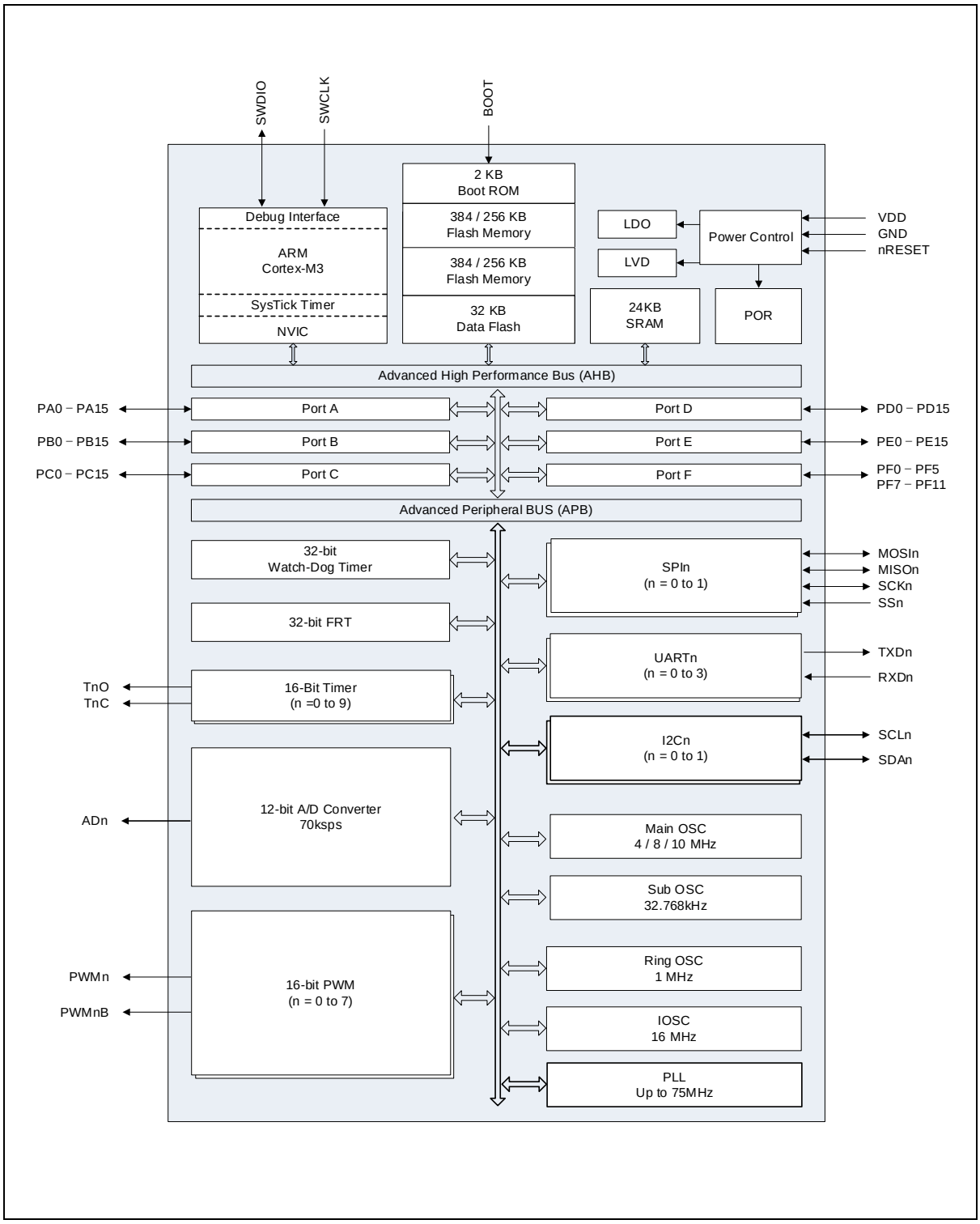
Table 4. Summary of A33G53x Peripherals

Peripheral		A33G53xVQ	A33G53xVL	A33G53xRL	A33G53xMM
Code Flash memory		A33G539: 768 KB A33G538: 512 KB			
Data Flash memory		32 KB			
SRAM		24 KB			
Timers	PWM	8 (16-bit)			
	General purpose	10 (16-bit)			
	SysTick Timer	1			
	Watchdog Timer	1			
	Free-Run Timer	1			
Communication interfaces	SPI	2			
	I2C	2			
	UART	4			
GPIO		90	90	71	60
ADCs		70 KSPS	70 KSPS	70 KSPS	70 KSPS
Number of channels		16	16	10	10
Max. CPU frequency		75 MHz			
Operating voltage		3.0 V to 5.5 V			
Operating temperature		Ambient operating temperature: −40°C to 85°C			
Packages		100-MQFP	100-LQFP	80-LQFP	64-LQFP

1.3 Block Diagram

Figure 1 shows a block diagram of the A33G53x series.

Figure 1. A33G53x Block Diagram



1.4 Functional Overview

The following sections provide overviews of the features of the A33G53x series microcontroller.

1.4.1 Cortex-M3 Core

The A33G53x series is based on the Cortex-M3 CPU core, an Arm's high-performance 32-bit microcontroller core. The Cortex-M3 processor uses Harvard architecture and supports the Thumb-2 instruction set.

Refer to the technical reference manual "ARM DDI0337H" for detailed information on Cortex-M3.

1.4.2 Embedded SRAM

The A33G53x series has a block of zero-wait on-chip SRAM. The size of the SRAM is 24 KB, and its base address is 0x2000_0000. The SRAM is used for storing data and as a stack memory.

The SRAM can also store program code for faster execution or during Flash erase/ programming operations. This device does not support a memory remap strategy. Therefore, performing a jump and return is necessary to execute the code stored in the SRAM.

1.4.3 Boot Configuration

The A33G53x series offers a boot mode for programming the internal Flash memory. The boot mode can be entered by setting the BOOT pin to 'H' at reset timing (The normal state is 'L').

The boot mode supports both UART boot and SPI boot:

- UART boot uses TXD0 and RXD0 ports.
- SPI boot uses MOSI0, MISO0, SCK0, and SS0 ports.

Pins for the boot mode are listed in Table 5.

Table 5. Boot Mode Pin List

Block	Pin Name	Pin Direction	Description
SYSTEM	nRESET/ PC6	Input	Reset input signal
	BOOT/ PC7	Input	Boot mode setting pin
UART0	RXD0/ PC8	Input	UART boot receives data.
	TXD0/ PC9	Output	UART boot transmits data.
SPI0	SS0/ PB10	Input	SPI boot slave select
	SCK0/ PB11	Input	SPI boot clock input
	MOSI0/ PB12	Input	SPI boot data input
	MISO0/ PB13	Output	SPI boot data output

1.4.4 Power Supply

The device requires a 3.0 V to 5.5 V operating voltage supply (VDD), and analog peripherals are supplied through the independent power domain AVDD.

Table 6. Power Supply

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	3.0	5.5	V
	AV_{DD} (Analog V_{DD})	3.0	5.5	V

During a power-up process, a reset plays an important role and affects the entire process of system booting. The A33G53x series has two power-related reset options, as described below:

- POR_RST (Power-On Reset) that controls the voltage less than 1.4 V.
- LVD_RST (Low-Voltage Detect Reset) that controls the voltage less than 2.6 V (default).

The Code Read operation may malfunction if the power level exceeds the POR and is below the Flash operating voltage (Min. 1.35 V). To prevent this abnormal Code Read operation, the LVD_RST operates to generate the SYSRESETn internal signal and enters the microcontroller into reset mode.

The minimum level that the LVR can set is 2.6 V, which satisfies the Flash minimum operating voltage.

1.4.5 Operation Mode

1.4.5.1 Transition of Operation Mode

INIT mode is the initial state of the chip when a reset is asserted.

In RUN mode, the CPU operates at the maximum performance with the high-speed clock system.

SLEEP and DEEP-SLEEP modes can be used as low-power consumption modes. In the low-power consumption mode, power is effectively managed to reduce power consumption by halting the processor core and any unused peripherals.

1.4.5.2 RUN Mode

The CPU and peripheral hardware operate with a high-speed clock in RUN mode. After a reset, the microcontroller enters RUN mode if the INIT state is detected.

1.4.5.3 SLEEP (IDLE) Mode

Once the microcontroller enters SLEEP mode, the CPU becomes inactive. By setting the PMU_PER and PMU_PCCR registers, users can determine which peripherals will be inactive in SLEEP mode.

1.4.5.4 DEEP-SLEEP (Power-down) Mode

The microcontroller enters DEEP-SLEEP mode when the core goes under the stop state using WFI instruction.

1.4.5.5 Reset Mode

The A33G53x series has two system reset options: a cold reset, which is effective during power-up or power-down sequences, and a warm reset, which is triggered by multiple reset sources.

The following are reset sources for the A33G53x series:

- Power-On Reset (POR)
- Low-Voltage Detect (LVD) Reset
- nRESET pin reset
- Watchdog timer (WDT) reset
- Software reset
- Clock oscillating error reset
- CPU request reset

1.4.6 Clocks and Startup

The A33G53x series has two main operating clocks: HCLK, which generates clock signals for CPU and AHB systems, and PCLK, which generates clock signals for peripheral systems.

1.4.6.1 HCLK Clock

The Cortex-M3 core requires two clocks: HCLK and FCLK. The HCLK supplies the clock to the CPU and AHB. While the FCLK remains enabled unless the system enters DEEP-SLEEP mode, the HCLK can be disabled in Idle mode.

The HCLK clocks the buses and memories. As the bus clock frequency is limited to a maximum of 75 MHz, the HCLK frequency must not exceed 75 MHz.

1.4.6.2 PCLK Clock

PCLK can be used as a clock source for any peripheral. The PMU_PCCR register determines whether the PCLK for each peripheral is enabled or disabled. Each peripheral block's registers cannot be read if its PCLK input is not enabled. Additionally, it is important to note that the PCLK stops operating in DEEP-SLEEP mode.

1.4.6.3 Clock Configuration Procedure

After the microcontroller is powered on, the Ring OSC (1 MHz) is initially enabled as a system clock source by default. Users initially set other clock sources while the Ring OSC clocks the system. The IOSC16 (16 MHz) can be enabled with the PMU_CCR (Clock Control Register).

Before enabling the Main OSC block, the pin mux configuration must be completed for XTALI and XTALO. Users must be careful not to affect other bits of the PC_MR and PC_CR registers during this process. Once the Main OSC block has been enabled, the users must wait for the crystal oscillation to stabilize.

The secondary Sub Crystal Oscillator (32.768 kHz) clock can be enabled with the PMU_CCR (Clock control register). Likewise, with pins XTALI and XTALO for the Main OSC, the Sub OSC must be enabled after configuring the pin mux for SXIN and SXOUT, allowing sufficient time for the oscillation to be stabilized.

1.4.7 Interrupts and Events

1.4.7.1 Nested Vectored Interrupt Controller (NVIC)

The A33G53x series includes up to 64 maskable interrupt channels that manage sixteen priority levels and the Nested Vectored Interrupt Controller (NVIC) that controls 16 interrupt lines of the Cortex®-M3.

The following are the advantages of NVIC:

- The NVIC enables interrupt processing while reducing interrupt latency.
- Interrupt Vector Table (IVT) address delivered directly to the core.
- The fast interrupt processing capability
- High-priority interrupts are completed before low-priority interrupts, even if generated later than the low-priority interrupts.
- Tail Chaining
- Automatic saving of processor state
- Interrupt restoring without instructional overhead at the end of the interrupt.

The NVIC hardware block provides flexible and efficient interrupt management with minimal interrupt latency.

1.4.7.2 Extended Interrupt (EXTI)

The Extended Interrupt feature enables the system to generate event requests or wake up from SLEEP or DEEP-SLEEP mode. Each external line can be configured independently to detect trigger events such as rising or falling edges or both edges and level events such as Low or High.

1.4.8 Port

1.4.8.1 Port Map Controller (PMC)

The A33G53x series has a Port Map Controller (PMC) module that controls the external input and output (I/O) ports. By setting the PMC registers, users can configure the pins' uses, input/ output direction, pull-up/ pull-down, and debouncing for their applications as needed.

1.4.8.2 General-Purpose Input/ Output (GPIO)

Except for the VDD, GND, and certain specific-purpose pins, pins can be used as General-Purpose Input/Output (GPIO) pins.

The GPIO module controls the general I/O ports. Output pins can be set to generate high or low-level signals by configuring the corresponding bits of the GPIO control registers, while logic input pins can be monitored for their input status in the control registers.

1.4.9 Embedded Flash Memory

The flash memory controller serves as an interface between the core and the embedded flash memory and is responsible for managing the data stored on the flash memory.

The flash memory of the A33G53x series has several key features, as listed below:

- Code Flash capacity: Built-in high-capacity code flash memory
  - A33G539 (768 KB, 384 sectors)
    - Bank0: 384 KB
    - Bank1: 384 KB
  - A33G538 (512 KB, 256 sectors)
    - Bank0: 256 KB
    - Bank1: 256 KB
- Data Flash capacity: 32 KB (32 sectors)
- Bank Swap and RWW (Read-While-Write) in code flash memory
- ECC (Error Correct Code)
- Up to 25 MHz flash memory access timing
- Program unit
  - Code Flash: word (4 bytes)
  - Data Flash: byte (Data Flash ECC disabled) / word (Data Flash ECC enabled)
- Erase unit
  - Page (512 bytes)
  - Sector (2 KB)
  - Bulk (Up to 768 KB, chip)
- Self-program function for code flash memory
  - Supports updating data in some Code Flash memory regions while executing user programs in the Code Flash area.
- A specific area of flash memory is restricted for protection and security.

1.4.10 Timers

1.4.10.1 16-bit Timer

The A33G53x series has a TIMER module configured with ten units. This 16-bit Timer supports four operating modes: Periodic mode, PWM mode, One-shot mode, and Capture mode.

Users can use a divided PCLK or an external clock as an input clock source for the 16-bit Timer. An internal 10-bit prescaler allows the generation of various timer base clocks.

Interrupts can be triggered regularly when the Timer is used in Periodic mode. The users can set the period and duty to form a PWM signal used in PWM mode.

In One-shot modes, the Timer can generate one PWM waveform. In Capture mode, the external input signal's pulse intervals can be measured based on the preset condition. Moreover, the Timer can export signals to other devices to control them. This Timer is primarily used as a periodic tick timer or wake-up source.

1.4.10.2 Free-Run Timer (FRT)

The A33G53x has a built-in 32-bit up-count timer for Free-Run Timer (FRT). The FRT can run with an overflow interrupt or a match interrupt according to the setting period of a user application.

1.4.10.3 Watchdog Timer (WDT)

A Watchdog Timer (WDT) is used to detect microcontroller errors caused by external interference or unexpected logical conditions. These errors cause the application program to deviate from its normal sequence. If the microcontroller loses control, the WDT will reset the microcontroller, allowing it to return to normal operation.

The WDT of the A33G53x series is a 32-bit down counter. If the WDT is set as a reset source, the microcontroller restarts when the down counter reaches 0.

If the WDT is not used to monitor the microcontroller, it can be used as a cycle timer that generates interrupts.

1.4.10.4 SysTick Timer

Although the SysTick Timer is primarily designed for real-time operating systems, it can also be utilized as a standard down-counter.

The SysTick Timer has the following features:

- 24-bit down-counter
- Automatic refreshing
- Maskable system interrupt generation when the counter reaches zero.

1.4.11 Universal Asynchronous Receiver/Transmitter (UART)

The A33G53x has four channels of UART compatible with 16C550/16C450. Among the four channels, UART0 and UART1 channels are 16550 with FIFO type, and UART2 and UART3 channels are 16450 with double buffer type.

When initialized, all UART channels operate in the same data mode (no FIFO mode) as 16450. After initialization, the FIFO mode setting is possible only for UART0 and UART1. In the FIFO mode, up to 16 bytes of data can be stored in the transmit/receive FIFO.

The built-in UART can read out the data of the set configuration and the received data or the current UART status. UART status information can be checked for the type and conditions of transmission and reception by UART and for errors (parity, overrun, framing, and break interrupt) that may occur when data is received.

Each UART has a programmable baud rate generator to divide the prescaled clock into a value between 1 and 65535. The clock is again divided into 16 clocks to create a clock that drives the UART's internal transmit and receive blocks.

Communication with the UART can also be controlled by an interrupt using a user-programmable interrupt function. However, although the general purpose 16550/16450 has a modem control signal and associated registers but does not operate the modem control function for the A33G53x.

1.4.12 Serial Peripheral Interface (SPI)

The A33G53x series has three built-in SPI modules. The SPI modules are synchronized by clocks, and the specifications of the transfer clocks are adjustable.

The SPI module supports communications between one Master and multiple Slaves. The slave can be selected by the Slave Select (SS) signal.

The SPI module performs three-wire or four-wire synchronous transfers via four signal terminals (SS, SCK, MOSI, and MISO). Its separate Transmit and Receive Buffers enable full-duplex communication, where data can be read and written simultaneously.

1.4.13 Inter Integrated Circuit (I2C) Interface

The I2C interface built in the A33G53x series satisfies the standard I2C communication protocol and is used for serial communication with internal and external devices via the I2C protocol.

Equipped with two units, the I2C supports both Master and Slave modes and can transmit and receive data in bytes by using interrupts or polling.

The I2C of the A33G53x series operates in Standard mode (100 kHz) or Fast mode (400 kHz) and supports General calls. It helps communicate with various peripherals that have the same bus type.

To use the I2C, it is recommended to set the SCL and SDA pins to open-drain and then connect external pull-up resistors to render their output signals' HIGH'.

Table 7. Features of I2Cn (n = 0 to 1)

I2C Features	I2C0	I2C1
7-bit addressing mode	O	O
Standard-mode (up to 100 kbit/s)	O	O
Fast-mode (up to 400 kbit/s)	O	O
General call	O	O

1.4.14 Pulse-Width Modulation (PWM)

The A33G53x has eight built-in PWM generators that can output PWM waveforms. Each PWM generator has a 16-bit resolution, four channels form a 1-unit, and each unit has a built-in prescaler.

Through PWM-related register settings, the PWM generator generates the square waveform signal required for user applications such as LEDs, motors, inverters, etc.

1.4.15 Analog-to-Digital Converter (ADC)

The A33G53x has a built-in 12-bit SAR type ADC that samples analog signals into digital signals at a rate of 70 KSPS. The ADC in the A33G53x is designed to receive up to 16 channels in a time-division manner.

When converting an analog signal to a digital signal, the analog value input to the ADC channel is converted to a 12-bit resolution digital value using the signal applied to the AVDD pin (analog voltage supply pin) as the reference voltage. In other words, the input reference voltage of the ADC can be set by varying the voltage of the AVDD pin, and the analog voltage ranging from GND to AVDD can be input and output as a digital signal.

1.5 Development Tools

In this chapter, various development tools for the A33G53x are introduced. ABOV provides software tools, debuggers, and programmers to assist users in achieving the desired results for their target applications. ABOV supports the development ecosystem for our customers.

1.5.1 Compiler

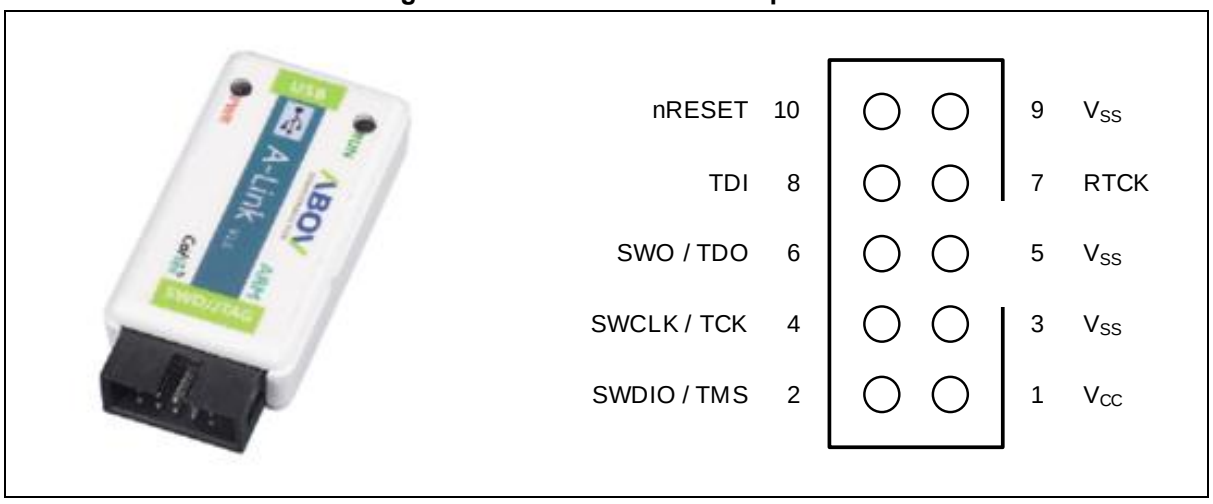
Since the A33G53x series has the Arm 32-bit Cortex-M3 core, any third-party compiler, such as Keil, IAR, and GCC cross-C compiler supporting Cortex-M3, is available.

1.5.2 Debugger

A-Link and A-LinkPro can be used to emulate the A33G53x microcontrollers using the SWD interface and have a two-wire interface to connect to the microcontroller on the user system. A-Link and A-LinkPro provide extensive debugging capabilities for the microcontroller, including the ability to read or write the value of the device's internal memory and I/O peripherals and control its internal debugging logic. A-Link and A-LinkPro are debug interfaces with third-party compilers, providing an excellent combination of debugging environments.

The figure below shows the pinout for programming with the A-Link and A-LinkPro. For more detailed information about the A-Link and A-LinkPro, visit www.abovsemi.com and download related software and documents.

Figure 2. A-Link and Pin Description



1.5.3 Programmer

1.5.3.1 E-PGM+

E-PGM+ and E-PGM Serial are standalone programmers which allow users to program directly on the device.

- Support for all ABOV microcontrollers.
- A dedicated tool for mass production
- 40-pin Textool DIP socket for single-chip programming (E-PGM+ only)
- 10-pin connector for ISP mode
- USB host interface
- HEX downloads and controls.

1.5.3.2 Gang Programmer

E-Gang4 and E-Gang6 can program multiple devices simultaneously and operate in host-controlled and standalone modes without requiring a host computer connection. These programmers feature a USB interface for easy connection to a handler.

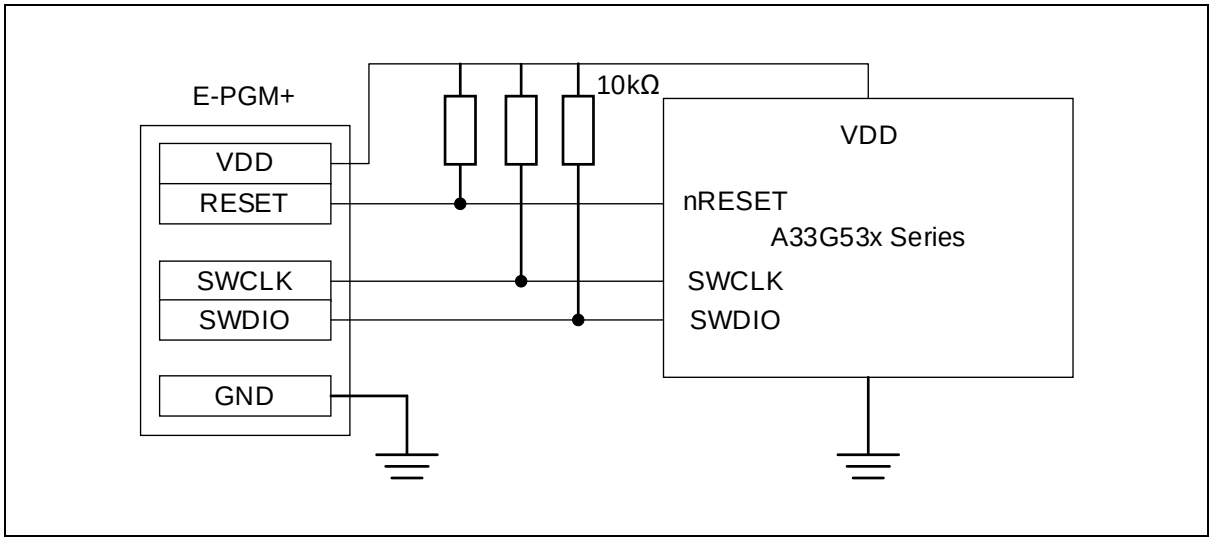
NOTE:

1. Visit www.abovsemi.com and refer to "Tools & Support > Programmer".

1.5.3.3 SWD Debug Mode and E-PGM+ Connection

The connection between the A33G53x series and the SWD debugger interface is illustrated in Figure 3.

Figure 3. A33G53x Series to E-PGM+ Connection using SWD Interface



2. Pinouts and Pin Descriptions

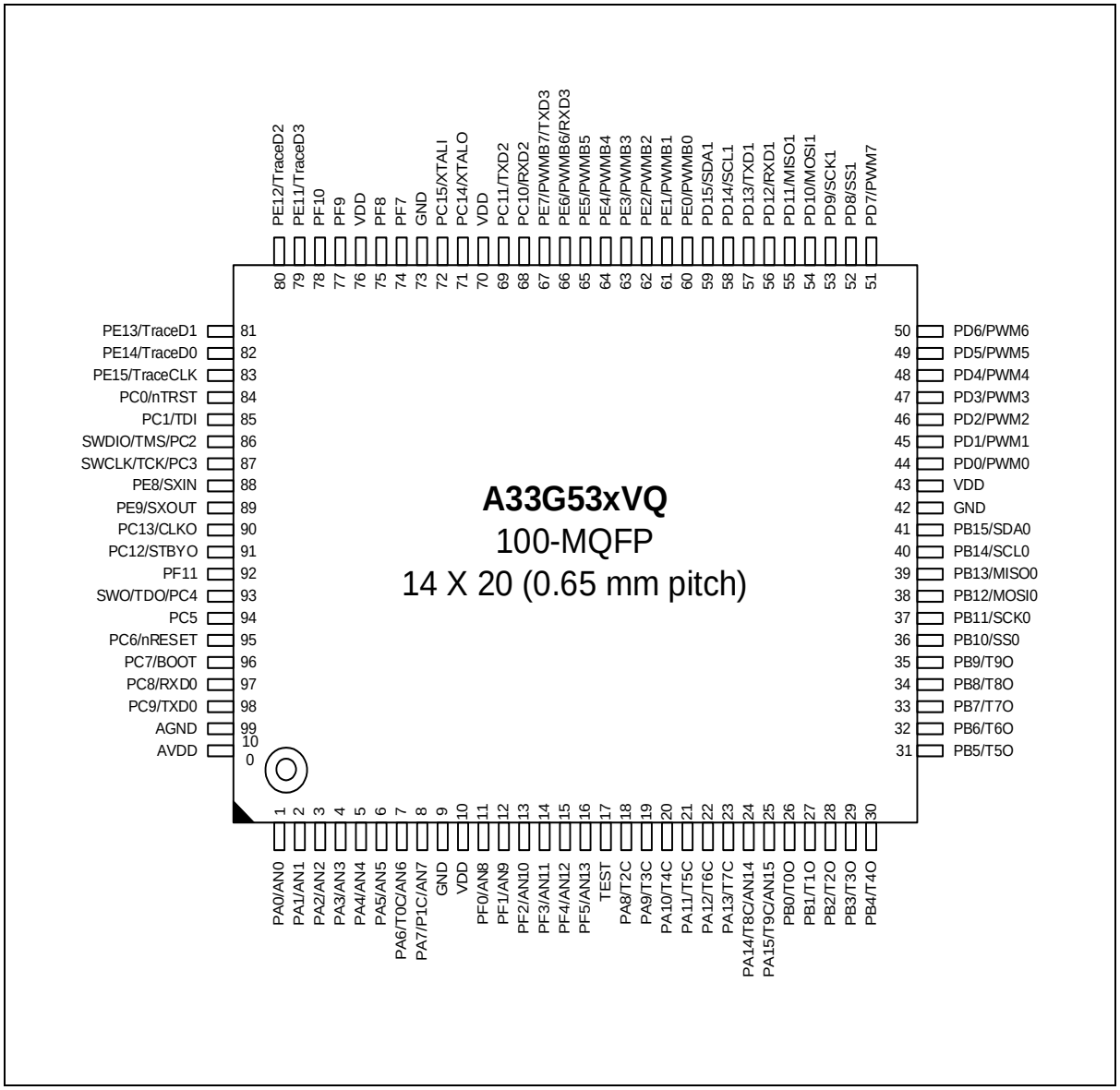
In this chapter, pinouts and pin descriptions of the A33G53x series are introduced.

2.1 Pinouts

Figure 4, Figure 5, Figure 6, and Figure 7 show the top views of the packages.

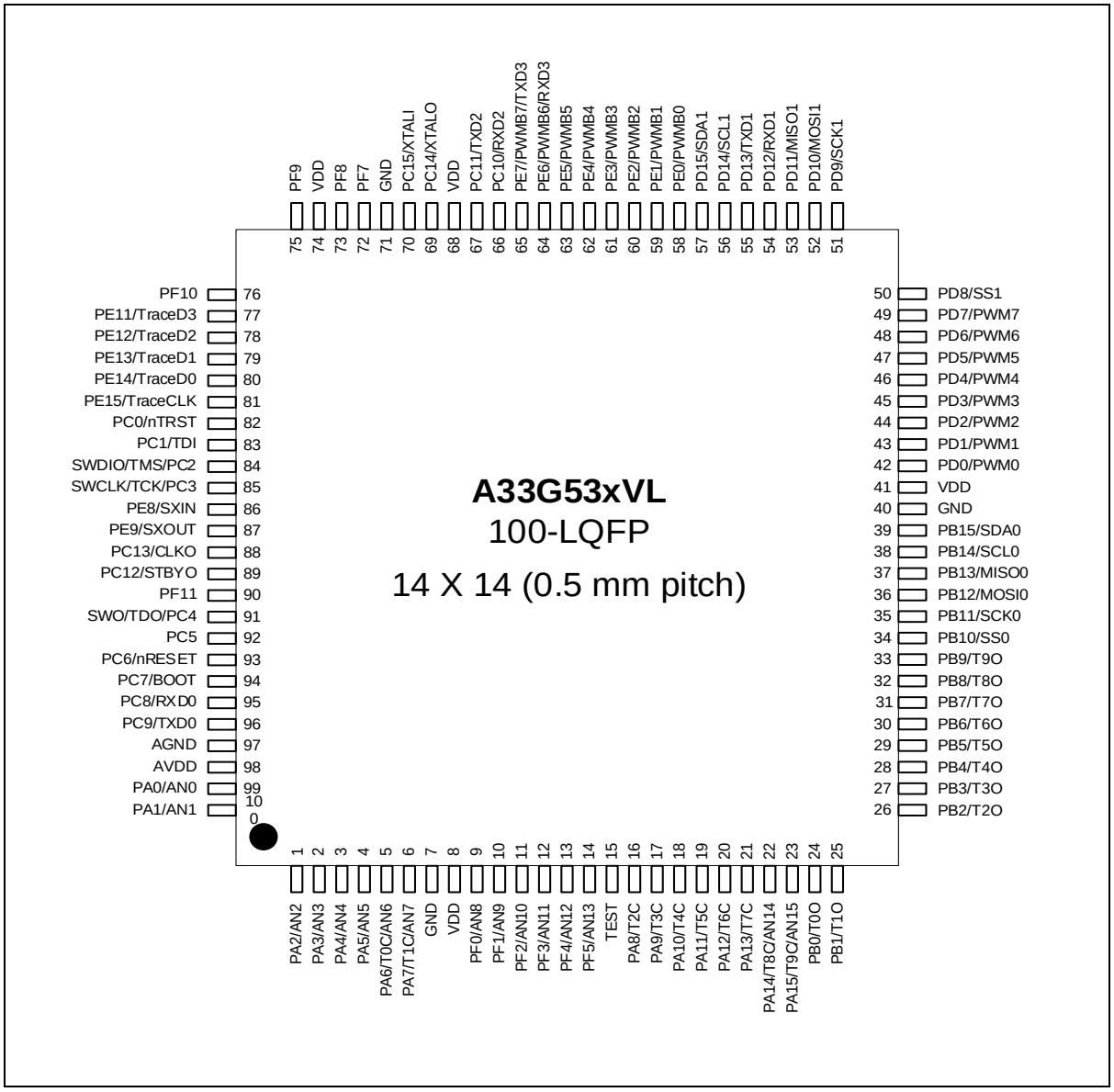
2.1.1 A33G539VQ / A33G538VQ (100-MQFP)

Figure 4. 100-MQFP Pinouts



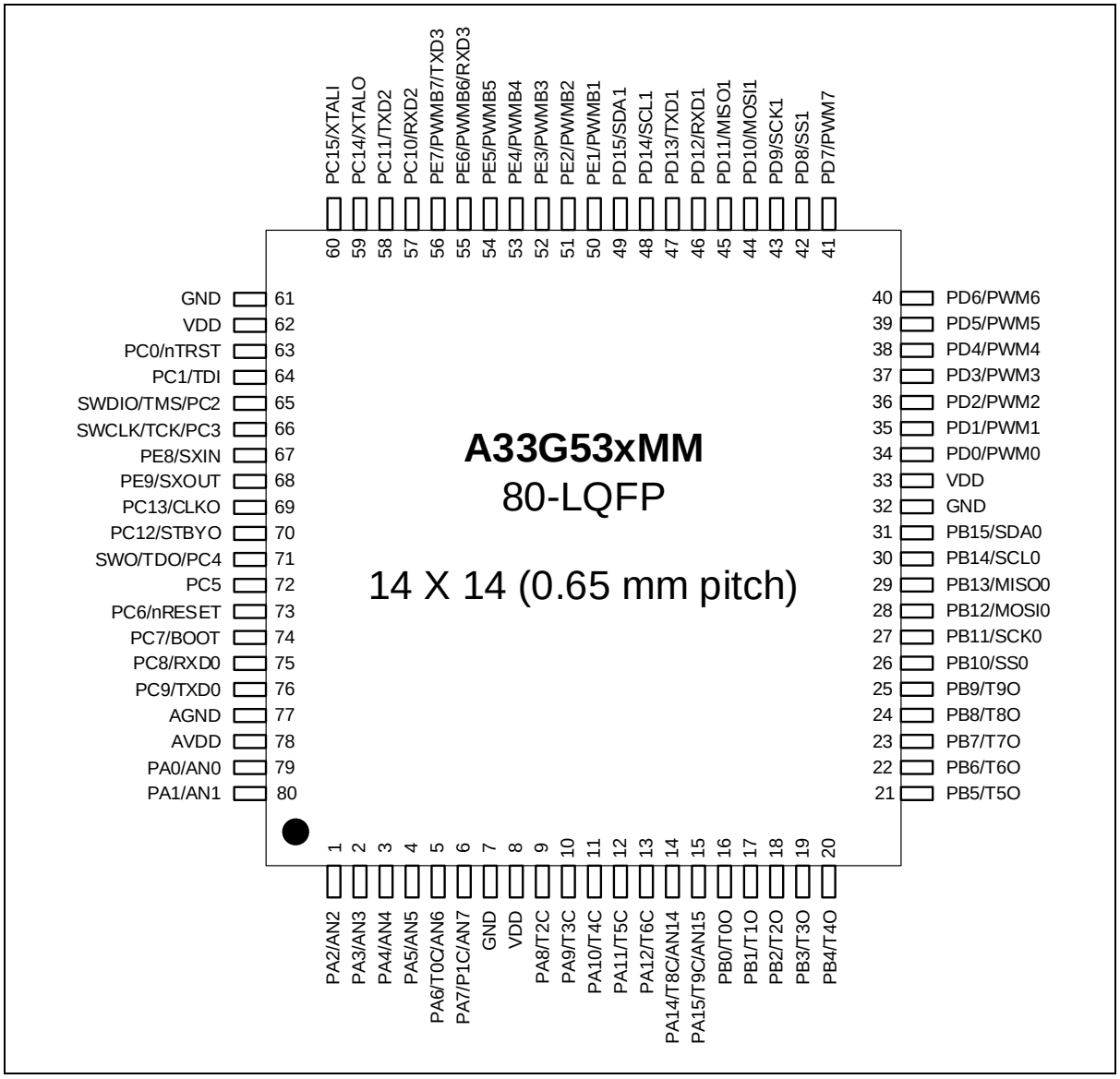
2.1.2 A33G539VL / A33G538VL (100-LQFP)

Figure 5. 100-LQFP Pinouts



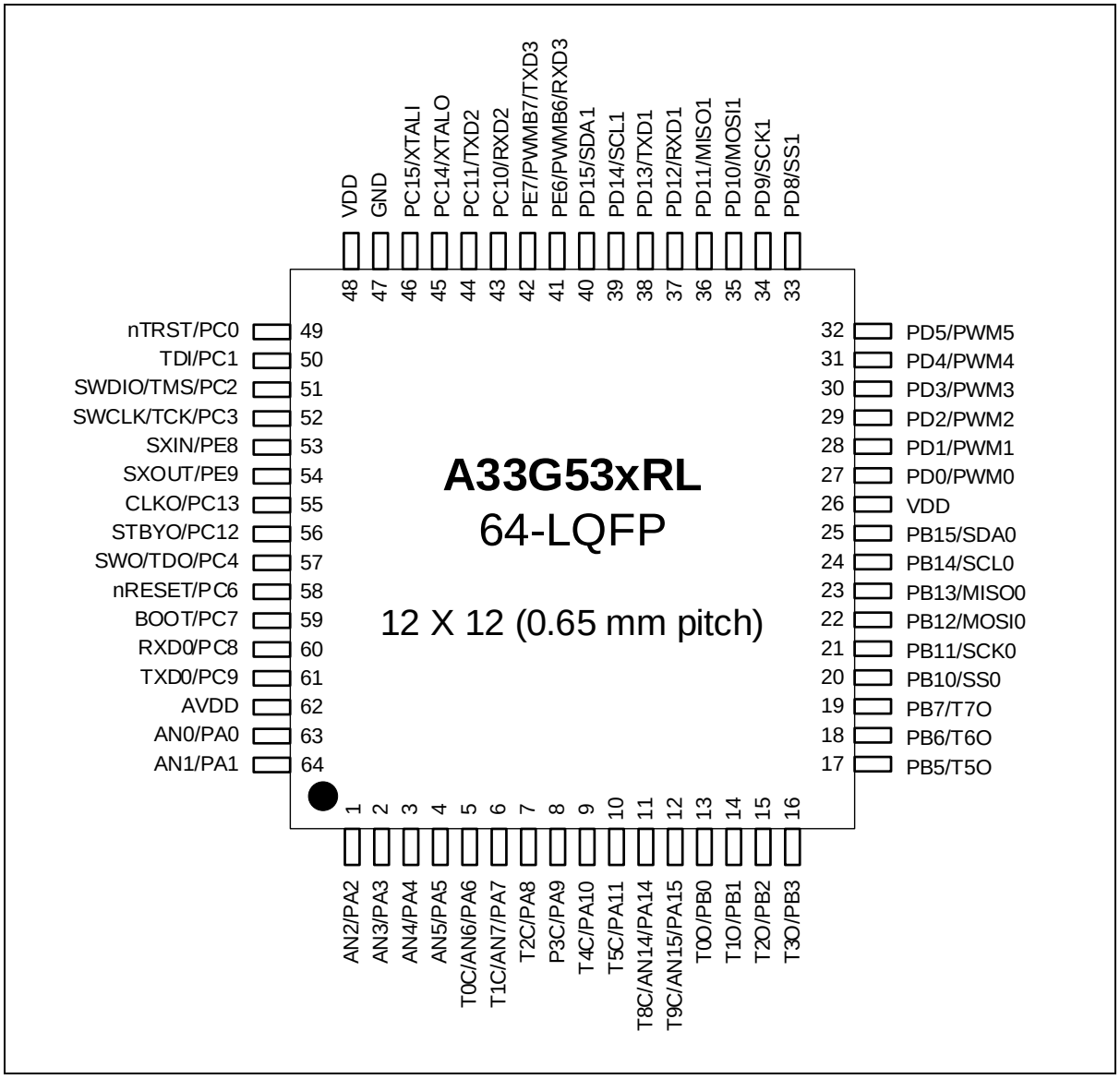
2.1.3 A33G539MM / A33G538MM (80-LQFP14)

Figure 6. 80-LQFP14 Pinouts



2.1.4 A33G539RL / A33G538RL (64-LQFP12)

Figure 7. 64-LQFP12 Pinouts



2.2 Pin Description

Table 8. Legend and Abbreviations used in Pin Description

Name	Definition	
Pin name	Unless otherwise specified in parentheses under the pin name, the pin name is fixed and always the same. Users can set a function on the pin using the alternate function.	
Pin type	I	Input
	O	Output
	U	Pull-up
	D	Pull-down
	S	Schmitt-trigger Input
	C	CMOS Input
	A	Analog
	P	Power
Notes	• After a reset, all the pins are configured to work for the function defined by their initial values. The initial value of the pin depends on the package type. This configuration complies with the 100-pin standard. • PC0 (nTRST), PC1 (TDI), PC2 (TMS/ SWDIO), PC3 (TCK/ SWCLK) and nRESET (PC6) are the default pull-up pins. • Do not configure unused pins as floating inputs. (We recommend configuring them as low outputs.) • Because the boot pin is a floating input after reset, it requires an external pull-down of 10 kΩ. • After reset, the internal pull-ups for the serial wire clock (SWCLK) and serial wire data I/O (SWDIO) are enabled. • The SWCLK and SWDIO pins should not be switched to other functions while they are being used. • If the PC14 (XTALO), PC15 (XTALI), PE8 (SXIN), and PE9 (SXOUT) pins are configured for functions other than a clock, and the clock is enabled by software, other functions may not operate properly. • The TEST pin requires a pull-down (0 to 10 kΩ) or should be connected to GND.	
Alternate functions	Functions selected through PnMR (PORT n pin multiplexer register) registers	

The pin configuration information in Table 9 contains two pairs of power/ground and other dedicated pins. The multi-function pins have up to five selections of functions, including GPIO. Configuration, including pin ordering, can be changed without notice.

Table 9. Pin Description

Pin No.				Pin Name	Type	Description	Remark
100-MQ	100-LQ	80-pin	64-pin				
99	1	79	63	PA0*	IOUS	GPIO A Bit 0 Input/ Output	
				AN0	IA	Analog Input 0	
100	2	80	64	PA1*	IOUS	GPIO A Bit 1 Input/ Output	
				AN1	IA	Analog Input 1	
1	3	1	1	PA2*	IOUS	GPIO A Bit 2 Input/ Output	
				AN2	IA	Analog Input 2	
2	4	2	2	PA3*	IOUS	GPIO A Bit 3 Input/ Output	
				AN3	IA	Analog Input 3	
3	5	3	3	PA4*	IOUS	GPIO A Bit 4 Input/ Output	
				AN4	IA	Analog Input 4	
4	6	4	4	PA5*	IOUS	GPIO A Bit 5 Input/ Output	
				AN5	IA	Analog Input 5	
5	7	5	5	PA6*	IOUS	GPIO A Bit 6 Input/ Output	
				T0C	IPUS	Timer 0 Clock/Capture input	
				AN6	IA	Analog Input 6	
6	8	6	6	PA7*	IOUS	GPIO A Bit 7 Input/ Output	
				T1C	IUS	Timer 1 Clock/Capture input	
				AN7	IA	Analog Input 7	
7	9	7	-	GND	P	Ground	
8	10	8	-	VDD	P	VDD (3.0 ~ 5.5 V)	
9	11	-	-	PF0*	IOUS	GPIO F Bit 0 Input/ Output	
				AN8	IA	Analog Input 8	
10	12	-	-	PF1*	IOUS	GPIO F Bit 1 Input/ Output	
				AN9	IA	Analog Input 9	
11	13	-	-	PF2*	IOUS	GPIO F Bit 2 Input/ Output	
				AN10	IA	Analog Input 10	
12	14	-	-	PF3*	IOUS	GPIO F Bit 3 Input/ Output	
				AN11	IA	Analog Input 11	
13	15	-	-	PF4*	IOUS	GPIO F Bit 4 Input/ Output	
				AN12	IA	Analog Input 12	
14	16	-	-	PF5*	IOUS	GPIO F Bit 5 Input/ Output	
				AN13	IA	Analog Input 13	
15	17	-	-	TEST	IDS	Test mode input (Default Pull-down)	
16	18	9	7	PA8*	IOUS	GPIO A Bit 8 Input/ Output	
				T2C	IUS	Timer 2 Clock/Capture input	
17	19	10	8	PA9*	IOUS	GPIO A Bit 9 Input/ Output	
				T3C	IUS	Timer 3 Clock/Capture input	
18	20	11	9	PA10*	IOUS	GPIO A Bit 10 Input/ Output	
				T4C	IUS	Timer 4 Clock/Capture input	

Table 9. Pin Description (continued)

Pin No.				Pin Name	Type	Description	Remark
100-MQ	100-LQ	80-pin	64-pin				
19	21	12	10	PA11*	IOUS	GPIO A Bit 11 Input/ Output	
				T5C	IUS	Timer 5 Clock/Capture input	
20	22	13	-	PA12*	IOUS	GPIO A Bit 12 Input/ Output	
				T6C	IUS	Timer 6 Clock/Capture input	
21	23	-	-	PA13*	IOUS	GPIO A Bit 13 Input/ Output	
				T7C	IUS	Timer 7 Clock/Capture input	
22	24	14	11	PA14*	IOUS	GPIO A Bit 14 Input/ Output	
				T8C	IUS	Timer 8 Clock/Capture input	
				AN14	IA	Analog Input 14	
23	25	15	12	PA15*	IOUS	GPIO A Bit 15 Input/ Output	
				T9C	IUS	Timer 9 Clock/Capture input	
				AN15	IA	Analog Input 14	
24	26	16	13	PB0*	IOUS	GPIO B Bit 0 Input/ Output	
				T0O	OUS	Timer 0 Output	
25	27	17	14	PB1*	IOUS	GPIO B Bit 1 Input/ Output	
				T1O	OUS	Timer 1 Output	
26	28	18	15	PB2*	IOUS	GPIO B Bit 2 Input/ Output	
				T2O	OUS	Timer 2 Output	
27	29	19	16	PB3*	IOUS	GPIO B Bit 3 Input/ Output	
				T3O	OUS	Timer 3 Output	
28	30	20	-	PB4*	IOUS	GPIO B Bit 4 Input/ Output	
				T4O	OUS	Timer 4 Output	
29	31	21	17	PB5*	IOUS	GPIO B Bit 5 Input/ Output	
				T5O	OUS	Timer 5 Output	
30	32	22	18	PB6*	IOUS	GPIO B Bit 6 Input/ Output	
				T6O	OUS	Timer 6 Output	
31	33	23	19	PB7*	IOUS	GPIO B Bit 7 Input/ Output	
				T7O	OUS	Timer 7 Output	
32	34	24	-	PB8*	IOUS	GPIO B Bit 8 Input/ Output	
				T8O	OUS	Timer 8 Output	
33	35	25	-	PB9*	IOUS	GPIO B Bit 9 Input/ Output	
				T9O	OUS	Timer 9 Output	
34	36	26	20	PB10*	IOUS	GPIO B Bit 10 Input/ Output	
				SS0	IOUS	SPI Channel 0 Select Signal Input/ Output	
35	37	27	21	PB11*	IOUS	GPIO B bit 11 Input/ Output	
				SCK0	IOUS	SPI Channel 0 Clock Signal Input/ Output	
36	38	28	22	PB12*	IOUS	GPIO B bit 12 Input/ Output	
				MOSI0	IOUS	SPI Channel 0 Master Out/Slave In Signal	
37	39	29	23	PB13*	IOUS	GPIO B bit 13 Input/ Output	
				MISO0	IOUS	SPI Channel 0 Master In/Slave Out Signal	
38	40	30	24	PB14*	IOUS	GPIO B bit 14 Input/ Output	
				SCL0	OUS	I2C Channel 0 SCL Signal	

Table 9. Pin Description (continued)

Pin No.				Pin Name	Type	Description	Remark
100-MQ	100-LQ	80-pin	64-pin				
39	41	31	25	PB15*	IOUS	GPIO B bit 15 Input/ Output	
				SDA0	OUS	I2C Channel 0 SDA Signal	
40	42	32	-	GND	P	Ground	
41	43	33	26	VDD	P	VDD (3.0 ~ 5.5V)	
42	44	34	27	PD0*	IOUC	GPIO D bit 0 Input/ Output	
				PWM0	OUC	PWM Channel 0 Output	
43	45	35	28	PD1*	IOUC	GPIO D bit 1 Input/ Output	
				PWM1	OUC	PWM Channel 1 Output	
44	46	36	29	PD2*	IOUC	GPIO D bit 2 Input/ Output	
				PWM2	OUC	PWM Channel 2 Output	
45	47	37	30	PD3*	IOUC	GPIO D bit 3 Input/ Output	
				PWM3	OUC	PWM Channel 3 Output	
46	48	38	31	PD4*	IOUC	GPIO D bit 4 Input/ Output	
				PWM4	OUC	PWM Channel 4 Output	
47	49	39	32	PD5*	IOUC	GPIO D bit 5 Input/ Output	
				PWM5	OUC	PWM Channel 5 Output	
48	50	40	-	PD6*	IOUC	GPIO D bit 6 Input/ Output	
				PWM6	OUC	PWM Channel 6 Output	
49	51	41	-	PD7*	IOUC	GPIO D bit 7 Input/ Output	
				PWM7	OUC	PWM Channel 7 Output	
50	52	42	33	PD8*	IOUC	GPIO D bit 8 Input/ Output	
				SS1	IOUC	SPI Channel 1 Select Signal Input/ Output	
51	53	43	34	PD9*	IOUC	GPIO D bit 9 Input/ Output	
				SCK1	IOUC	SPI Channel 1 Clock Signal Input/ Output	
52	54	44	35	PD10*	IOUC	GPIO D bit 10 Input/ Output	
				MOSI1	IOUC	SPI Channel 1 Master Out/Slave In Signal	
53	55	45	36	PD11*	IOUC	GPIO D bit 11 Input/ Output	
				MISO1	IOUC	SPI Channel 1 Master In/Slave Out Signal	
54	56	46	37	PD12*	IOUC	GPIO D bit 12 Input/ Output	
				RXD1	IUC	UART Channel 1 Receive Data Input	
55	57	47	38	PD13*	IOUC	GPIO D bit 13 Input/ Output	
				TXD1	OUC	UART Channel 1 Transmit Data Output	
56	58	48	39	PD14*	IOUC	GPIO D bit 14 Input/ Output	
				SCL1	OUC	I2C Channel 1 SCL Signal	
57	59	49	40	PD15*	IOUC	GPIO D bit 15 Input/ Output	
				SDA1	OUC	I2C Channel 1 SDA Signal	
58	60	-	-	PE0*	IOUS	GPIO E bit 0 Input/ Output	
				PWMB0	OUS	PWM Channel 0 Inversion Output	
59	61	50	-	PE1*	IOUS	GPIO E bit 1 Input/ Output	
				PWMB1	OUS	PWM Channel 1 Inversion Output	
60	62	51	-	PE2*	IOUS	GPIO E bit 2 Input/ Output	
				PWMB2	OUS	PWM Channel 2 Inversion Output	

Table 9. Pin Description (continued)

Pin No.				Pin Name	Type	Description	Remark
100-MQ	100-LQ	80-pin	64-pin				
61	63	52	-	PE3*	IOUS	GPIO E bit 3 Input/ Output	
				PWMB3	OUS	PWM Channel 3 Inversion Output	
62	64	53	-	PE4*	IOUS	GPIO E bit 4 Input/ Output	
				PWMB4	OUS	PWM Channel 4 Inversion Output	
63	65	54	-	PE5*	IOUS	GPIO E bit 5 Input/ Output	
				PWMB5	OUS	PWM Channel 5 Inversion Output	
64	66	55	41	PE6*	IOUS	GPIO E bit 6 Input/ Output	
				PWMB6	OUS	PWM Channel 6 Inversion Output	
				RXD3	IUS	UART Channel 3 Receive Data Input	
65	67	56	42	PE7*	IOUS	GPIO E bit 7 Input/ Output	
				PWMB7	OUS	PWM Channel 7 Inversion Output	
				TXD3	OUS	UART Channel 3 Transmit Data Output	
66	68	57	43	PC10*	IOUS	GPIO C bit 10 Input/ Output	
				RXD2	IUS	UART Channel 2 Receive Data Input	
67	69	58	44	PC11*	IOUS	GPIO C bit 11 Input/ Output	
				TXD2	OUS	UART Channel 2 Transmit Data Output	
68	70	-	-	VDD	P	VDD (3.0 ~ 5.5 V)	
69	71	59	45	PC14*	IOUS	GPIO C bit 14 Input/ Output	
				XTALO	IA	Main Crystal Oscillator Output (4/8/10MHz)	
70	72	60	46	PC15*	IOUS	GPIO C bit 14 Input/ Output	
				XTALI	IA	Main Crystal Oscillator Input (4/8/10MHz)	
71	73	61	47	GND	P	Ground	
72	74	-	-	PF7	IOUS	GPIO F bit 7 Input/ Output	
73	75	-	-	PF8	IOUS	GPIO F bit 8 Input/ Output	
74	76	62	48	VDD	P	VDD (3.0 ~5.5 V)	
75	77	-	-	PF9	IOUS	GPIO F bit 9 Input/ Output	
76	78	-	-	PF10	IOUS	GPIO F bit 10 Input/ Output	
77	79	-	-	PE11*	IOUS	GPIO E bit 11 Input/ Output	
				TraceD3	IOUS	ETM Trace Data 3	
78	80	-	-	PE12*	IOUS	GPIO E bit 12 Input/ Output	
				TraceD2	IOUS	ETM Trace Data 2	
79	81	-	-	PE13*	IOUS	GPIO E bit 13 Input/ Output	
				TraceD1	IOUS	ETM Trace Data 1	
80	82	-	-	PE14*	IOUS	GPIO E bit 14 Input/ Output	
				TraceD0	IOUS	ETM Trace Data 0	
81	83	-	-	PE15*	IOUS	GPIO E bit 15 Input/ Output	
				TraceCLK	IOUS	ETM Trace Clock	
82	84	63	49	PC0	IOUS	GPIO C bit 0 Input/ Output	
				nTRST*	IUS	JTAG nTRST Signal Input	Pull-up
83	85	64	50	PC1	IOUS	GPIO C bit 1 Input/ Output	
				TDI*	IUS	JTAG TDI Signal Input	Pull-up

Table 9. Pin Description (continued)

Pin No.				Pin Name	Type	Description	Remark
100-MQ	100-LQ	80-pin	64-pin				
84	86	65	51	PC2	IOUS	GPIO C bit 2 Input/ Output	
				TMS/SWDIO*	IUS	JTAG TMS, SWD Data Input/ Output	Pull-up
85	87	66	52	PC3	IOUS	GPIO C bit 3 Input/ Output	
				TCK/SWCLK*	IUS	JTAG TCK, SWD Clock Input	Pull-up
86	88	67	53	PE8*	IOUS	GPIO E bit 8 Input/ Output	
				SXIN	IA	Sub Crystal Oscillator Signal Input (32.768kHz)	
87	89	68	54	PE9*	IOUS	GPIO E bit 9 Input/ Output	
				SXOUT	IA	Sub Crystal Oscillator Signal Output (32.768kHz)	
88	90	69	55	PC13*	IOUS	GPIO C bit 13 Input/ Output	
				CLKO	OUS	External Clock Output	
89	91	70	56	PC12*	IOUS	GPIO C bit 12 Input/ Output	
				STBYO	OUS	Stand-by(Power-down) Indication Output Signal	
90	92	-	-	PF11	IOUS	GPIO F bit 11 Input/ Output	
91	93	71	57	PC4	IOUS	GPIO C bit 4 Input/ Output	
				TDO/SWO*	OUS	JTAG TDO, SWO Signal Output	
92	94	72	-	PC5	IOUS	GPIO C bit 5 Input/ Output	
93	95	73	58	PC6	IOUS	GPIO C bit 6 Input/ Output	
				nRESET*	IUS	Reset Input	Pull-up
94	96	74	59	PC7	IOUS	GPIO C bit 7 Input/ Output	
				BOOT*	IUS	Boot Signal input (input mode when reset)	
95	97	75	60	PC8	IOUS	GPIO C bit 8 Input/ Output	
				RXD0*	IUS	UART Channel 0 Receive Data Input	
96	98	76	61	PC9	IOUS	GPIO C bit 9 Input/ Output	
				TXD0*	OUS	UART Channel 0 Transmit Data Input	
97	99	77	-	AGND	P	ADC/Analog Ground	
98	100	78	62	AVDD	P	ADC/Analog VDD	

2.3 Alternate Function Pins

The GPIO pins have alternate functions, as described in Table 10.

Table 10. GPIO Alternate Function

Pin Name	Alternate Function			
	AF0	AF1	AF2	AF3
PA0	PA0 (1)			AN0
PA1	PA1 (1)			AN1
PA2	PA2 (1)			AN2
PA3	PA3 (1)			AN3
PA4	PA4 (1)			AN4
PA5	PA5 (1)			AN5
PA6	PA6 (1)	T0C		AN6
PA7	PA7 (1)	T1C		AN7
PA8	PA8 (1)	T2C		
PA9	PA9 (1)	T3C		
PA10	PA10 (1)	T4C		
PA11	PA11 (1)	T5C		
PA12	PA12 (1)	T6C		
PA13	PA13 (1)	T7C		
PA14	PA14 (1)	T8C		AN14
PA15	PA15 (1)	T9C		AN15
PB0	PB0 (1)	T0O		
PB1	PB1 (1)	T1O		
PB2	PB2 (1)	T2O		
PB3	PB3 (1)	T3O		
PB4	PB4 (1)	T4O		
PB5	PB5 (1)	T5O		
PB6	PB6 (1)	T6O		
PB7	PB7 (1)	T7O		
PB8	PB8 (1)	T8O		
PB9	PB9 (1)	T9O		
PB10	PB10 (1)	SS0		
PB11	PB11 (1)	SCK0		
PB12	PB12 (1)	MOSI0		
PB13	PB13 (1)	MISO0		
PB14	PB14 (1)	SCL0		
PB15	PB15 (1)	SDA0		

Table 10. GPIO Alternate Function (continued)

Pin Name	Alternate Function			
	AF0	AF1	AF2	AF3
PC0	PC0	nTRST (1)		
PC1	PC1	TDI (1)		
PC2	PC2	TMS (SWDIO) (1)		
PC3	PC3	TCK (SWCLK) (1)		
PC4	PC4	TDO (SWO) (1)		
PC5	PC5 (1)			
PC6	PC6	nRESET (1)		
PC7	PC7/BOOT (1)			
PC8	PC8 (1)	RXD0		
PC9	PC9 (1)	TXD0		
PC10	PC10 (1)	RXD2		
PC11	PC11 (1)	TXD2		
PC12	PC12 (1)	STBYO		
PC13	PC13 (1)	CLKO		
PC14	PC14 (1)	XTALO		
PC15	PC15 (1)	XTALI		
PD0	PD0 (1)	PWMA0		
PD1	PD1 (1)	PWMA1		
PD2	PD2 (1)	PWMA2		
PD3	PD3 (1)	PWMA3		
PD4	PD4 (1)	PWMA4		
PD5	PD5 (1)	PWMA5		
PD6	PD6 (1)	PWMA6		
PD7	PD7 (1)	PWMA7		
PD8	PD8 (1)	SS1		
PD9	PD9 (1)	SCK1		
PD10	PD10 (1)	MOSI1		
PD11	PD11 (1)	MISO1		
PD12	PD12 (1)	RXD1		
PD13	PD13 (1)	TXD1		
PD14	PD14 (1)	SCL1		
PD15	PD15 (1)	SDA1		

Table 10. GPIO Alternate Function (continued)

Pin Name	Alternate Function			
	AF0	AF1	AF2	AF3
PE0	PE0 (1)	PWM0B		
PE1	PE1 (1)	PWM1B		
PE2	PE2 (1)	PWM2B		
PE3	PE3 (1)	PWM3B		
PE4	PE4 (1)	PWM4B		
PE5	PE5 (1)	PWM5B		
PE6	PE6 (1)	PWM6B	RXD3	
PE7	PE7 (1)	PWM7B	TXD3	
PE8	PE8 (1)	SXIN		
PE9	PE9 (1)	SXOUT		
-	-	-	-	-
PE11	PE11 (1)	TraceD3		
PE12	PE12 (1)	TraceD2		
PE13	PE13 (1)	TraceD1		
PE14	PE14 (1)	TraceD0		
PE15	PE15 (1)	TraceCLK		
PF0	PF0 (1)			AN8
PF1	PF1 (1)			AN9
PF2	PF2 (1)			AN10
PF3	PF3 (1)			AN11
PF4	PF4 (1)			AN12
PF5	PF5 (1)			AN13
-	-	-	-	-
PF7	PF7 (1)			
PF8	PF8 (1)			
PF9	PF9 (1)			
PF10	PF10 (1)			
PF11	PF11 (1)			
-	-	-	-	-
-	-	-	-	-
-	-	-	-	-
-	-	-	-	-

NOTES:

1. It means 'selected pin function after reset condition'. (The initial value of the pin depends on the package type.)
2. The unused pins are set to outputs using firmware. (Setting them to low outputs is recommended).
3. PE10, PF6, and PF12 ~ PF15 pins are not available.

3. Electrical Characteristics

3.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to GND.

3.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions of ambient temperature, supply voltage, and frequency.

Data based on characterization results, design simulation, and/or technical characteristics are not tested in production but are indicated in the table footnotes.

3.1.2 Typical Values

Unless otherwise specified, typical data are based on the conditions of T_A = 25°C and VDD = AVDD = 5.0 V. The typical data are provided only as design recommendations and are not tested.

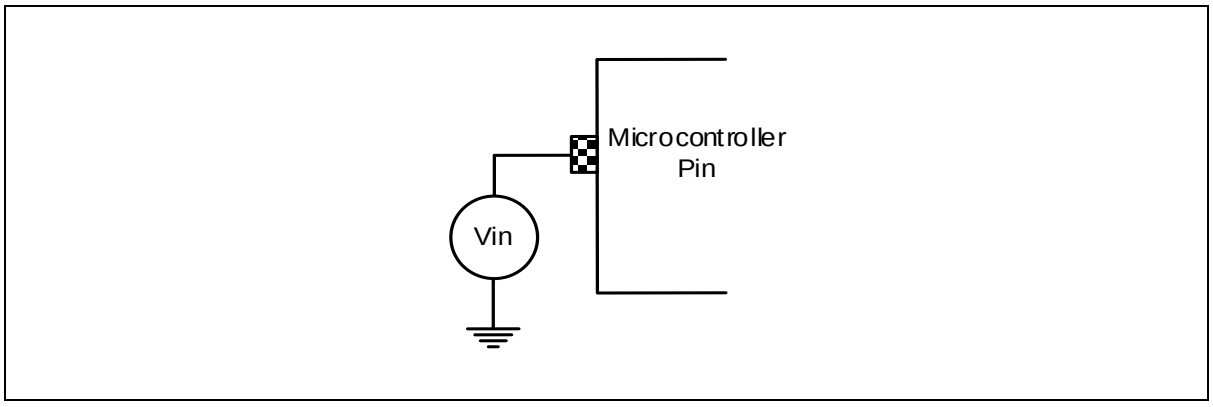
3.1.3 Typical Curves

Unless otherwise specified, all typical curves are provided only as design recommendations and are not tested.

3.1.4 Pin Input Voltage

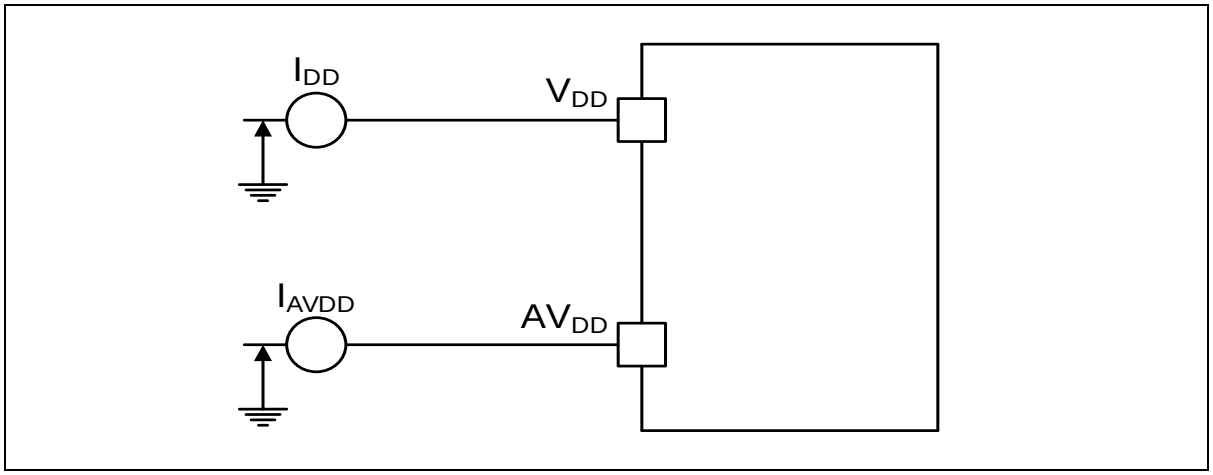
The input voltage measurement on a pin of the device is described in Figure 8.

Figure 8. Pin Input Voltage



3.1.5 Current Consumption Measurement

Figure 9. Current Consumption Measurement

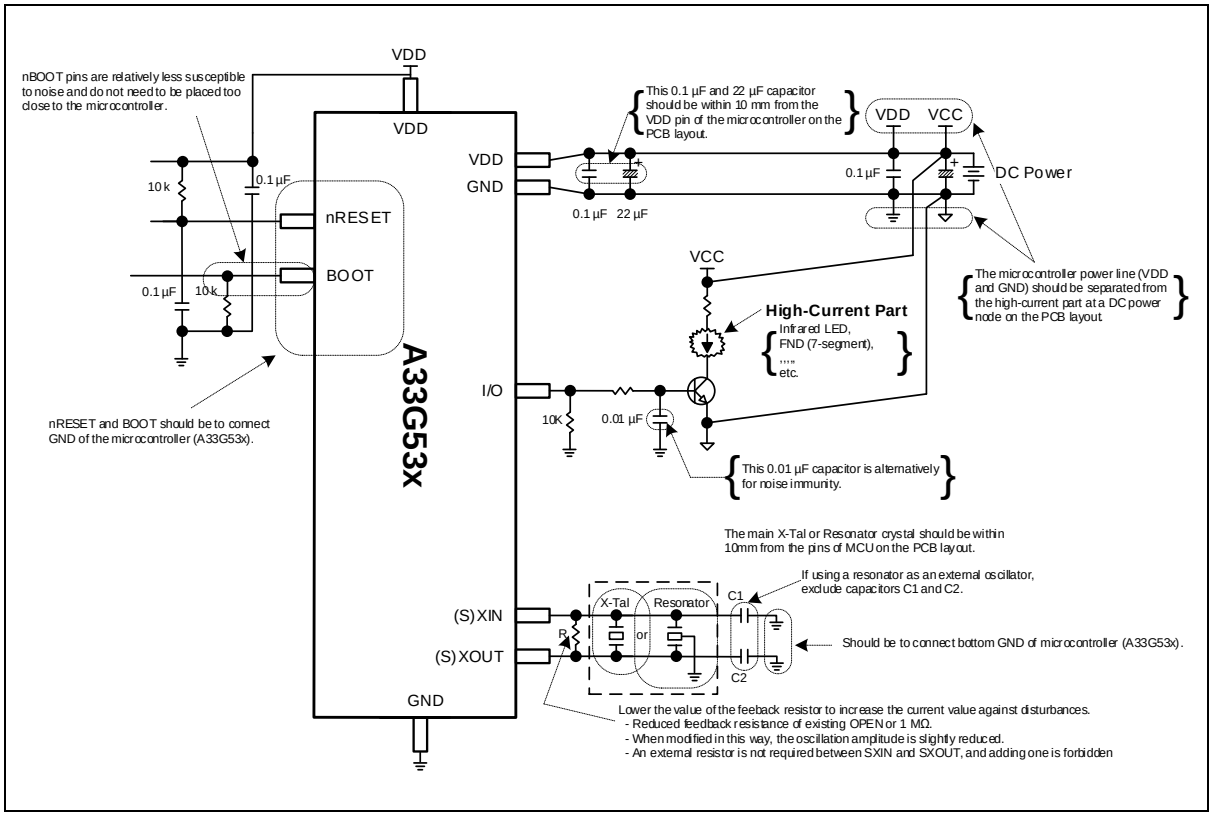


NOTE:

1. The IDD and IAVDD parameters represent the total microcontroller consumption, including the current supplying VDD and AVDD.

3.1.6 Power Supply Diagram

Figure 10. Power Supply Diagram



NOTE:

1. As shown above, each power supply pair (VDD/GND, etc.) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

3.2 Absolute Maximum Ratings

Exceeding stresses specified in Table 11 for Absolute maximum ratings characteristics may result in permanent damage to the device. The values in the tables are stress ratings only and do not imply that the device will function properly under these conditions. Prolonged exposure to these maximum rating conditions may impact the device's reliability. It is important to operate the device within its specified maximum ratings to ensure reliable performance.

Table 11. Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}(1)	Digital power supply	−0.3 ~ +6.5	V
AV_{DD}(1)	Analog power supply	−0.3 ~ +5.5	V
V_I(2)	Input voltage on I/O	VSS−0.3 ~ VDD+0.3	V
V_O	Output voltage on I/O	VSS−0.3 ~ VDD+0.3	V
I_{OH}	Output current sink by I/O	10	mA
$\sum I_{OH}$	Total output current sink by sum of all I/Os and control pins(3)	80	mA
I_{OL}	Output current source by I/O	20	mA
$\sum I_{OL}$	Total output current sourced by the sum of all I/Os and control pins(3)	160	mA
f_{XIN}	Input Main Clock Range	8	MHz
f_{PLLOUT}	Operating Frequency	75	MHz
P_T	Total Power Dissipation	600	mW
T_{OP}	Operating Temperature	−40 ~ +85	°C
T_{STG}	Storage Temperature	−45 ~ +125	°C
T_J	Maximum Operating Junction Temperature	105	°C

NOTES:

1. All main power (VDD, AVDD) and ground (GND, AGND) pins must always be connected to the external power supply in the permitted range.
2. The VI maximum value must always be observed.
3. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count packages.

3.3 Operating Condition

3.3.1 General Operating Condition

Table 12. General Operating Condition

(Temperature: −40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Digital Power Supply	4 ~ 75 MHz	3.0(1)	5.0	5.5	V
AV_{DD}	Analog Power Supply	-	3.0	-	VDD	V
T_{OP}	Operating Temperature	VDD = 3.0 V ~ 5.5 V	−40	-	85	°C
f_{REQ}	Operating Frequency	f_{XIN}	-	4	8	MHz
		Internal Ring OSC	0.5	1	1.5	MHz
		Internal OSC	15.36	16	16.64	MHz
		PLL	4	-	75	MHz
t_{rVDD}	Supply Rise Rate	-	-	-	0.05	V/μs
t_{fVDD}	Supply Fall Rate	-	-	-	0.1	V/μs

NOTES:

1. f_{XIN} is the input signal frequency of the PLL. The input signal frequency of the MXOSC can be up to 10 MHz.
2. When RESET is released, functionality is guaranteed up to the Min. value of V_{LVR0}.
3. AGND ≤ ANx (x = 0 to 15) ≤ AVDD ≤ VDD

3.3.2 Power-On Reset Characteristics

Table 13. POR Electrical Characteristics

(Temperature: −40°C to 85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{DD}	Operating current	Typ. < 6uA If always on	-	60	-	nA
V_{set}	POR set level	VDD rising (slow)	1.20	1.40	1.70	V
t_R	VDD voltage rising time	-	0.02	-	20	ms/V
t_F	VDD voltage falling time	-	0.4	-	20	ms/V
V_{reset}	POR reset level	VDD falling (slow)	0.85	1.35	1.60	V

3.3.3 Operating Condition at Power-up/Power-down

The parameters in Table 14 are derived from tests performed under the ambient temperature conditions summarized in Table 12.

Table 14. Operating Condition at Power-up/Power-down

(Temperature: −40°C to 85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	-	0.02	-	20	ms/V
	V_{DD} fall time rate	-	0.4	-	20	ms/V

3.3.4 Embedded Reset and Power Control Block Characteristics (LVDR, LVDI)

The parameters in Table 15 and Table 16 are derived from tests performed under the ambient temperature conditions summarized in Table 12.

Once the VDD level has fallen below the LVD level, the operation before the stabilization time of approximately 200 µs after rising above the LVD voltage is not guaranteed.

The operating timing of LVD is shown below.

Figure 11. Operating Timing of LVD

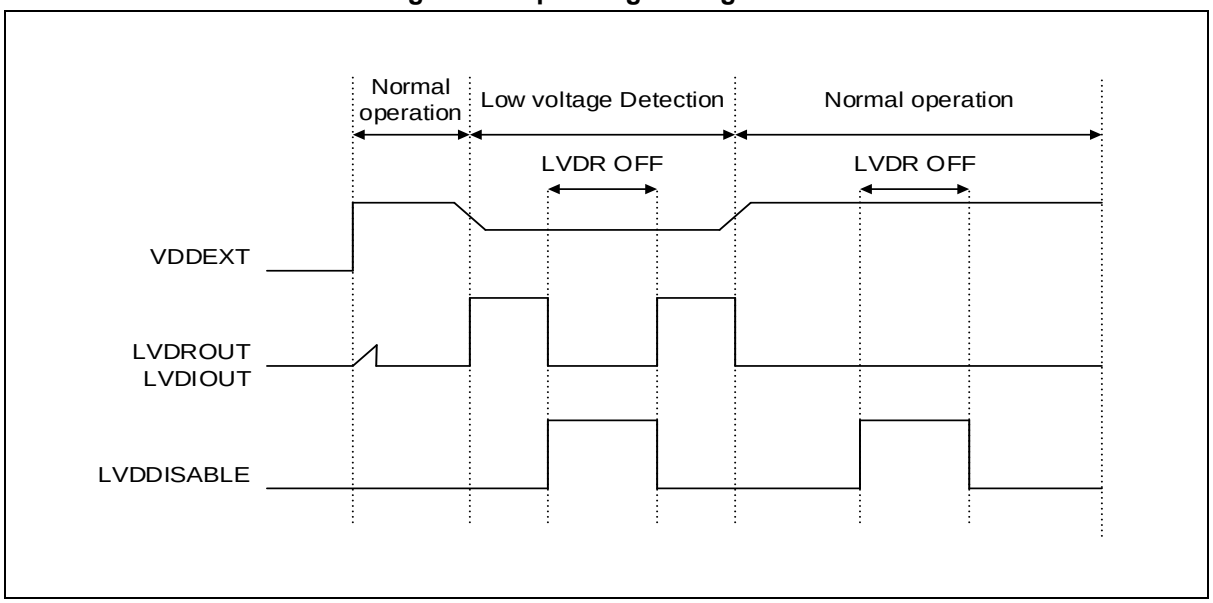


Table 15. Low-Voltage Detector Reset Characteristics

(Temperature: −40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Operation current	-	-	-	50	µA
I_{STOP}	STOP current	-	-	-	-	µA
V_{DET}	LVD Level	2.60 V	−10	-	+10	%
		2.80 V				
		3.00 V				
		3.30 V				
		3.75 V				
		4.00 V				
		4.25 V				
		4.50 V				
V_H	Hysteresis	2 µs delay	-	100	-	mV

3.3.5 Supply Current Characteristics

The amount of current consumed by the device is determined by various factors and parameters, including but not limited to the operating voltage, ambient temperature, load on I/O pins, software configuration, operating frequency, switching rate of I/O pins, location of the program in memory, and the binary code being executed.

The current consumption is measured under the conditions specified in Table 16.

3.3.5.1 Supply Current Consumption

Table 16. Supply Current Characteristics

(Temperature: 25°C)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
		Frequency	Status				
IDD (NORMAL)	Normal operation (Run mode)	ROSC	RUN	-	30	-	mA
		IOSC16	RUN				
		MXOSC	RUN				
		SXOSC	RUN				
IDD (SLEEP)	SLEEP mode (IDLE mode)	ROSC	RUN	-	500	-	μA
		IOSC16	STOP				
		MXOSC	STOP				
		SXOSC	STOP				
IDD (DEEP SLEEP)	DEEP-SLEEP mode (Power-down mode)	ROSC	STOP	-	100	-	μA
		IOSC16	STOP				
		MXOSC	STOP				
		SXOSC	STOP				

NOTE:

1. In DEEP-SLEEP mode, all clocks are disabled.

3.3.5.2 I/O System Current Consumption

The current consumption in the I/O system is due to the two components, Static and Dynamic.

3.3.5.3 I/O Static Current Consumption

All I/O pins used as inputs with pull-ups cause the current consumption when the pins remain Low from the outside. This current consumption value can be calculated simply using the pull-up/pull-down resistor value provided in the I/O port characteristics.

Users need to consider external pull-downs or loads to estimate the current consumption at the output pins.

Additional I/O current consumption can be caused due to the I/Os configured as inputs if the medium voltage level is applied externally. This current is consumed by the input Schmitt trigger circuit used to tell the input value. Unless the application requires a specific configuration, users can prevent this supply current consumption by configuring the I/Os in analog mode instead of using the Schmitt circuit. Specifically, the input pins of the ADC must be configured as analog inputs.

3.3.5.4 I/O Dynamic Current Consumption

The I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply it to the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin.

3.3.6 External Clock Source Characteristics

3.3.6.1 External Main Clock Generated from a Crystal/Ceramic Resonator

External Main Clock (MXOSC) can be supplied with crystal/ceramic resonator oscillators ranging from 4 to 8 MHz. All information in this section is based on the design simulation results obtained by the typical external components specified in Table 17.

The resonator and load capacitor must be placed as close to the oscillator pin as possible to minimize the outputs in the application.

Contact the crystal resonator manufacturer for more information on the distortion, stabilization time, and resonator characteristics (frequency, package, and accuracy).

Table 17. External Main Oscillator Characteristics(1)

(Temperature: −40°C to 85°C)

Symbol	Parameter	Conditions(2)	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	-	3.0	5.0	5.5	V
I_{DD}	MXOSC Current Consumption	VDD = 5 V f_{OUT} = 8 MHz	-	500*	1000	μA
f_{OUT}	Operating Frequency	-	4	8	10	MHz
V_{XOUT}	Output Voltage	-	0.8 VDD	-	-	V
I_{XOUT}	Output Current	-	3**	-	-	mA
C_L	External Load Capacitor	-	-	18 / 22	35	pF

NOTES:

1. Guaranteed by design.
2. Resonator characteristics provided by the crystal/ceramic resonator manufacturer.
3. * The swing scheme changed from Half-Swing to Full-Swing: the IDD current was adjusted.
4. ** Output Current (IXOUT) indicates the current driving capacity of the transistor that constitutes the oscillation part.

Figure 12. Crystal/Ceramic Oscillator

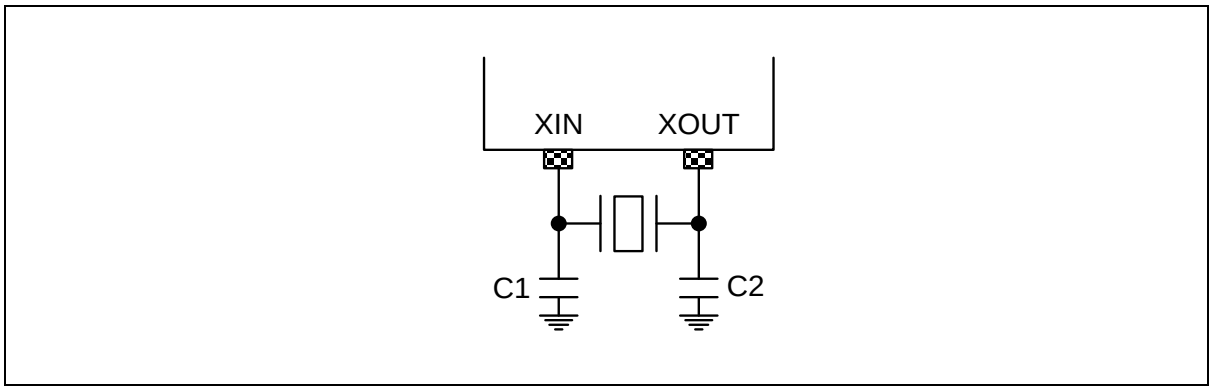


Figure 13. External Clock

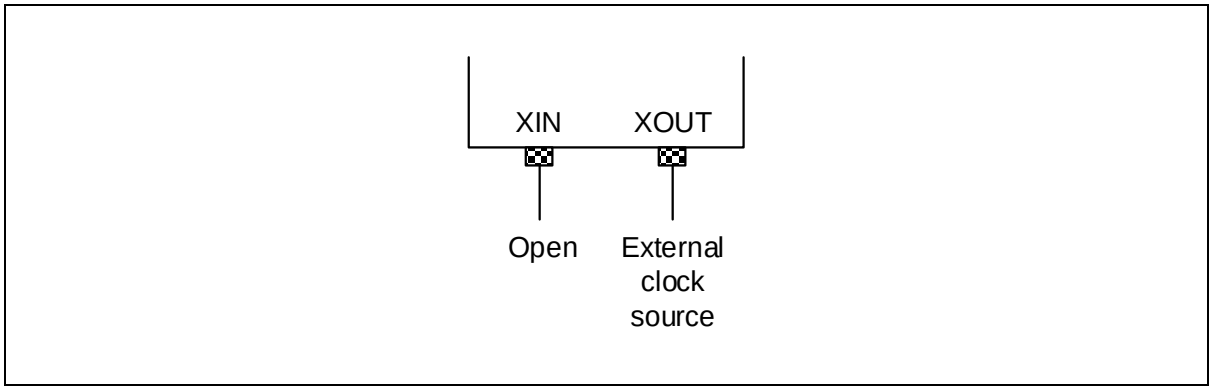
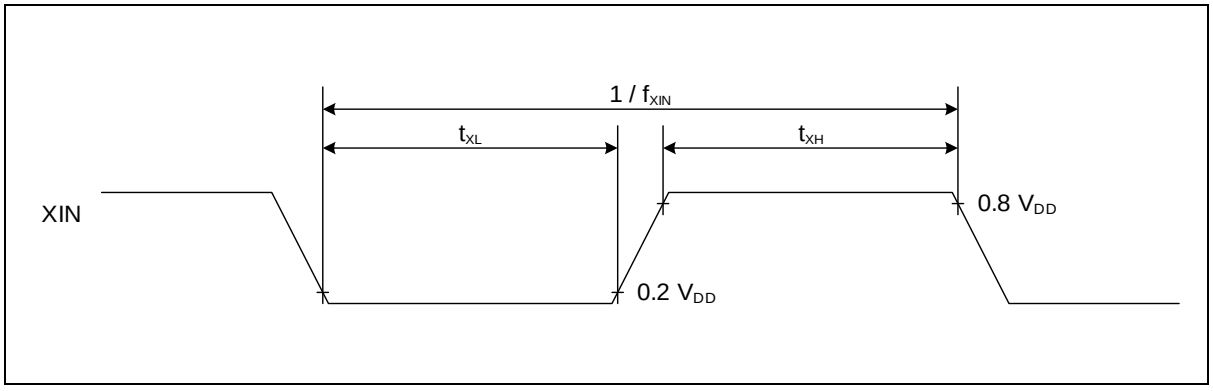


Figure 14. Clock Timing Measurement at XIN

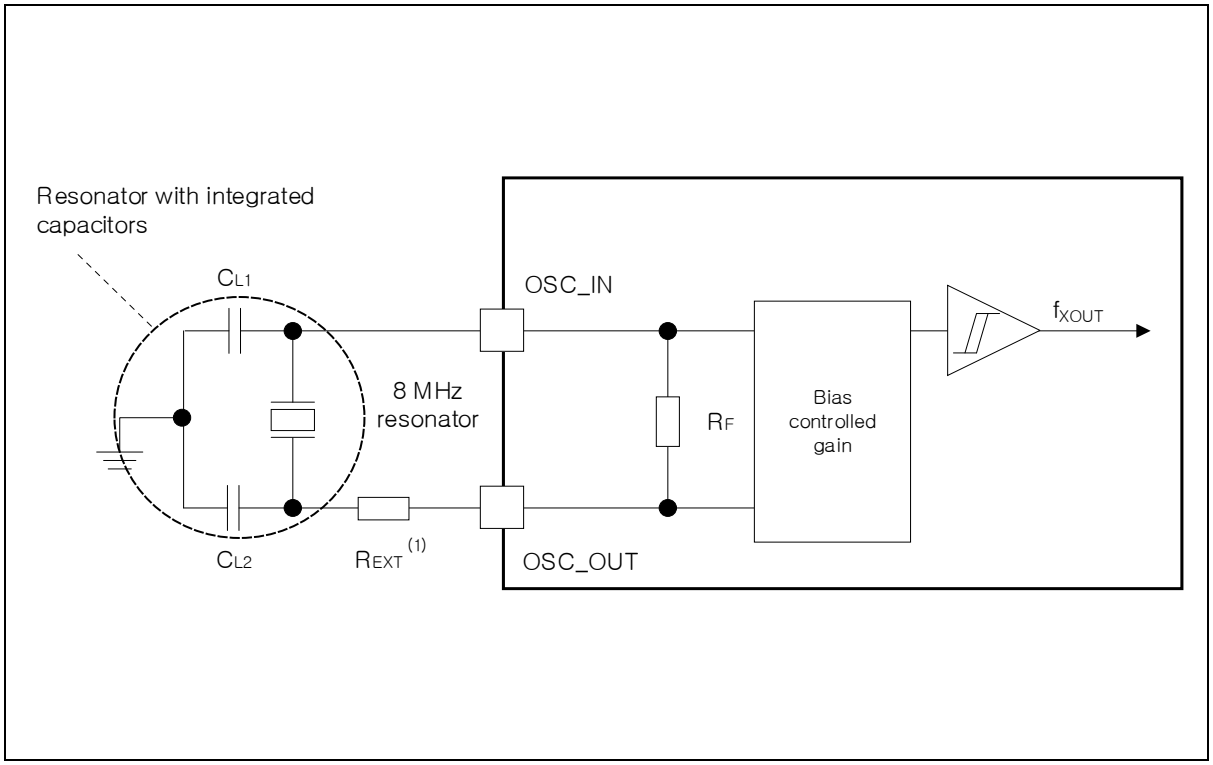


It is recommended to use high-quality external ceramic capacitors designed for high-frequency applications and selected to match the requirements of the crystal or resonator. The capacitance of the C_{L1} and C_{L2} capacitors should be between 5 pF to 20 pF. The C_{L1} and C_{L2} capacitors are usually the same size, and the crystal manufacturer specifies a load capacitance that is the series combination of both capacitors.

However, the capacitance of the Printed Circuit Board (PCB) and microcontroller pin should also be considered, which must be included in the calculation of the overall capacitance. A rough estimate of the combined pin and board capacitance is about 10 pF, which can be used to size C_{L1} and C_{L2} appropriately.

Figure 15 shows a circuit diagram of a typical application using an 8 MHz crystal.

Figure 15. Typical Application Using an 8 MHz Crystal



NOTE:

1. R_{EXT} value depends on the crystal characteristics.

3.3.6.2 External Sub-Oscillator Generated from a Crystal Resonator

A crystal/ceramic resonator oscillator at 32.768 kHz can be used to generate the external sub-oscillator (SXOSC). The information in this paragraph is based on the characterization results obtained using typical external components listed in Table 18

It is recommended to place the resonator and load capacitors as close as possible to the oscillator pins in the application to minimize output distortion and startup stabilization time.

For further information on the resonator characteristics, such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

Table 18. External Sub-Oscillator Characteristics(1) (f_{SXOSC} = 32.768 kHz)

(Temperature: −40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	-	3.0	5.0	5.5	V
I_{DD}	MXOSC current consumption	-	-	4	7	μA
f_{OUT}	Operating Frequency	-	-	32.768	-	kHz
V_{XOUT}	Output Voltage	-	-	1.5	-	V
C_L	External Load Capacitor	-	5	15	25	pF

NOTES:

1. Guaranteed by design.
2. Do not set SOSC when the GPIO output is High.

Figure 16. Crystal Oscillator

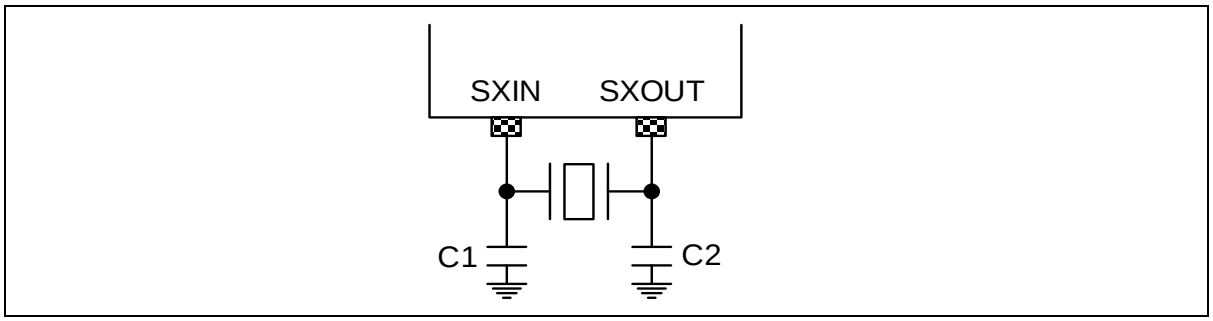


Figure 17. Clock Timing Measurement at SXIN

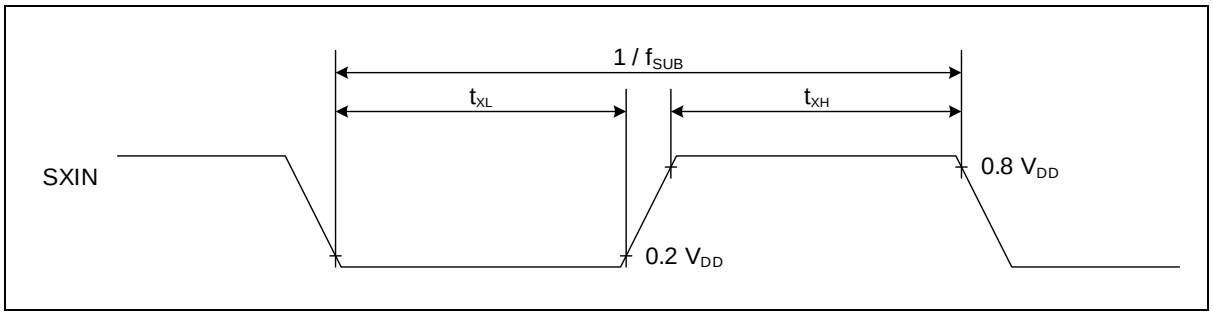
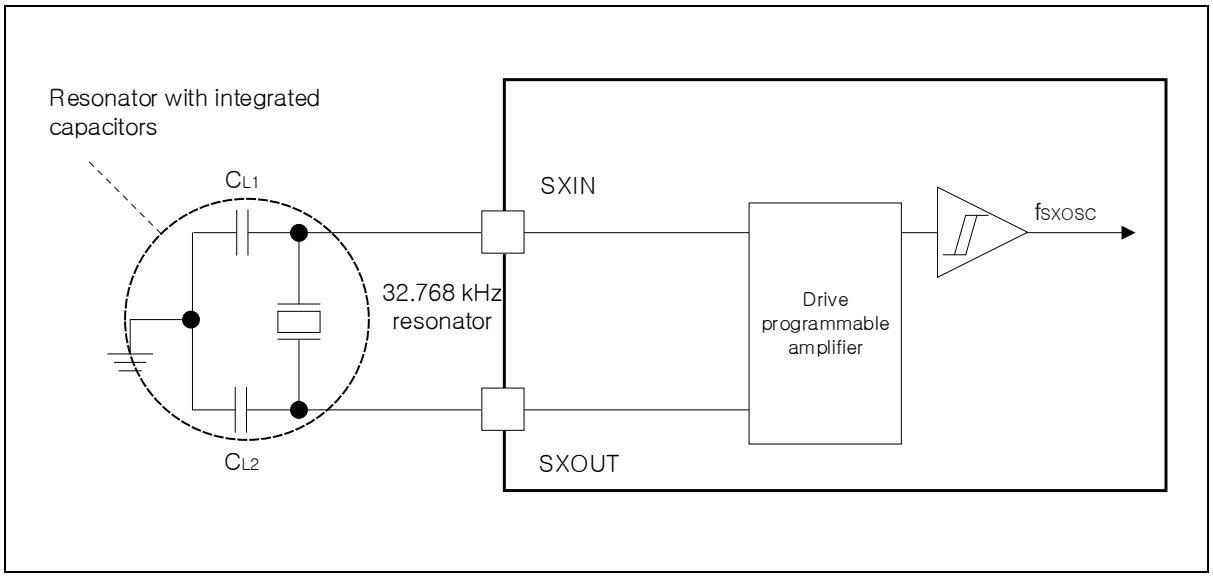


Figure 18. Typical Application with 32.768 kHz Crystal



NOTE:

1. An external resistor is not required between SXIN and SXOUT, and adding one is forbidden.

3.3.7 Internal Clock Source Characteristics

The parameters listed in Table 19 and Table 20 are obtained through tests conducted under ambient temperature and supply voltage conditions specified in Table 12.

3.3.7.1 Internal Oscillator

Table 19. Internal Oscillator Characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	-	3.0	5.0	5.5	V
I_{DD}	Operating Current	-	-	160	250	μA
f_{IOSC16}	Output Frequency	@ −20°C to 70°C (± 3.0%)	15.52	16	16.48	MHz
		@ −40°C to 85°C (± 4.0%)	15.36	16	16.64	MHz
DuCy (IOSC16)	Output Frequency Duty	-	40	-	60	%

NOTE:

1. Guaranteed by characterization results and design.

3.3.7.2 Internal Ring Oscillator

Table 20. Internal Ring Oscillator Characteristics

(Temperature: −40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	-	3.0	5.0	5.5	V
I_{DD}	Operating Current	-	-	4	8	μA
f_{ROSC}	Output Frequency	± 50%	0.5	1.0	1.5	MHz

NOTE:

1. Guaranteed by design.

3.3.8 PLL Characteristics

The parameters listed in Table 21 are obtained through tests conducted under ambient temperature and supply voltage conditions specified in Table 12.

Table 21. PLL Characteristics(1)

(Temperature: −40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	-	3.0	5.0	5.5	V
I_{DD} (PLL)	PLL Power Consumption on V_{DD}	PLL freq = 75 MHz	-	1.3	-	mA
$f_{PLL\_P\_OUT}$	Output Frequency		8	75	90	MHz
f_{DUTY}	Duty	-	40	-	60	%
t_{JITTER}	P-P Jitter	@ Lock state	-	-	500	ps
f_{VCO_OUT}	VCO Frequency (Extended Mode)		50	-	200	MHz
f_{VCOx2_OUT}	VCOx2* Frequency (Extended Mode)		100	-	250	MHz
$f_{PLLINCLK}$	Input Frequency	-	4	-	8	MHz
t_{LOCK}	PLL Lock Time	-	-	-	10	ms

NOTES:

1. Guaranteed by design.
2. * VCOx2 means that VCO Doubler mode is enabled after the VCOMODE bit of PMU_PLLCON register is set to '1'.

3.3.9 Flash Memory Characteristics

Table 22. Code Flash Memory Specification

(Temperature: −40°C to 85°C)

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature	-40	-	+85	°C
Total Code Memory Size *	-	-	768	KB
Unit Sector Size	2048	-	-	byte
Bus Width	-	-	32	bit
Endurance of Write/Erase	10,000	-	-	times
Retention Time	10	-	-	years

NOTE:

1. A33G539: 768 KB, A33G538: 512 KB

Table 23. Code Flash Memory Characteristics

(Temperature: −40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{SB}	Stand-by Current	-	-	-	10	μA
I_{CC1}	Active Read Current	f = 20 MHz	-	-	10	mA
I_{CC2}	Write Current	-	-	-	7	mA
I_{CC3}	Erase Current	-	-	-	7	mA
t_{AC}	Read Access Time	-	40	-	-	ns
t_{AAD}	Read Cycle Time	-	40	-	-	ns
t_{PROG}	Program Time	-	21	30	39	us
t_{SER}	Sector Erase Time	-	2.8	4	5.2	ms
t_{MER}	Macro Erase Time	-	5.6	8	10.4	ms

Table 24. Data Flash Memory Specification

(Temperature: −40°C to 85°C)

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature	−40	-	+85	°C
Total Code Memory Size	-	-	32	KB
Unit Sector Size	2048	-	-	byte
Bus Width	-	-	8	bit
Endurance of Write/Erase	100,000	-	-	times
Retention Time	10	-	-	years

Table 25. Data Flash Memory Characteristics

(Temperature: −40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{SB}	Stand-by Current	-	-	-	10	μA
I_{CC1}	Active Read Current	f = 20 MHz	-	-	3	mA
I_{CC2}	Write Current	-	-	-	7	mA
I_{CC3}	Erase Current	-	-	-	7	mA
t_{AC}	Read Access Time	-	40	-	-	ns
t_{AAD}	Read Cycle Time	-	40	-	-	ns
t_{PROG}	Program Time	-	21	30	39	us
t_{SER}	Sector Erase Time	-	2.8	4	5.2	ms
t_{MER}	Macro Erase Time	-	5.6	8	10.4	ms

3.3.10 I/O Port Characteristics

Table 26. DC Electrical Characteristics(1)

(VDD : 5 V, GND = 0 V, Temperature: 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	Port A, B, C, E, F	−0.3	-	1	V
		Port D	−0.3	-	1	V
V_{IH}	Input High Voltage	Port A, B, C, E, F	4	-	5.3	V
		Port D	2.7	-	5.3	V
V_H	Hysteresis Voltage (1)	-	-	1.0	-	V
V_{OL}	Output Low Voltage	IOL = 3 mA (Port A, B, C, E, F)	0	-	1	V
		IOL = 18 mA (Port D)	0	-	1	V
V_{OH}	Output High Voltage	IOH = −1.2 mA (Port A, B, C, E, F)	4	-	5	V
		IOH = -8.0 mA (Port D)	4	-	5	V
I_{OL}	Output Low Current	VOL = 1 V (Port A, B, C, E, F)	3	-	-	mA
		VOL = 1 V (Port D)	18	-	-	mA
I_{OH}	Output High Current	VOH = 4 V (Port A, B, C, E, F)	-	-	−1.2	mA
		VOH = 4 V (Port D)	-	-	-8	mA
I_{IL}	Input Low Leakage Current	-	−4	-	-	
I_{IH}	Input High Leakage Current	-	-	-	4	µA
R_{PU}	Pull-up Register	-	10	-	60	kΩ
R_{PD}	Pull-down Register	-	40	-	70	kΩ

NOTE:

1. Hysteresis voltage between Schmitt trigger switching levels; based on characterization, NOT tested in production.

Table 27. DC Electrical Characteristics[2]

(VDD = 3.3 V, GND = 0 V, Temperature: 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	Port A, B, C, E, F	–0.3	-	0.6	V
		Port D	–0.3	-	0.6	V
V_{IH}	Input High Voltage	Port A, B, C, E, F	2.7	-	3.6	V
		Port D	2.2	-	3.6	V
V_H	Hysteresis Voltage [1]	-	-	1.0	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA (Port A, B, C, E, F)	0	-	0.66	V
		I_{OL} = 10 mA (Port D)	0	-	0.66	V
V_{OH}	Output High Voltage	I_{OH} = -0.8 mA (Port A, B, C, E, F)	2.64	-	3.3	V
		I_{OH} = -6.0 mA (Port D)	2.64	-	3.3	V
I_{OL}	Output Low Current	V_{OL} = 0.6 V (Port A, B, C, E, F)	2	-	-	mA
		V_{OL} = 0.6 V (Port D)	10	-	-	mA
I_{OH}	Output High Current	V_{OH} = 2.7 V (Port A, B, C, E, F)	-	-	–0.8	mA
		V_{OH} = 2.7 V (Port D)	-	-	–6.0	mA
I_{IL}	Input Low Leakage Current	-	–4	-	-	
I_{IH}	Input High Leakage Current	-	-	-	4	µA
R_{PU}	Pull-up Register	-	10	-	100	kΩ
R_{PD}	Pull-down Register	-	40	-	70	kΩ

NOTE:

1. Hysteresis voltage between Schmitt trigger switching levels; based on characterization, NOT tested in production.

3.3.11 Analog-to-Digital Converter Characteristics

Table 28. ADC Electrical Characteristics

(Temperature: −20°C to 85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	unit
AV_{DD}	Operating voltage	-	3.0	5	5.5	V
-	Resolution	-	-	-	12	bit
I_{DDA}	Operating Current	AV_{DD} = 5.0 V	-	1	2	mA
V_{AN}	Analog Input Range	-	VSS	-	AV_{DD}	V
f_{CON}	Conversion Rate	5.0 V < AV_{DD} < 5.5 V	-	60 × MCLK	66.6	ksps
f_{MCLK}	Operating Frequency	-	-	-	4	MHz
INL	DC Accuracy	AV_{DD} = 5.0 V, T_A = 25°C	-	±8	-	LSB
DNL			-	±2	-	LSB
ZOE	Zero Offset Error[1)]		-	2	-	LSB
FSE	Full-Scale Error[2)]		-	2	-	LSB

NOTES:

1. Zero Offset Error is the difference between the zero-input voltage (VSS) converted to a digital value and 0x000.
2. Full-Scale Error is the difference between the top input voltage (VDD) converted to a digital value and 0xFFF.

3.3.11.1 General PCB Design Guidelines

The power supplier must be separated, conforming to the scheme shown in Figure 10. The de-coupling capacitors across the V_{DD}/AV_{DD} are ceramic (good quality) capacitors and must be as close as possible to the chip.

3.3.12 Communication Interfaces Characteristics

3.3.12.1 I2C Interface Characteristics

The I2C interface conforms to the timing requirements specified in the I2C-bus specification, in addition to the user timing requirements listed below:

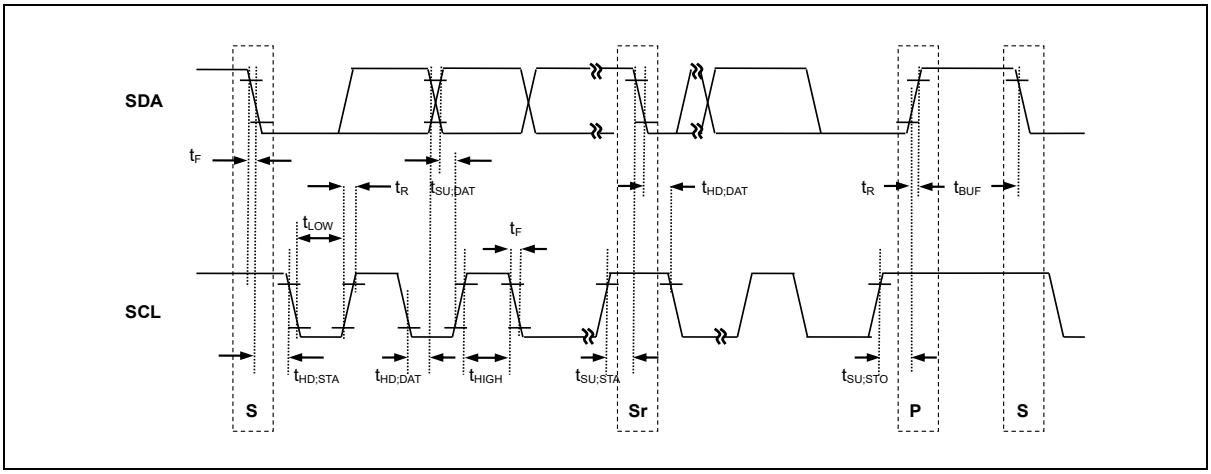
- Standard mode (Sm): up to 100 kbps bit rate
- Fast mode (Fm): up to 400 kbps bit rate

The I2C timing requirements are guaranteed by design when the I2C peripheral is configured correctly and the I2C clock frequency is equal to or greater than the minimum value listed in the table below.

Table 29. I2C Characteristics

Symbol	Parameter	Standard		Fast		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	0	100	0	400	kHz
$t_{HD;\ STA}$	Hold Time after (Repeated) START Condition (After this period, the first clock pulse is generated.)	4.0	-	0.6	-	µs
t_{LOW}	LOW Period of the SCL Clock	4.7	-	1.3	-	µs
t_{HIGH}	HIGH Period of the SCL Clock	4.0	-	0.6	-	µs
$t_{SU;STA}$	Setup Time for a Repeated START Condition	4.7	-	0.6	-	µs
$t_{HD;DAT}$	Data Hold Time	0	3.45	0	0.9	µs
$t_{SU;DAT}$	Data Setup Time	100	-	100	-	ns
t_F	Clock/Data Fall Time	0	300	0	300	ns
t_R	Clock/Data Rise Time	0	1000	0	300	ns
$t_{SU;STO}$	Setup Time for a STOP Condition	4.0	-	0.6	-	µs
t_{BUF}	Bus Free Time between STOP and START Conditions	4.7	-	1.3	-	µs

Figure 19. I2C Interface Bus Timing

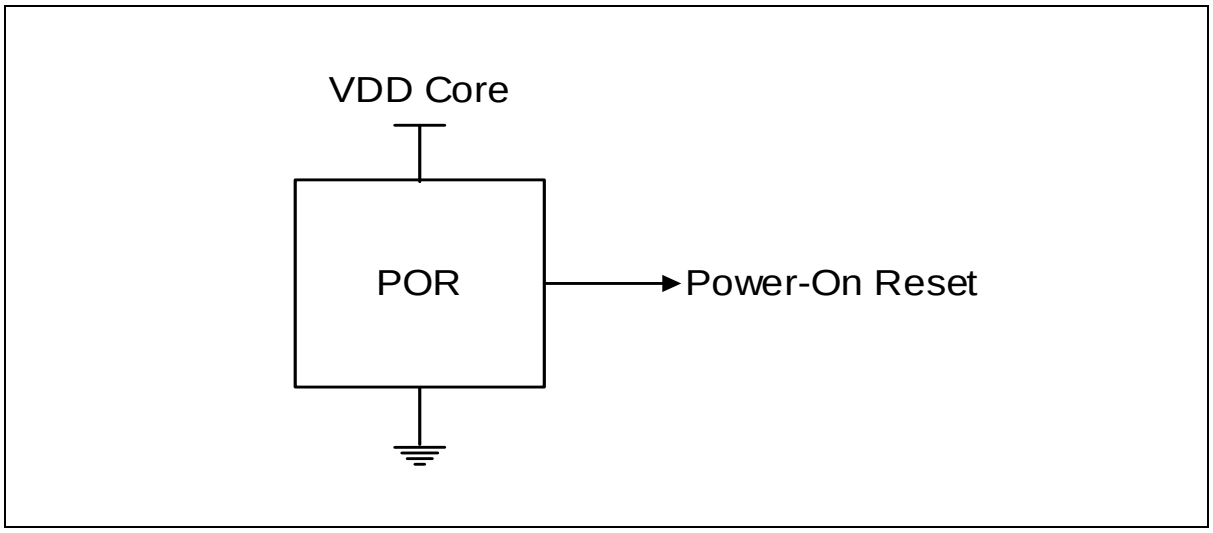


3.4 Characteristics of Analog Block

3.4.1 Power-On Reset (POR)

The A33G53x has a built-in Power-On Reset (POR) that monitors the internal voltage of the VDD Core and generates a reset signal for the microcontroller's cold start.

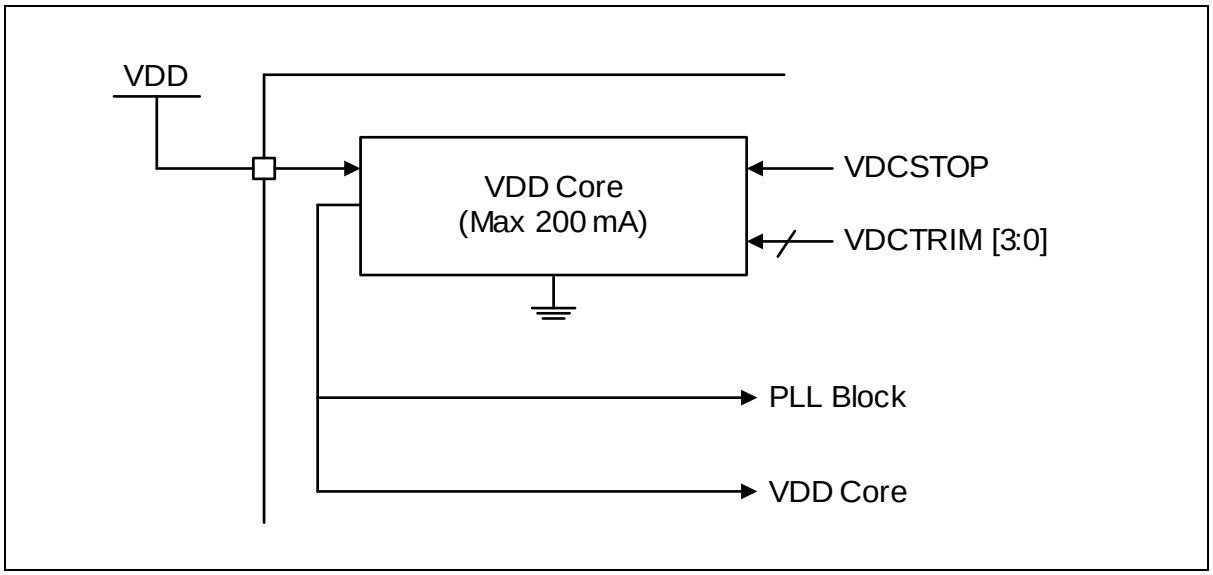
Figure 20. POR Block Diagram



3.4.2 Voltage Down Converter (VDC)

Built-in VDC generates the power regulated from external power for internal logic and analog block.

Figure 21. VDC Block Diagram

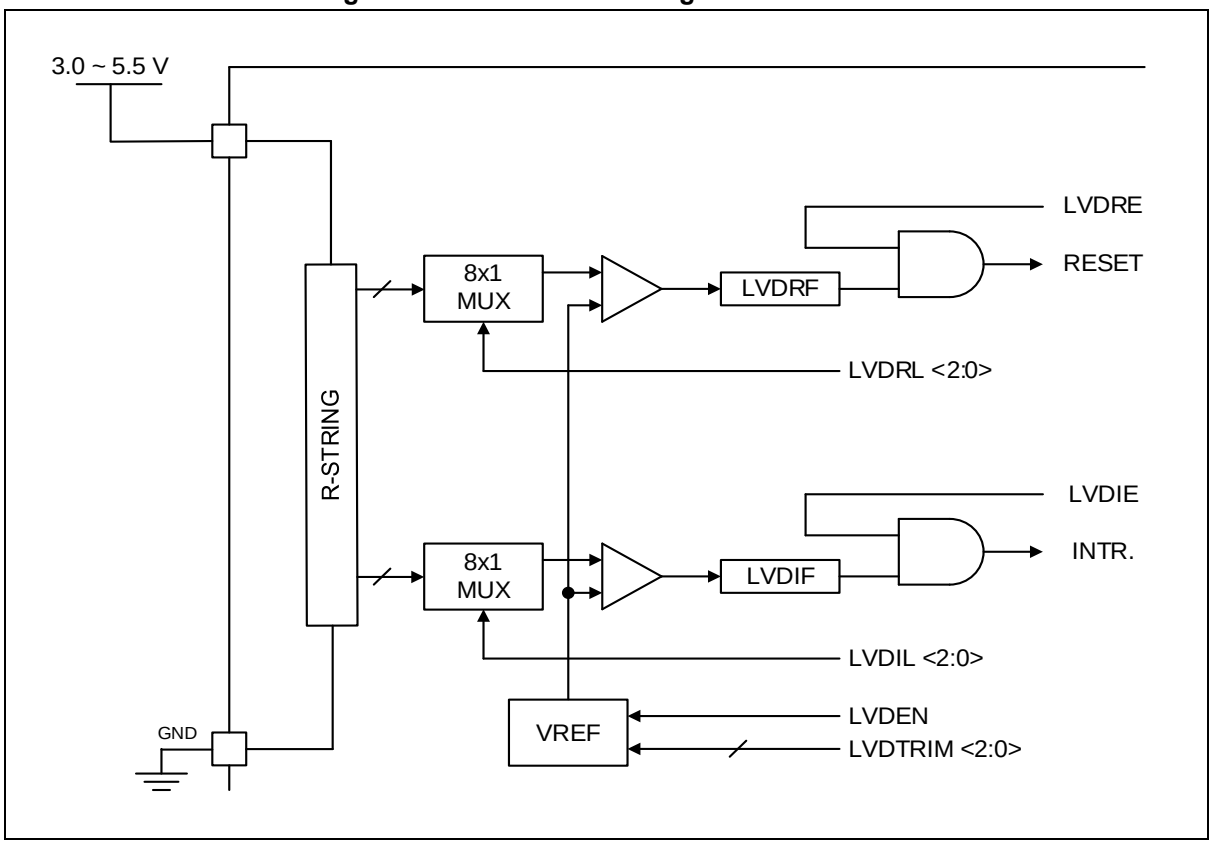


3.4.3 Low-Voltage Detector (LVD)

The A33G53x has two built-in LVDs. Each LVD generates an interrupt or reset depending on settings. LVDs are monitoring external 5 V power.

Figure 22 shows a configuration of LVDs.

Figure 22. The Internal Configuration of LVDs



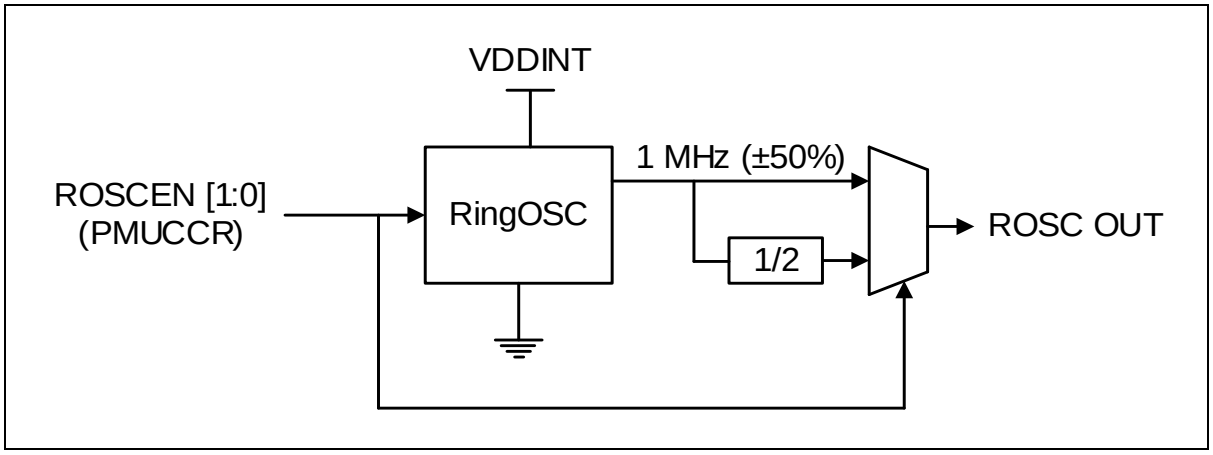
3.4.4 Internal Ring Oscillator (RingOSC/ROSC)

The A33G53x has a simple ring oscillator to monitor the system and supply clocks to other peripherals. This ring oscillator generates a frequency of 1 MHz and is used for POR, WDT, clock monitoring, etc.

This ring oscillator is used as the system operating clock for smaller power consumption in SLEEP mode. However, a ring oscillator is not desirable to be used where precise frequency is needed due to the characteristic that the ring oscillator is easily affected by the power and temperature.

Figure 23 shows a block diagram of the ring oscillator.

Figure 23. Internal Configuration of RingOSC

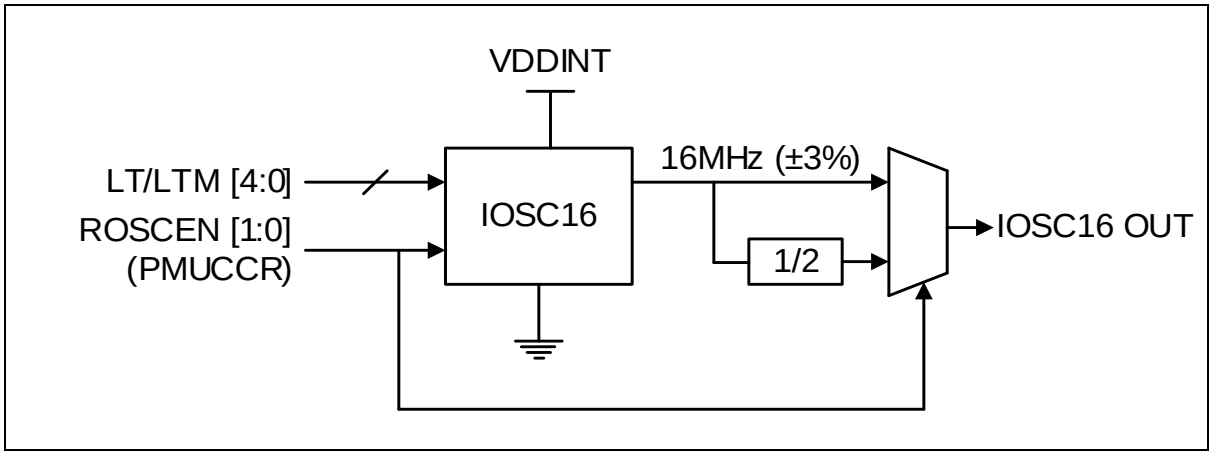


3.4.5 Internal 16MHz Oscillator (IOSC16)

The A33G53x has a built-in 16 MHz oscillator to operate without any external clock.

Figure 24 shows a configuration of the internal 16 MHz oscillator.

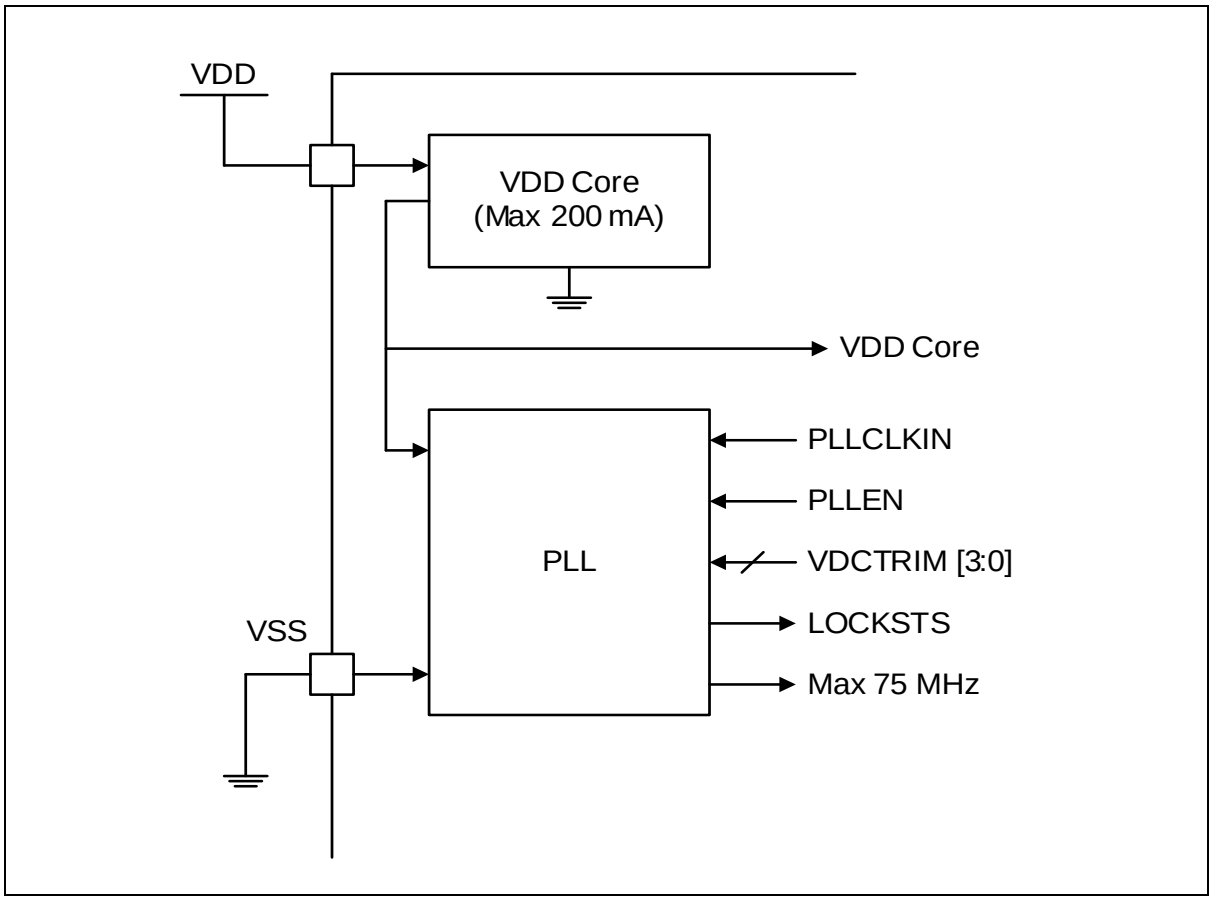
Figure 24. Internal Configuration of IOSC16



3.4.6 Phase-Locked-Loop (PLL)

The built-in PLL can multiply internal or external clocks up to 75 MHz. The PLL frequency synthesizer can be used to set the PLL output frequency up to 75 MHz in 1 MHz increments. The VDD Core power required for the PLL is supplied from inside the microcontroller.

Figure 25. Configuration of PLL

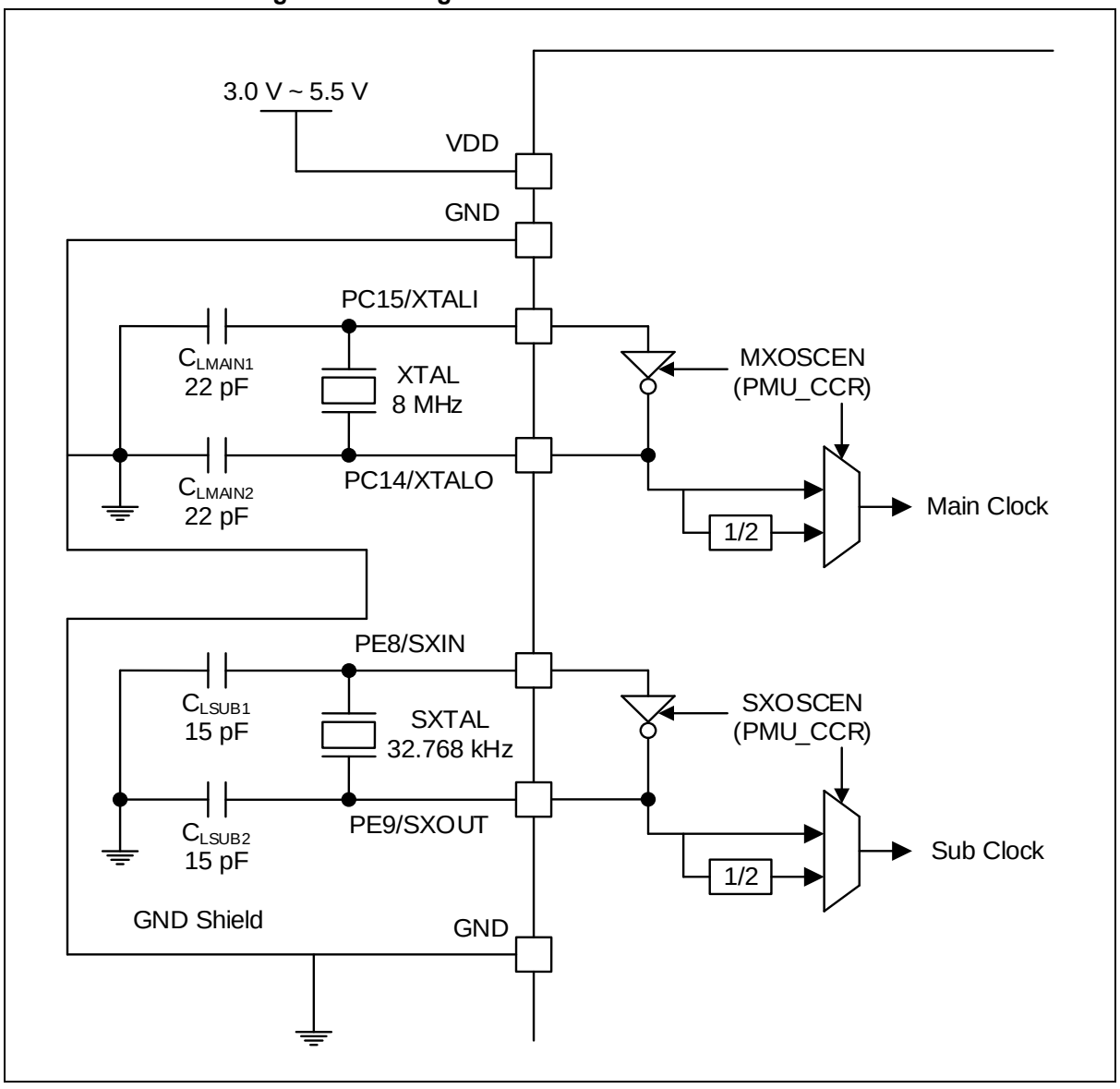


3.4.7 External Main and Sub Oscillator

The A33G53x has a Main Oscillator that produces 4 to 10 MHz frequencies and a Sub-Oscillator with 32.768kHz. They are crystal oscillators designed for more immunity performance to electrical noises.

Figure 26 shows a configuration of the Main and Sub-Oscillators.

Figure 26. Configuration of Main and Sub-Oscillators



3.4.8 Power Configuration

Figures in this section show the power configuration of the A33G53x by package.

Figure 27. Power Configuration of A33G53x (100-MQFP)

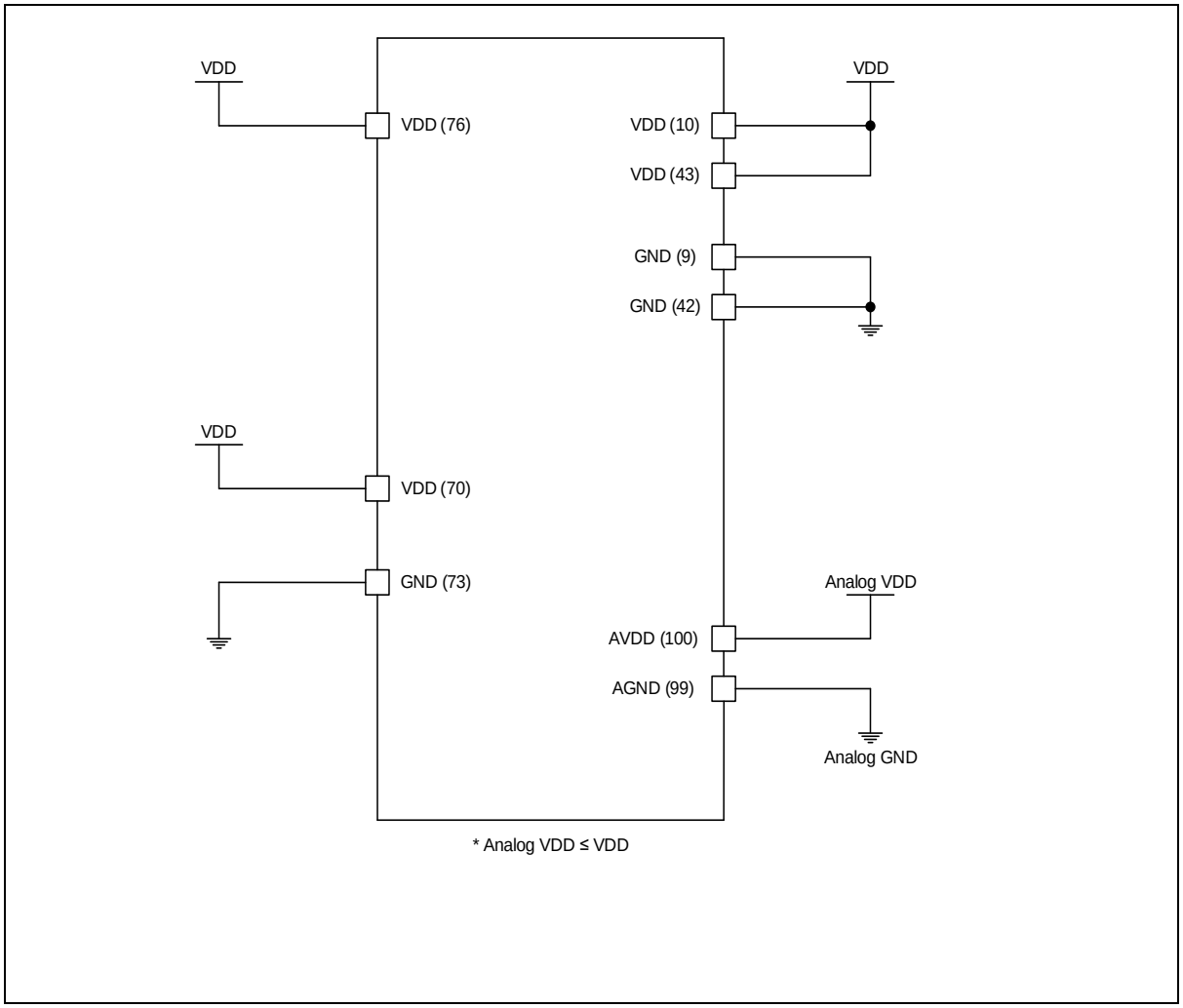


Figure 28. Power Configuration of A33G53x (100-LQFP14)

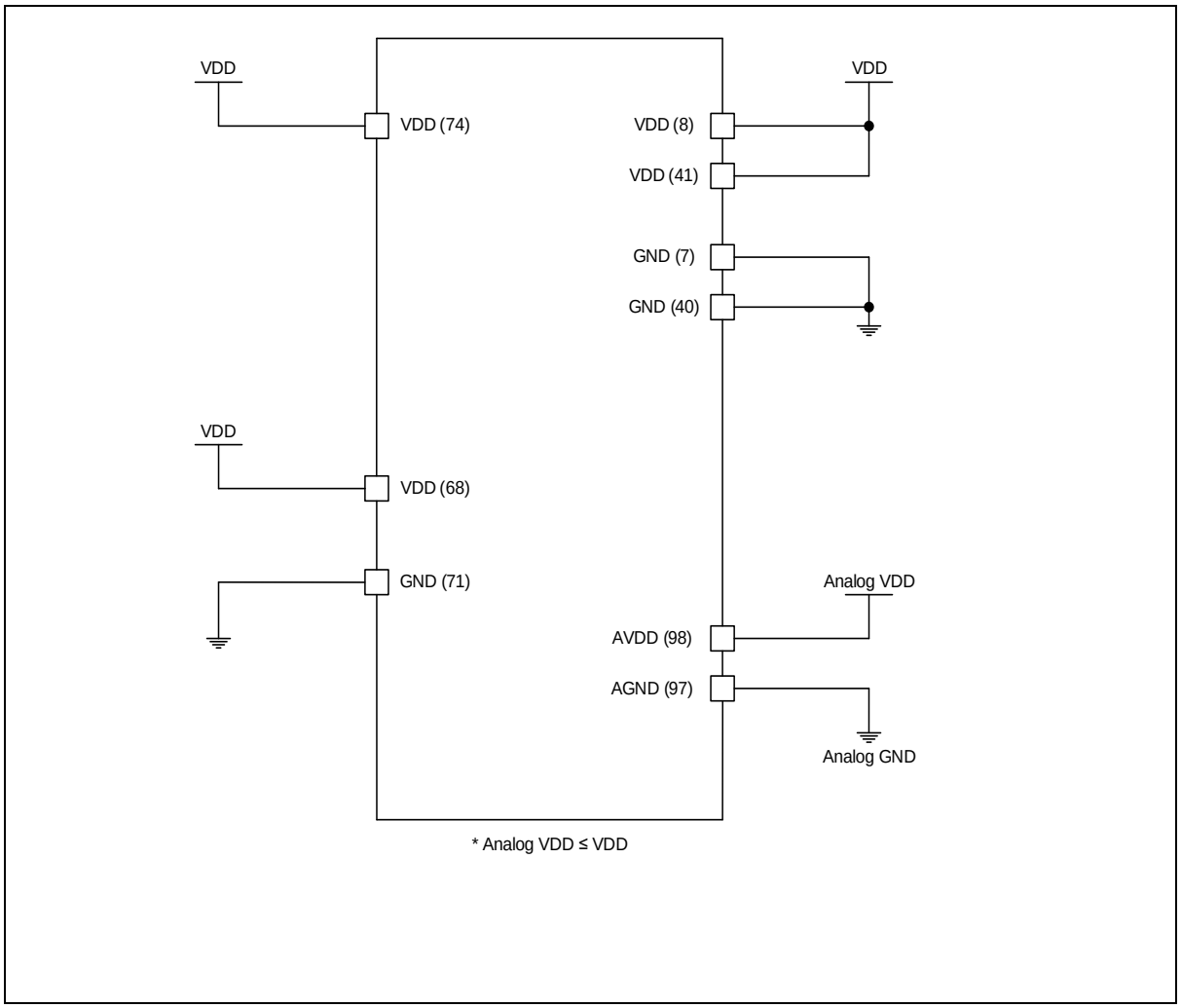


Figure 29. Power Configuration of A33G53x (80-LQFP14)

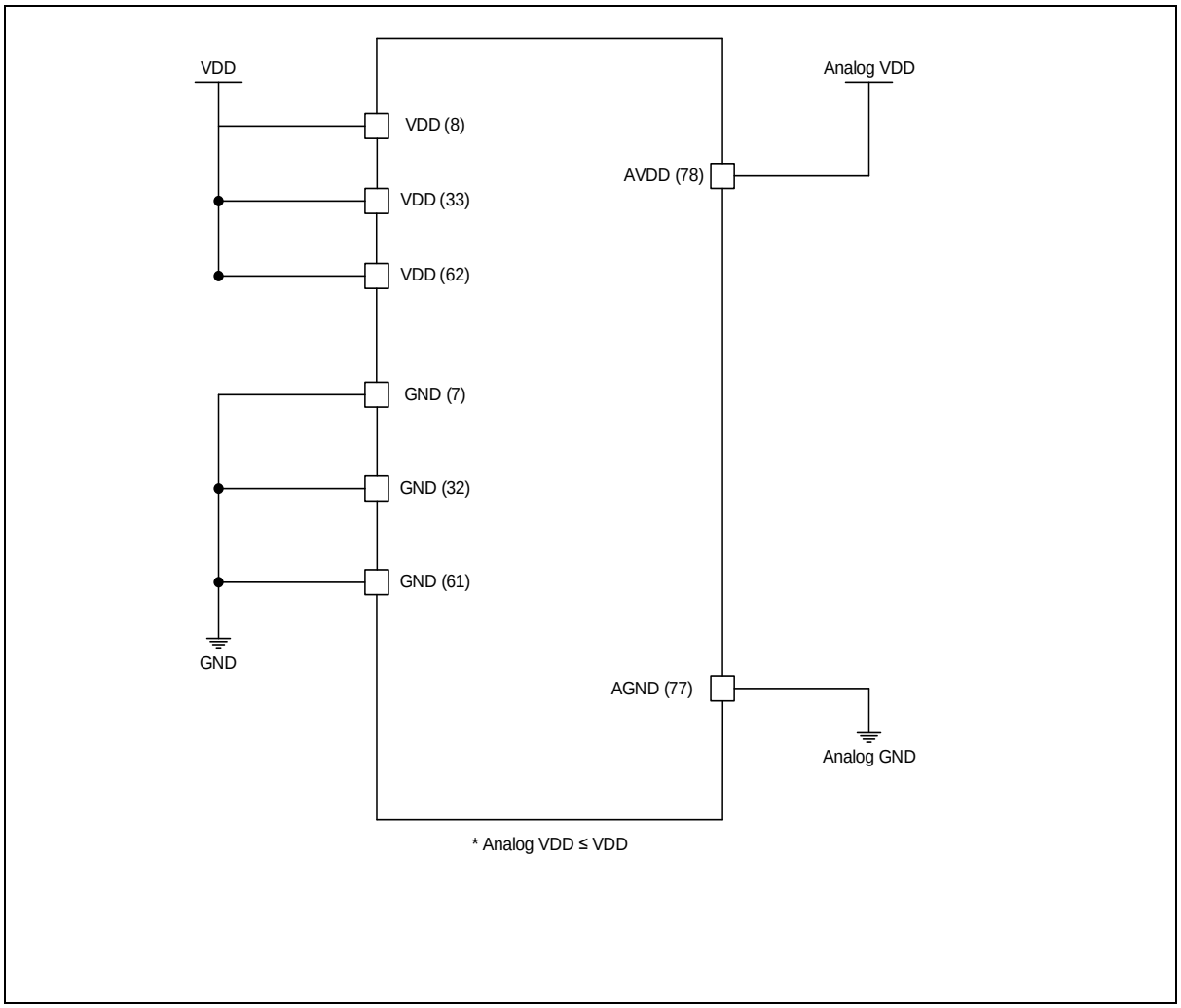
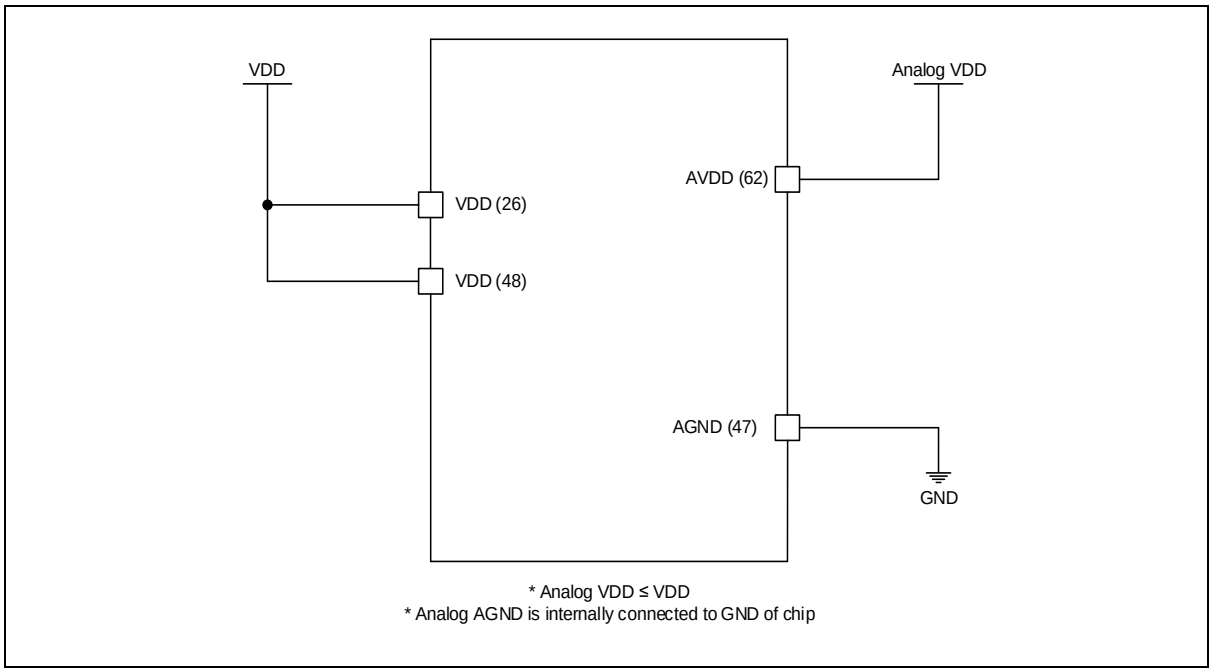


Figure 30. Power Configuration of A33G53x (64-LQFP12)

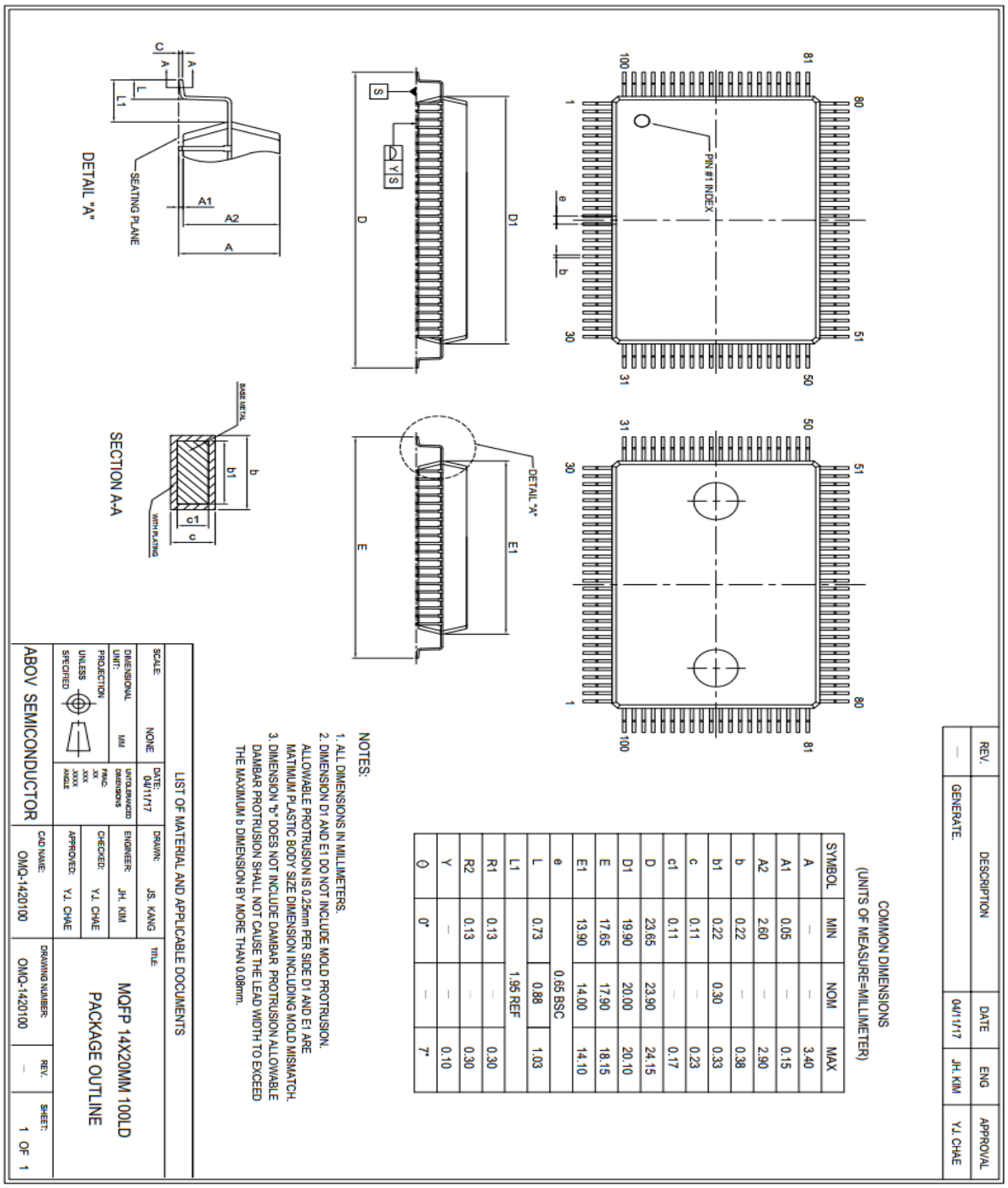


4. Package Information

4.1 100-MQFP Package Information

100-MQFP is a 100-pin, 14 x 20 mm metric quad flat package.

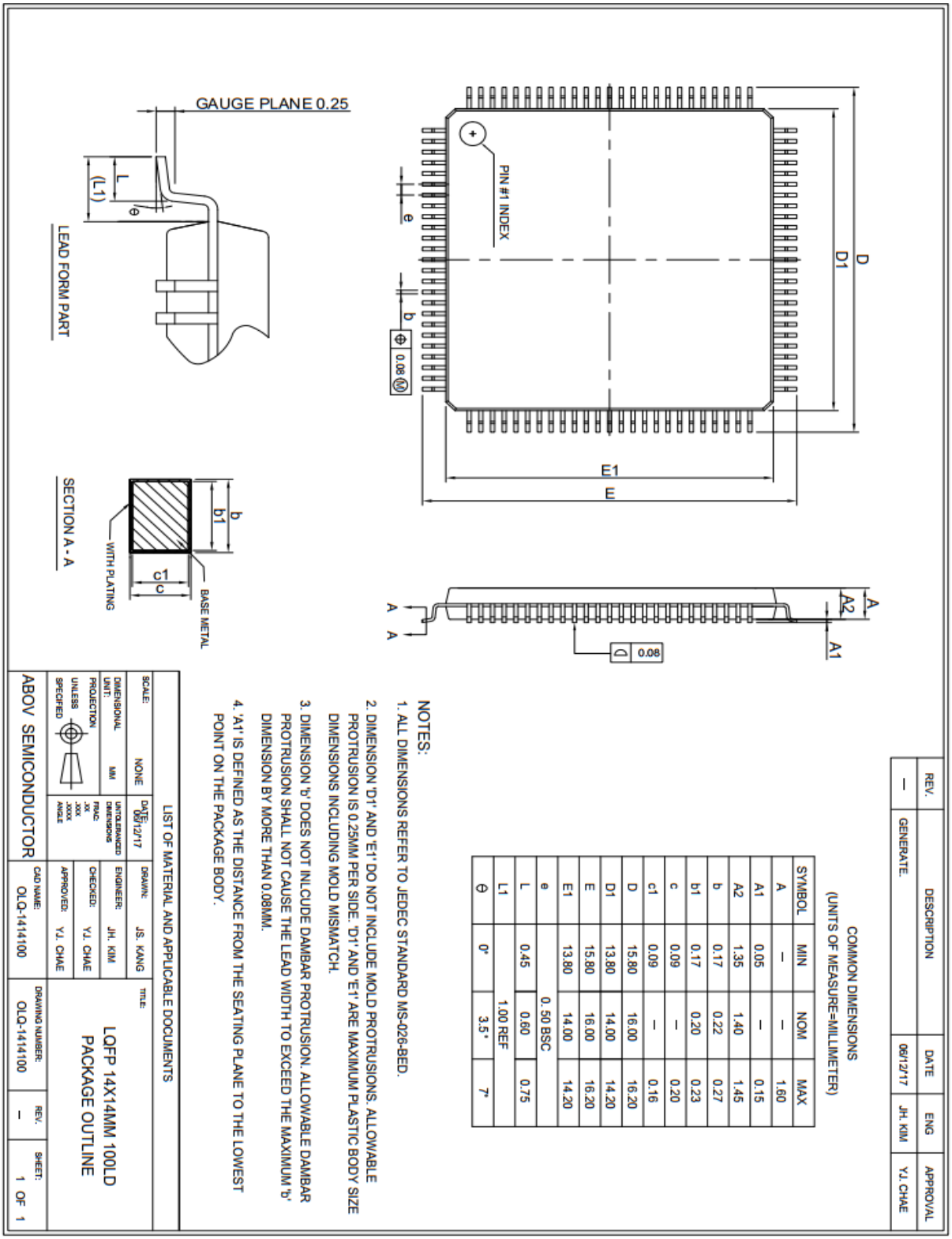
Figure 31. Package Dimension (100-MQFP)



4.2 100-LQFP Package Information

100-LQFP is a 100-pin, 14 x 14 mm quad flat package.

Figure 32. Package Dimension (100-LQFP)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	–	0.20
c1	0.09	–	0.16
D	15.80	16.00	16.20
D1	13.80	14.00	14.20
E	15.80	16.00	16.20
E1	13.80	14.00	14.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BED.
2. DIMENSION 'D1' AND 'E1' DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INLCUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	06/12/17	JH. KIM	YJ. CHAE

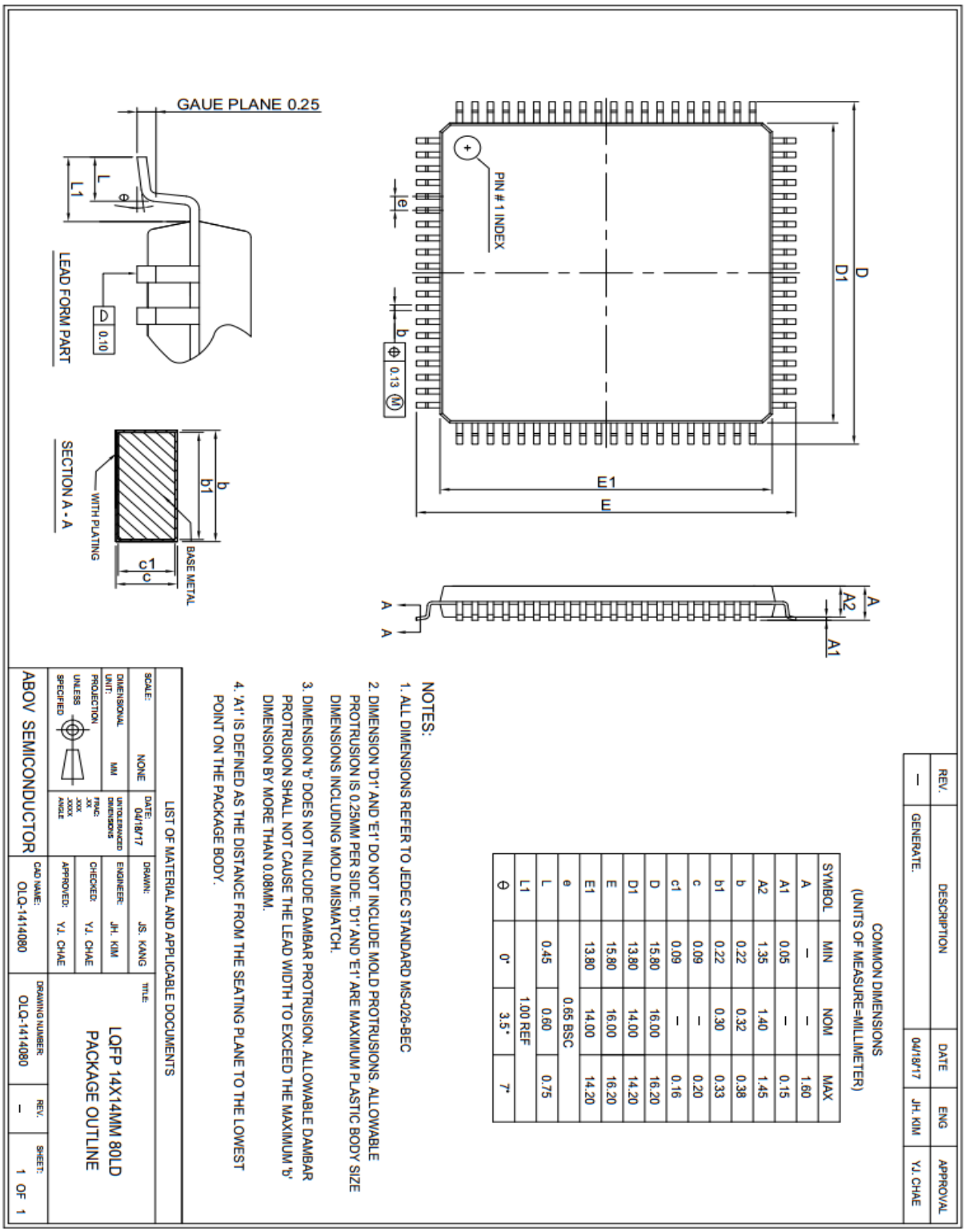
LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 06/12/17	DRAWN: JS. KANG	TITLE: LQFP 14X14MM 100LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM	
PROJECTION UNLESS SPECIFIED	FRAC: XX .XXX ANGLE:	CHECKED: YJ. CHAE	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-1414100	APPROVED: YJ. CHAE	DRAWING NUMBER: OLQ-1414100
			REV: —
			SHEET: 1 OF 1

4.3 80-LQFP Package Information

80-LQFP is an 80-pin, 14 x 14 mm quad flat package.

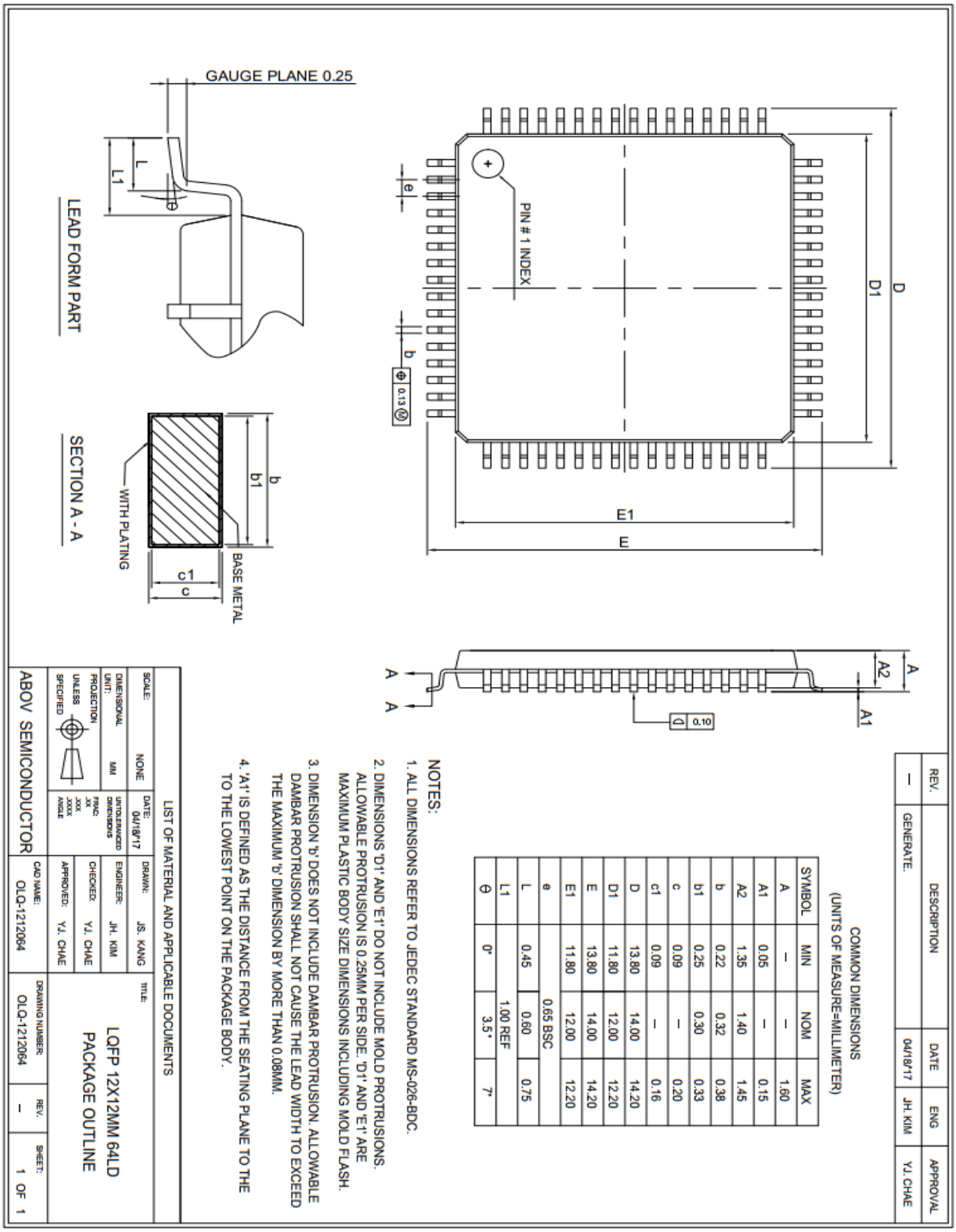
Figure 33. Package Dimension (80-LQFP)



4.4 64-LQFP Package Information

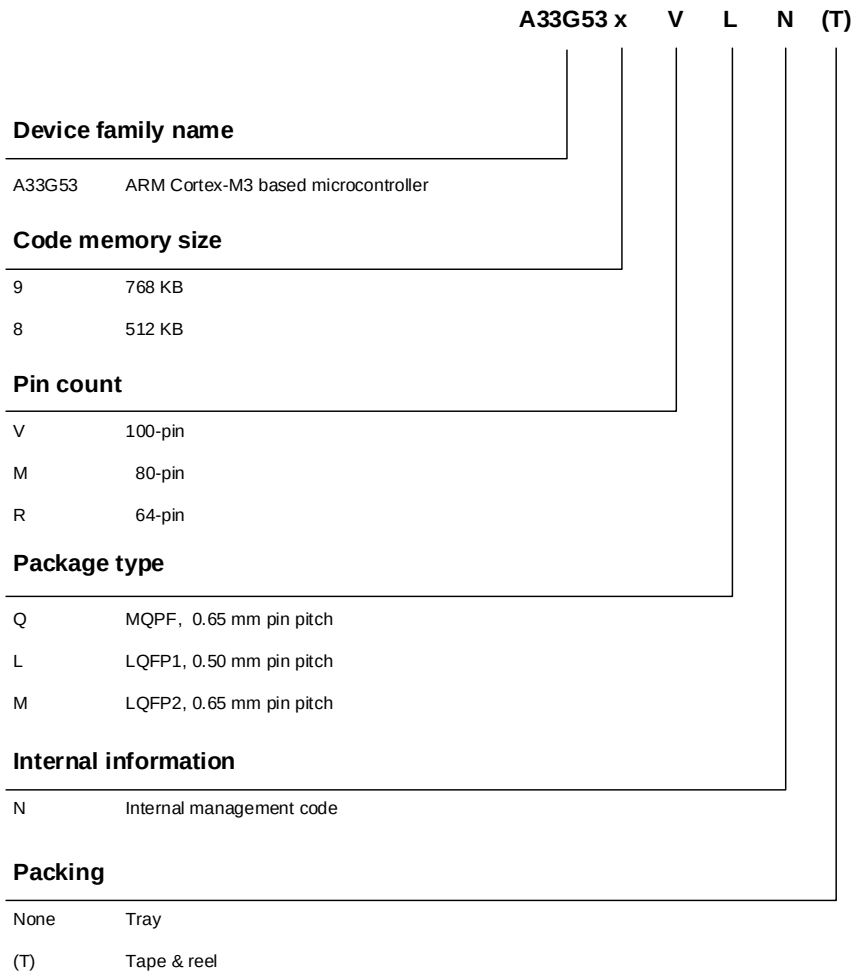
64-LQFP is a 64-pin, 12 x 12 mm quad flat package.

Figure 34. Package Dimension (64-LQFP)



Ordering Information

Figure 35. Device Nomenclature - Part Number Decoder



NOTE:

1. For a list of available options (memory, package, and so on) or further information on any aspect of this device, contact the nearest ABOV sales office.

Glossary

This section gives a brief definition of acronyms and abbreviations used in this document:

- Word: Data of 32-bit length
- AHB: Advanced High-performance Bus
- APB: Advanced Peripheral Bus
- Byte: Data of 8-bit length
- CRC: Cyclic Redundancy Check
- ECC: Error Correct Code
- FIFO: First-In/First-Out
- FRT: Free-Run Timer
- I2C: Inter-Integrated Circuit
- IOSC: Internal Oscillator
- LSB: Least Significant Bit
- LQFP: Low-profile Quad Flat Package
- LVDR: Low-Voltage Detector Reset
- LVDI: Low-Voltage Detector Interrupt
- MQPF: Metric Quad Flat Package
- MSB: Most Significant Bit
- MXOSC: External Main Oscillator (MainOSC)
- PGM: Programming
- PLL: Phase-Locked-Loop
- PMC: Port Map Control
- PMU: Power Management Unit
- POR: Power-On Reset
- PWM: Pulse-Width Modulation
- SPI: Serial Peripheral Interface
- UART: Universal Asynchronous Receiver Transmitter
- RingOSC: Internal Ring Oscillator
- SXOSC: External Sub-Oscillator (SubOSC)
- WDT: WatchDog Timer

Revision History

Revision	Date	Notes
1.00	Nov. 8, 2023	Initial release
1.01	Feb. 22, 2024	Modified section 3.1.1, section 3.1.2 and section 3.3.2.

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