December 3, 2015 Ver 1.1

4-BIT SINGLE CHIP MICROCOMPUTERS

ADAM46P20XX

USER`S MANUAL

- ADAM46P2016
- ADAM46P2016T
- ADAM46P2014
- ADAM46P2014D
- ADAM46P2010
- ADAM46P2008
- ADAM46P2008T
- ADAM46P2008D

ABOV SEMICONDUCTOR

0. Revision History

Version	Date	Description
VER 0.0	2010.11.17	1'st Release.
VER 0.1	2010.12.03	-. Change the VDI Level : 3.6V → 3.3V, 2.4V → 2.2V -. Change the LVD Level : 2.0V → 1.8V, 2.4V → 2.2V -. Change the Operating Voltage : 2.0V~5.5V @4MHz -. Correct the some Errata.
VER 0.2	2010.12.04	-. Add the Package types (14-DIP, 10-MSOP, 8-DIP)
VER 0.3	2011.01.27	-. Remove a instruction ("LPG") -. Change the "S" bit of SFR in reset state.
VER 0.4	2011.04.05	-. Add the peripheral register ("ABR3").
VER 0.5	2011.07.21	-. Add the External RESETB Circuit.
VER 1.0	2012.07.15	-. Change the Operating Voltage Spec (page-2, 15) Ver 0.5 : ● 2.0 ~ 5.5 V @ 0.5MHz ~ 4MHz ● 2.2 ~ 5.5 V @ 4MHz ~ 8MHz ● 2.7 ~ 5.5 V @ 8MHz ~ 16MHz Ver 1.0 : ● 2.0 ~ 5.5 V @ 0.5MHz ~ 4MHz ● 2.7 ~ 5.5 V @ 8MHz ● 4.5 ~ 5.5 V @ 16MHz
VER 1.1	2015.12.3	Add the chapter '1.7.5 POR Electrical Characteristics'. (19 page) Add the electrical specification of LVD & Temperature characteristics. (16, 18 page)

1. OVERVIEW

The ADAM46P20XX is the High Speed and Low Voltage operating 4-bit single chip microcomputer. This chip contains ADAM46 CPU, EPROM, RAM, Timer/Count, Interrupt, Watch Dog Timer, Input/Output Ports and Oscillation Circuit.

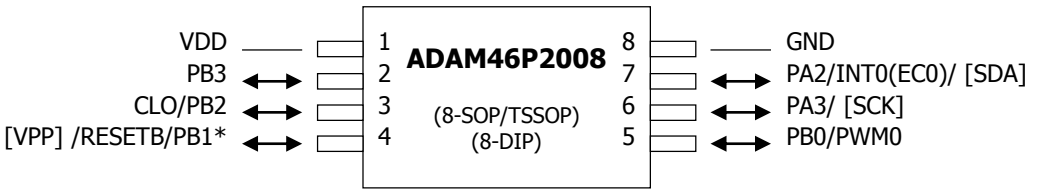
1.1. Features

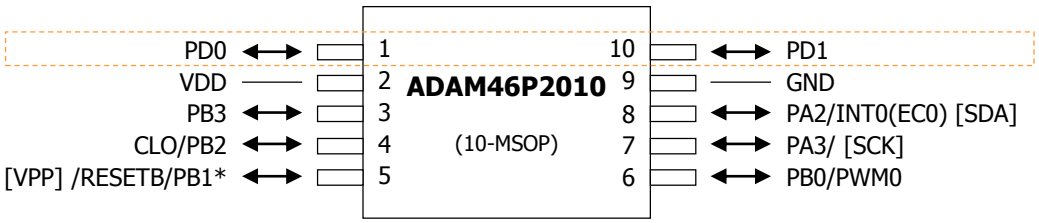
- ◆ Instruction Execution Time
  - ● 500ns @ fosc=8MHz
- ◆ Program Memory Area (OTP)
  - ● 2K Bytes (1,024 x 16bit)
- ◆ Data memory (RAM)
  - ● 64 nibble (64 x 4bit)
- ◆ 16-Bit Table read Instruction.
- ◆ Timer (Timer/Counter/Capture/PWM)
  - ● 8Bit x 1ch
- ◆ Watch-Dog Timer (with RCWDT=64kHz)
  - ● 19Bit x 1ch
- ◆ Oscillator Type
  - ● Calibrated Internal RCOSC : typ. 16/8/4/2/1/0.5MHz selectable
- ◆ Power On Reset
- ◆ Power Saving Operation Modes
  - ● STOP
  - ● RCWDT
- ◆ Interrupt Sources
  - ● External : 1ch (INT0)
  - ● Internal : 3ch (T0, WDT, VDI)
- ◆ Reset
  - ● Built-in Watch-dog timer
  - ● Built-in Power-on Reset (POR)
  - ● Built-in Low Voltage Detection & Reset (LVD)
  - ● Built-in Voltage Detection Indicator & Reset (VDI)
  - ● External RESETB
- ◆ Low Voltage Detection Reset Circuit
- ◆ 2-level Voltage Detection Indicator (3.3V/2.2V)
- ◆ Operating Voltage Range
  - ● 2.0 ~ 5.5 V @ 0.5MHz ~ 4MHz
  - ● 2.7 ~ 5.5 V @ 8MHz
  - ● 4.5 ~ 5.5 V @ 16MHz
- ◆ Operating Temperature Range
  - ● -40 ~ 85 ℃

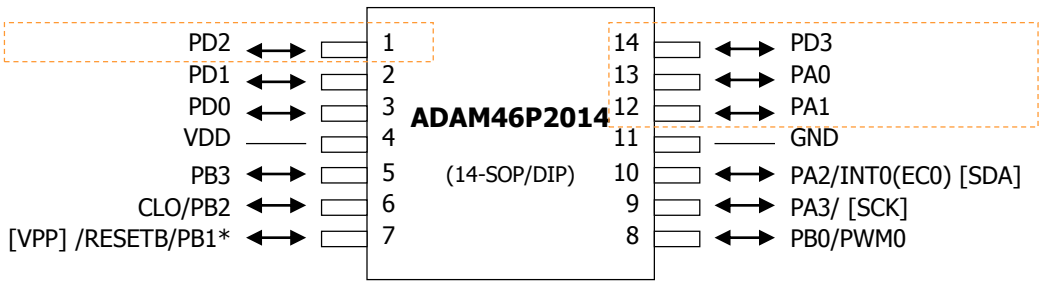
☑ ADAM46P20XX Device Summary

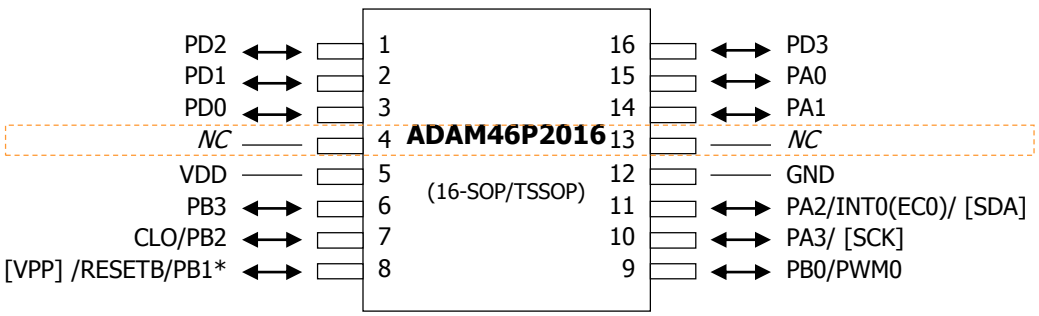
Series	ADAM46P2016	ADAM46P2014	ADAM46P2010	ADAM46P2008
Program memory	1,024 x 16	1,024 x 16	1,024 x 16	1,024 x 16
Data memory	64 x 4	64 x 4	64 x 4	64 x 4
I/O ports	12	12	8	6
Package	16-SOP/TSSOP	14-SOP/DIP	10-MSOP	8-SOP/TSSOP/DIP

1.2. Pin Assignments



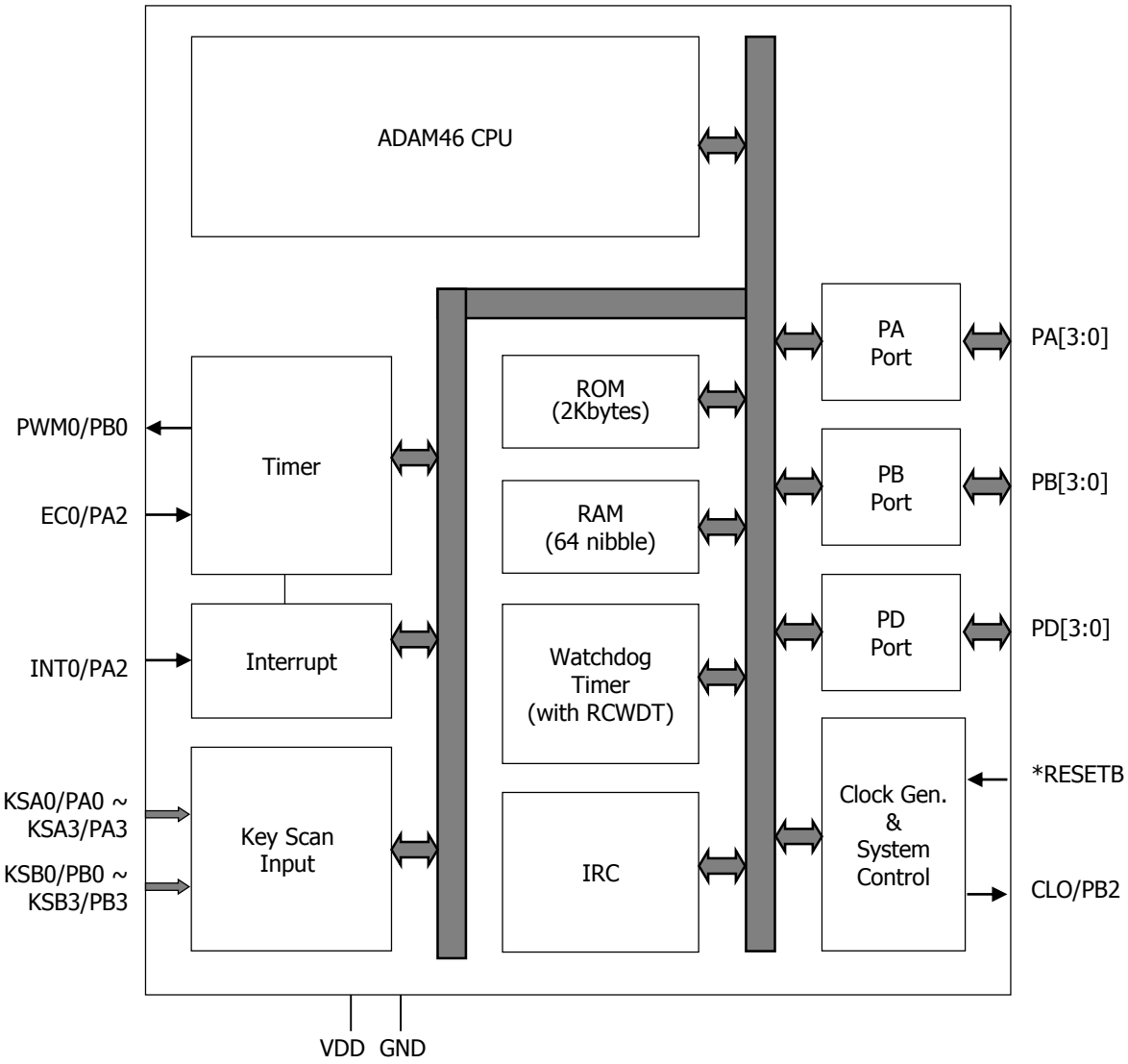






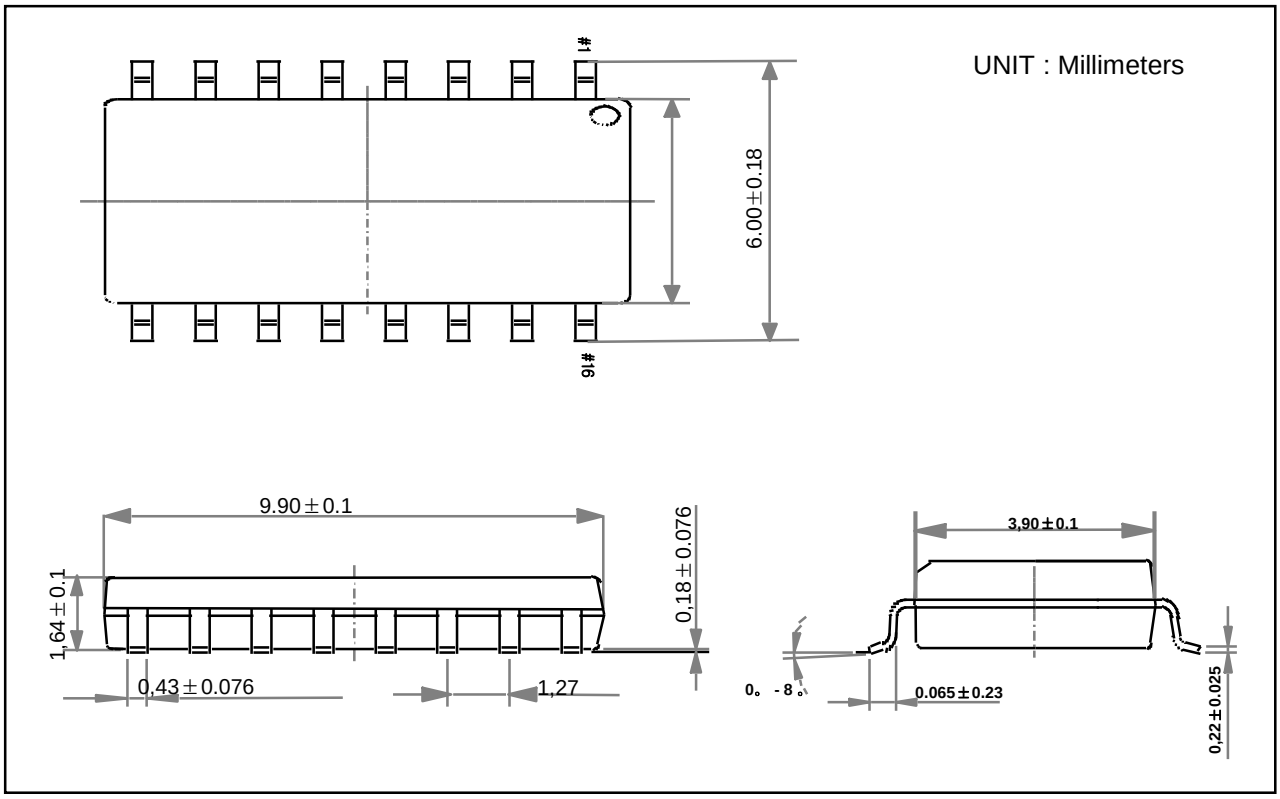
※ RESETB is selected by setting the OTP Configuration Bit.

1.3. Block Diagram

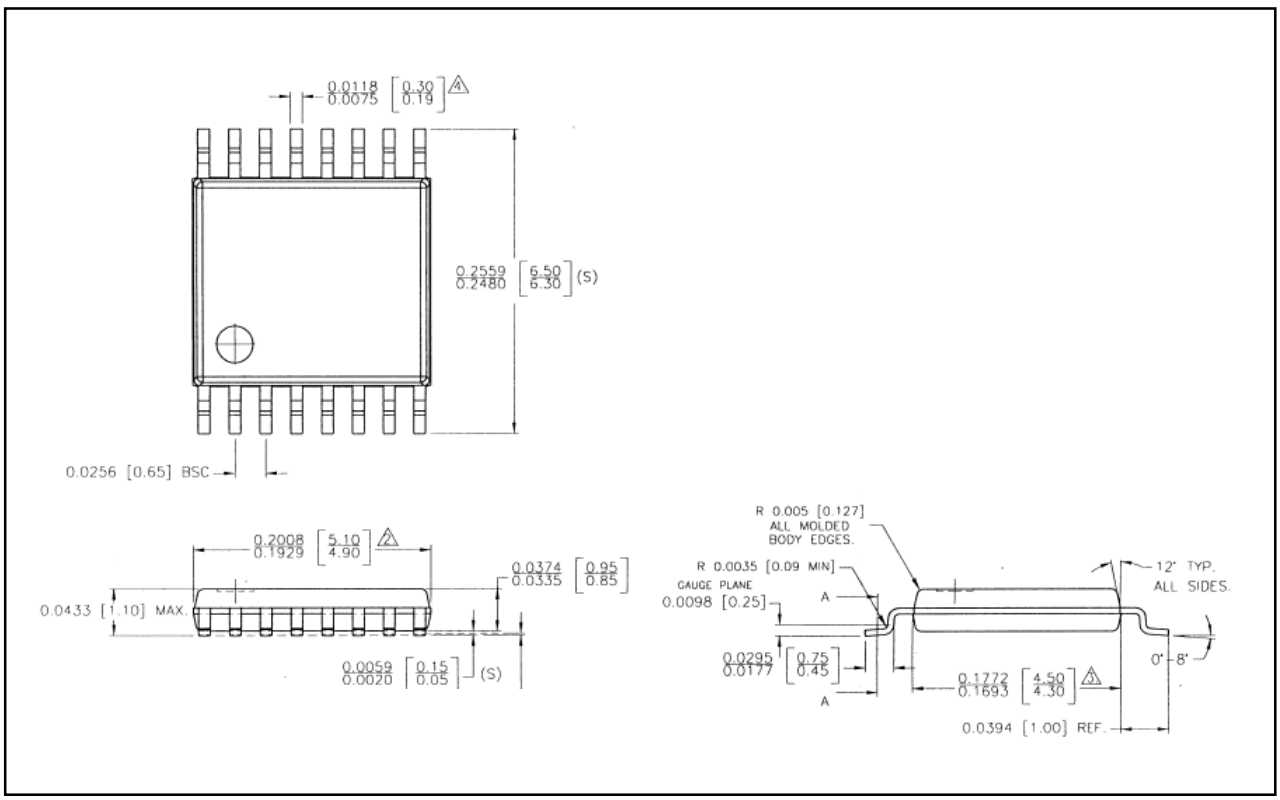


※ *RESETB is selected by setting the OTP Configuration Bit.*

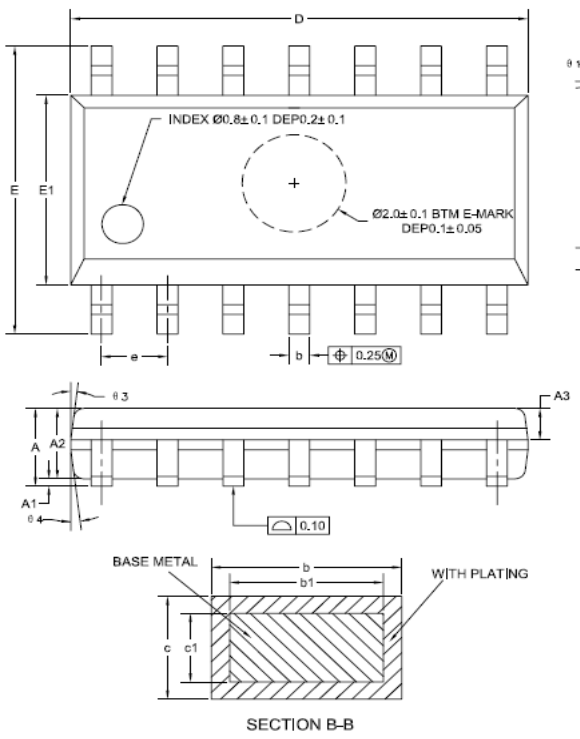
1.4. Package Dimension



16 SOP (150Mil) Pin Dimension (dimensions in millimeters)



16 TSSOP (4.4 mm) Pin Dimension (dimensions in inch [millimeters])

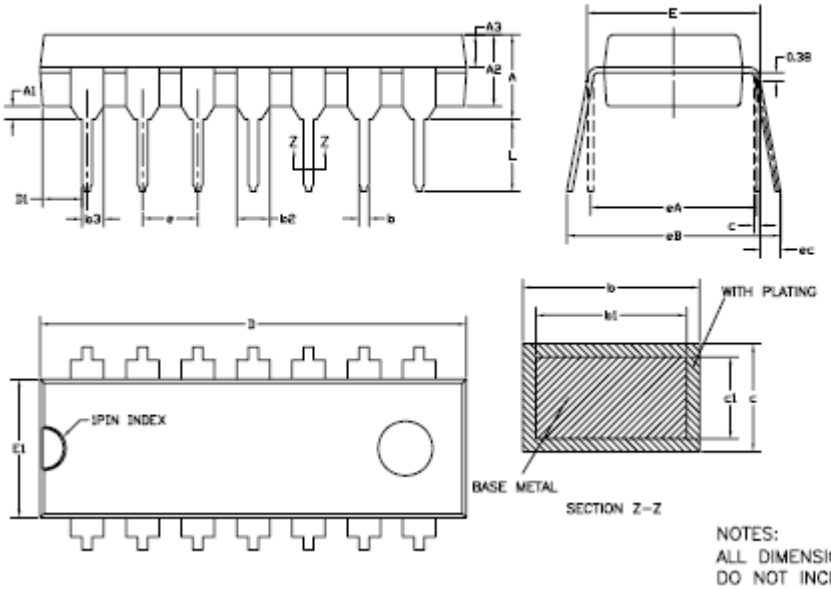


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b	0.36	-	0.49
b1	0.35	0.40	0.45
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	-	-
R1	0.07	-	-
h	0.30	0.40	0.50
θ	0°	-	8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS-012 AB
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

14 SOP (150Mil) Pin Dimension (dimensions in millimeters)

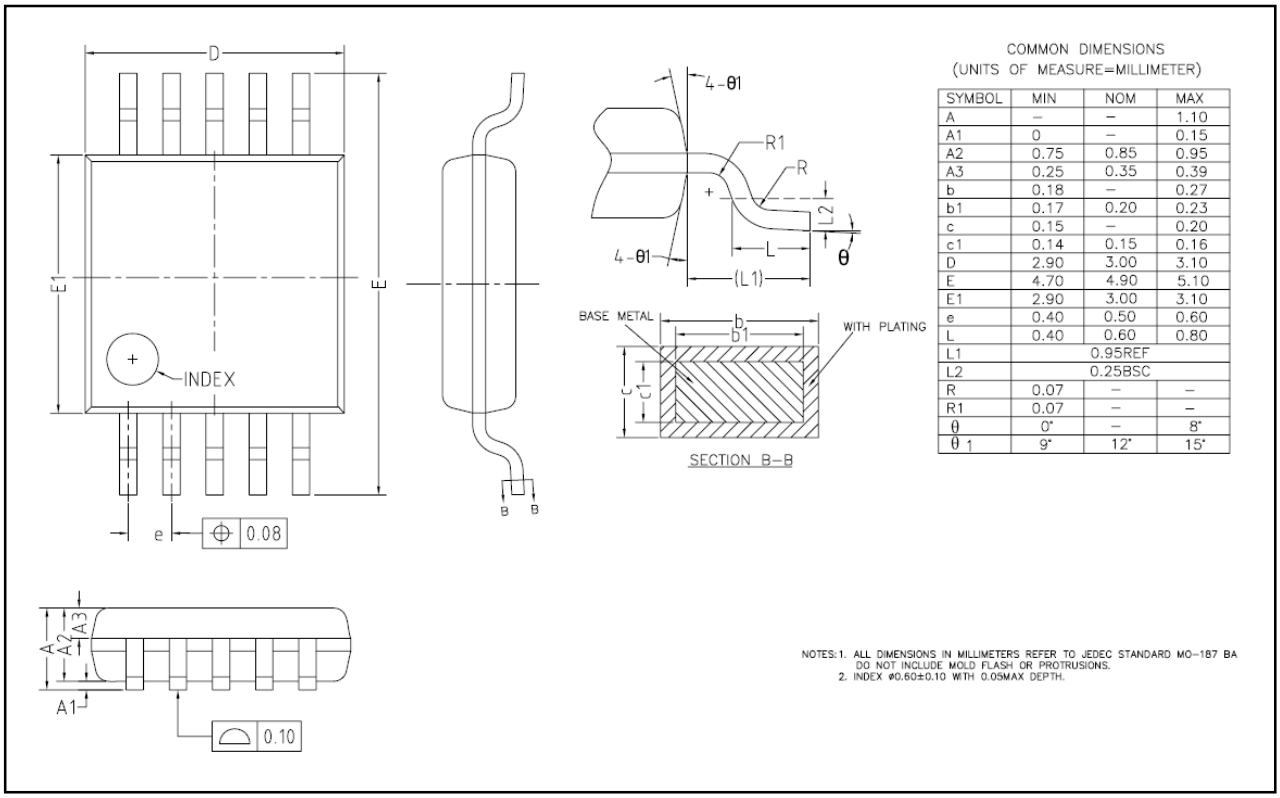


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	4.80
A1	0.50	–	–
A2	3.05	3.25	3.45
A3	1.40	1.50	1.60
b	0.38	–	0.55
b1	0.38	0.46	0.51
b2	1.47	1.52	1.57
b3	0.89	0.99	1.09
c	0.21	–	0.35
c1	0.20	0.25	0.30
D	19.20	19.30	19.40
D1	0.13	–	–
E	7.62	7.87	8.25
E1	6.25	6.35	6.45
e		2.54BSC	
eA		7.62BSC	
eB	7.62	8.80	10.90
eC	0	–	1.52
L	2.92	3.30	3.81

NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS-001 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

14 DIP (300Mil) Pin Dimension (dimensions in millimeters)

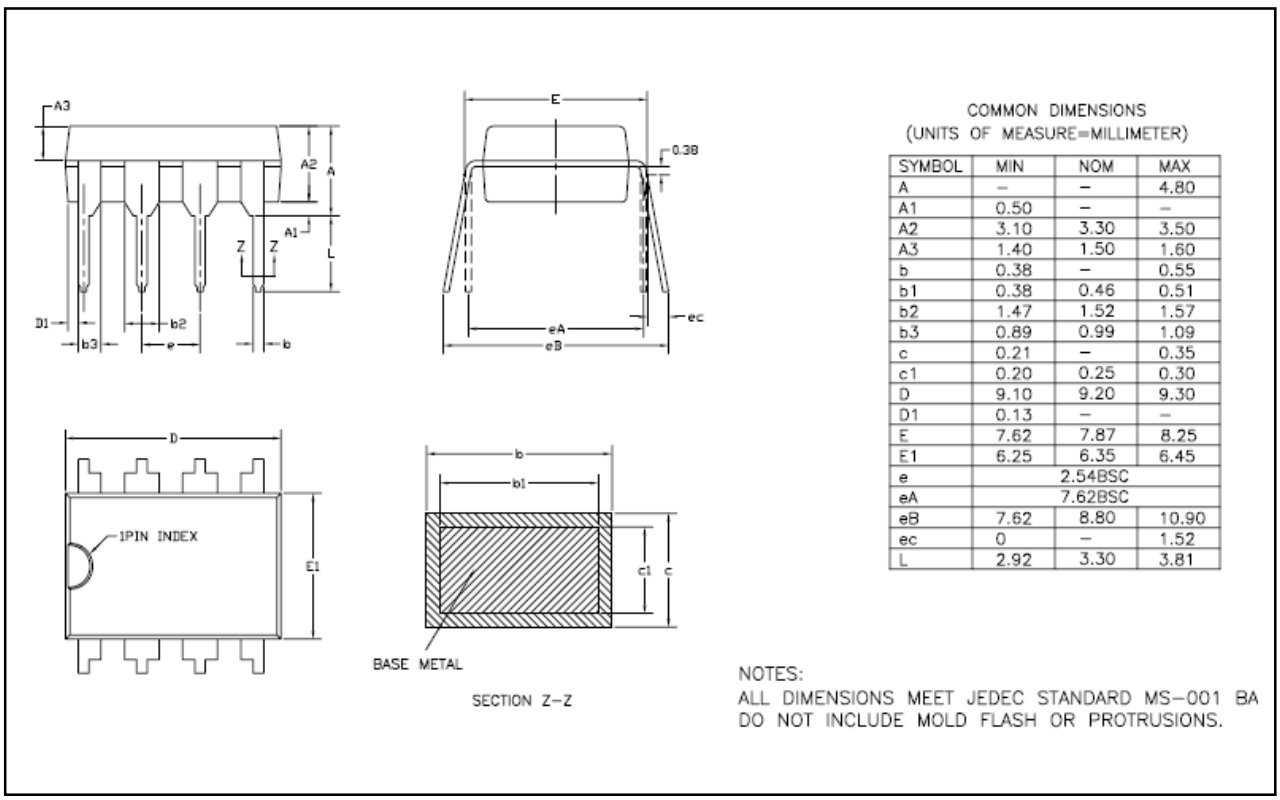


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.10
A1	0	–	0.15
A2	0.75	0.85	0.95
A3	0.25	0.35	0.39
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.15	–	0.20
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.40	0.50	0.60
L	0.40	0.60	0.80
L1		0.95REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
θ	0°	–	8°
θ1	9°	12°	15°

NOTES:1. ALL DIMENSIONS IN MILLIMETERS REFER TO JEDEC STANDARD MO-187 BA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. INDEX φ0.60±0.10 WITH 0.05MAX DEPTH.

10 MSOP Pin Dimension (dimensions in millimeters)

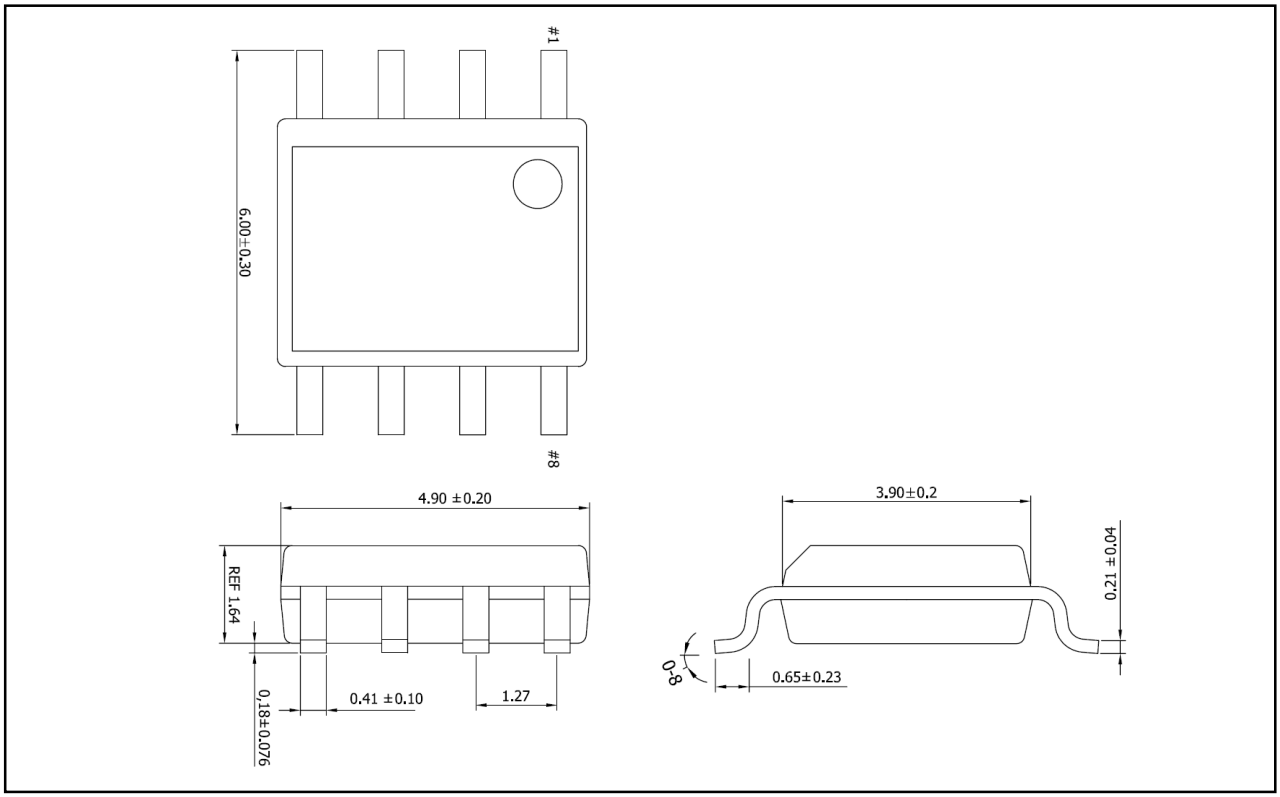


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

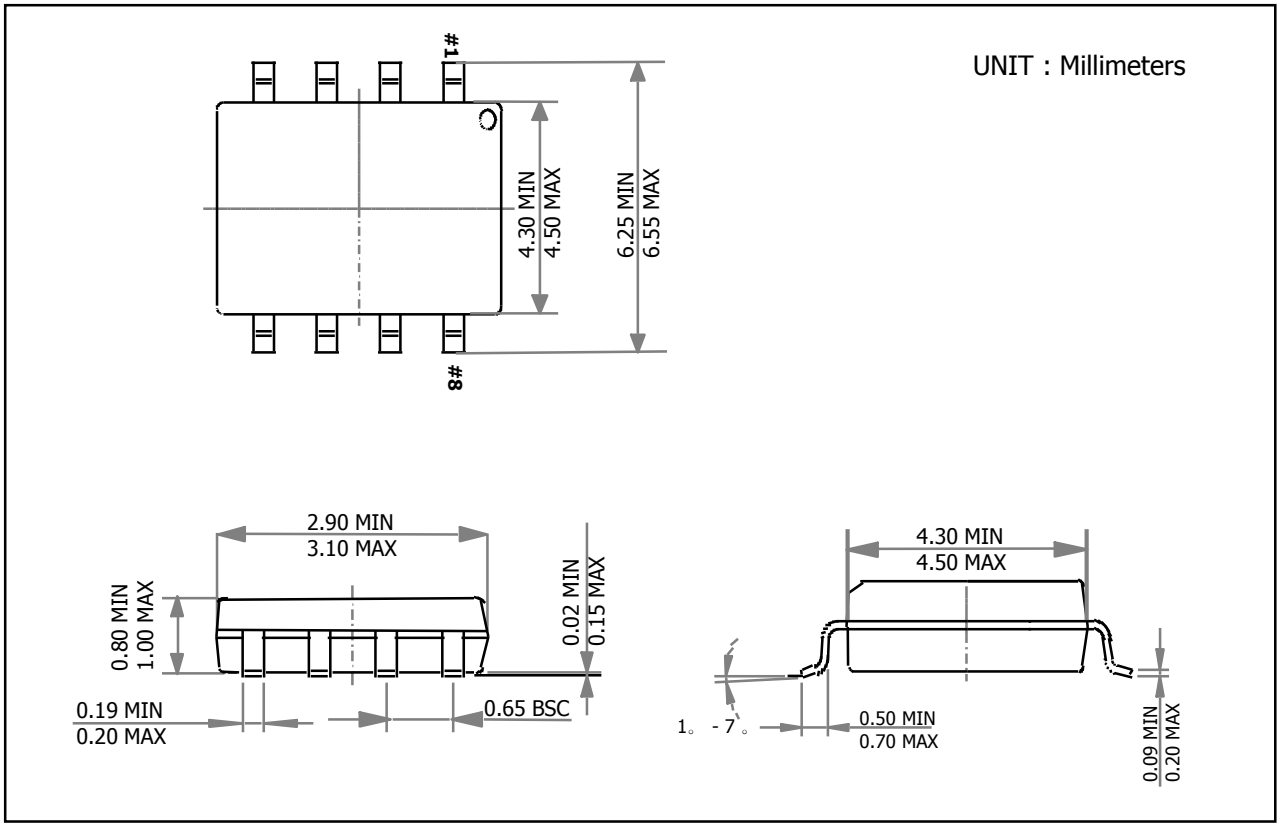
SYMBOL	MIN	NOM	MAX
A	–	–	4.80
A1	0.50	–	–
A2	3.10	3.30	3.50
A3	1.40	1.50	1.60
b	0.38	–	0.55
b1	0.38	0.46	0.51
b2	1.47	1.52	1.57
b3	0.89	0.99	1.09
c	0.21	–	0.35
c1	0.20	0.25	0.30
D	9.10	9.20	9.30
D1	0.13	–	–
E	7.62	7.87	8.25
E1	6.25	6.35	6.45
e		2.54BSC	
eA		7.62BSC	
eB	7.62	8.80	10.90
ec	0	–	1.52
L	2.92	3.30	3.81

NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS-001 BA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

8 DIP (300Mil) Pin Dimension (dimensions in millimeters)



8 SOP (150Mil) Pin Dimension (dimensions in millimeters)



8 TSSOP (4.4 mm) Pin Dimension (dimensions in inch [millimeters])

1.5. Pin Function

1.5.1. Port Pins

Pin Name	I/O	Function	@RESET	@STOP	Shared Pins
PA0	I/O	- 4-bit I/O Port. - CMOS input. - Push-pull output. - Each pin can be set and reset by Data register value. - Can be programmable as N-ch open drain/Pull-up/ Pull-down/KSCN/INT(EC) individually. - Direct driving of LED (N-TR).	Input (without Pull-up)	State of before STOP	KSA0
PA1					KSA1
PA2					INT0(EC0)/KSA2
PA3					KSA3
PB0	I/O	- 4-bit I/O Port. - CMOS input. - Push-pull output (except PB1). - Each pin can be set and reset by Data register value. - Can be programmable as N-ch open drain/Pull-up/ KSCN/Clock/TIMER output individually. - Direct driving of LED (N-TR). - PB1 is N-ch Open drain output only at output mode.	Input (without Pull-up)	State of before STOP	PWM0/KSB0
PB1					RESETB/KSB1
PB2					CLO/KSB2
PB3					KSB3
PD0	I/O	- 4-bit I/O Port. - CMOS input. - Push-pull output. - Each pin can be set and reset by Data register value. - Can be programmable as N-ch open drain/Pull-up/ individually. - Direct driving of LED (N-TR).	Input (without Pull-up)	State of before STOP	-
PD1					-
PD2					-
PD3					-

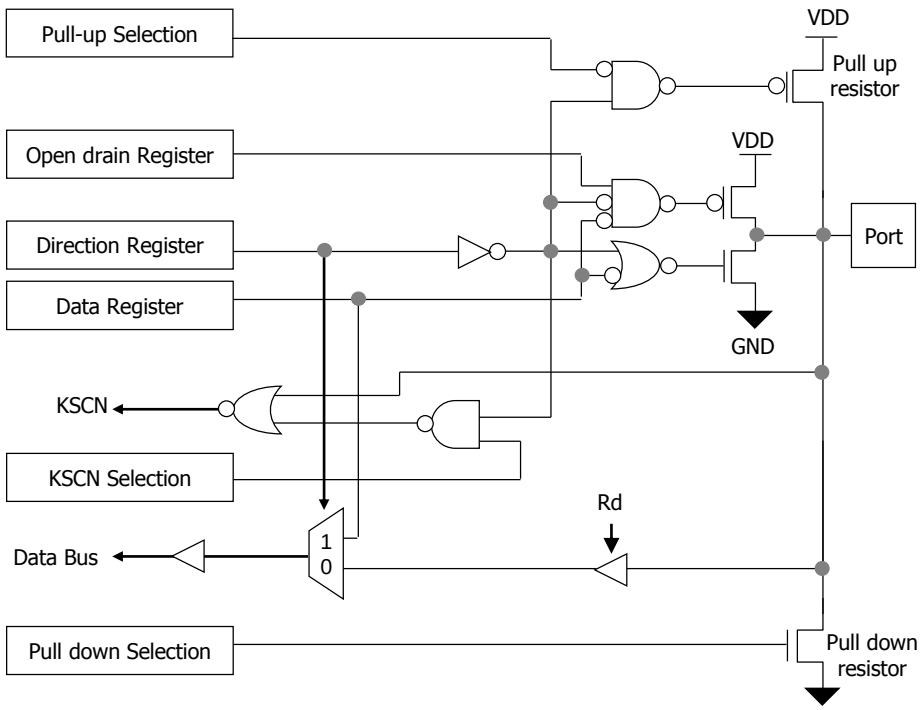
1.5.2. Non-Port Pins

Pin Name	I/O	Function	@RESET	Shared Pins
INT0	I	- External Interrupt input for which the valid edges (rising edge, falling edge , both rising and falling edge) can be specified. - Timer0 capture input.	Input (Pull-up off)	PA2
EC0	I	- Timer0 event counter input.	Input (Pull-up off)	PA2
PWM0	O	- 8-bit PWM0 (shared with Timer0) output.	Input (Pull-up off)	PB0
CLO	O	- System Clock output. (Fosc)	Input (Pull-up off)	PB2
KSA0 ~ KSA3	I	- STOP mode release input which can be selected individually by user program. - It is released by "L" input at STOP mode.	Input (Pull-up off)	PA0 ~ PA3
KSB0 ~ KSB3				PB0 ~ PB3
RESETB	I	- External RESETB Input by Code Option.	Input (Pull-up off)	PB1
VDD	P	- Positive power supply.	-	-
GND	P	- Ground.	-	-

1.5.3. OTP Programming Pin Description (OTP Program Mode)

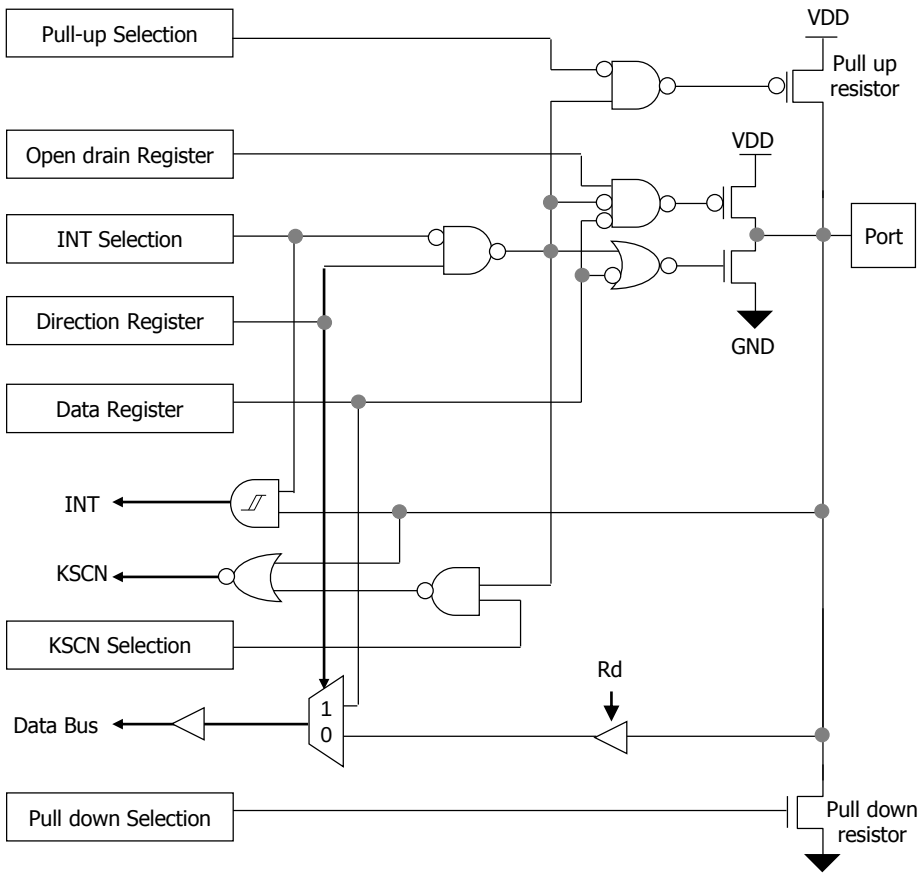
Pin No.				Pin Name	I/O	Function	Shared Pins
8Pin	10pin	14pin	16pin				
#1	#2	#4	#5	VDD	P	- Programming Power supply (+ 5.0V)	VDD
#4	#5	#7	#8	VPP	P	- Programming high voltage Power supply (+11.5V)	PB1/RESETB
#8	#9	#11	#12	GND	P	- Ground	GND
#6	#7	#9	#10	SCK	I	- Programming Clock input pin	PA3
#7	#8	#10	#11	SDA	I/O	- Programming Data Input/Output pin	PA2/INT0(EC0)

1.6. Port Structure

Pin Name	Circuit Type	RESET
PA0 **PA1** **PA3**		Input (without Pull-up)
Shared Function	KSCN	

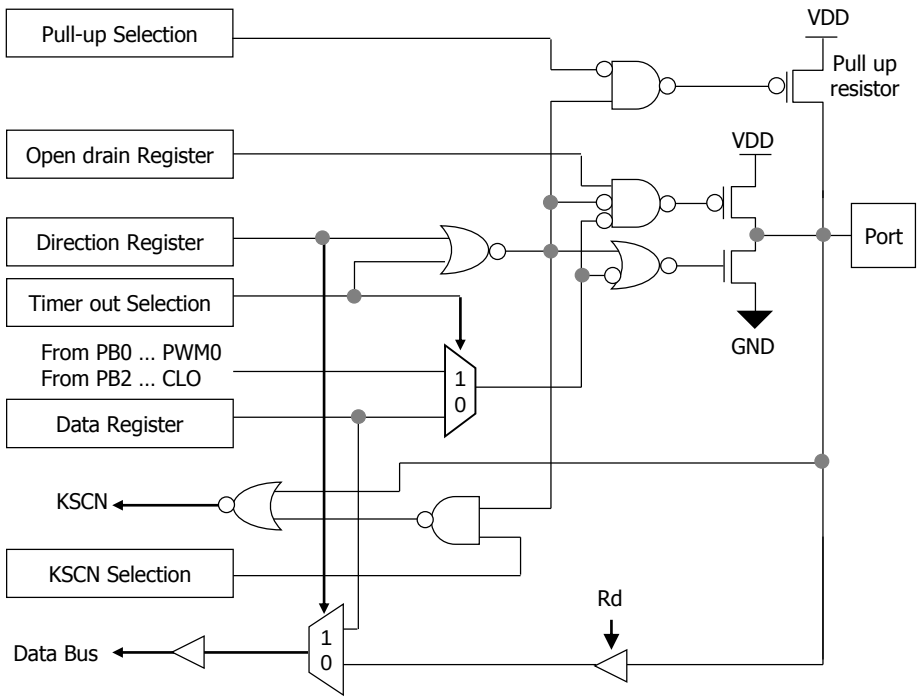
Assignment	Direction	Pull-Up	Pull -Down	Port Read		Port	Remarks	RESET
				Dir. Input	Dir. Output			
KSCN	**	**	**	Port	Data	KSA0 KSA1 KSA3		Disable

** : It is depend on user definition.

Pin Name	Circuit Type	RESET
PA2		Input (without Pull-up)
Shared Function	KSCN/INT(EC)	

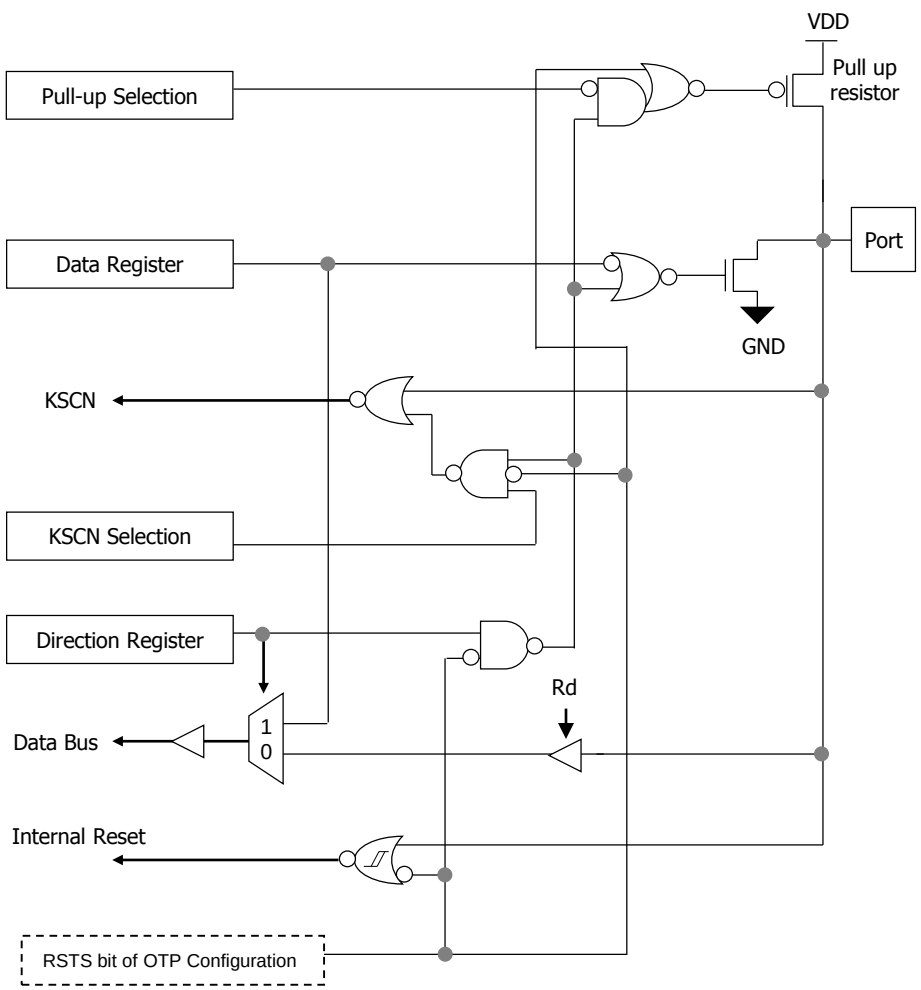
Assignment	Direction	Pull-Up	Pull -Down	Port Read		Port	Remarks	RESET
				Dir. Input	Dir. Output			
KSCN	**	**	**	Port	Data	KSA2		Disable
INT	Input	**	**	Port	Data	INT0(EC0)	Schmitt input	

** : It is depend on user definition.

Pin Name	Circuit Type	RESET
PB0 **PB2**		Input (without Pull-up)
Shared Function	KSCN/TIMER	

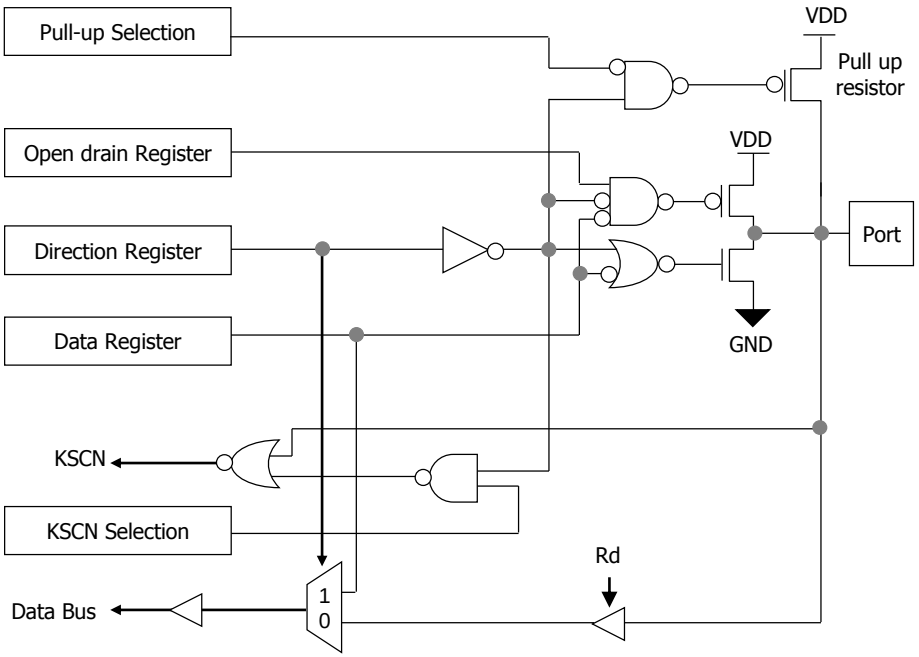
Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
KSCN	**	**	Port	Data	KSB0 KSB2		Disable
TIMER	Output	Off	Port	Data	PWM0 CLO		

** : It is depend on user definition.

Pin Name	Circuit Type	RESET
PB1		Input
Shared Function	KSCN/RESETB	

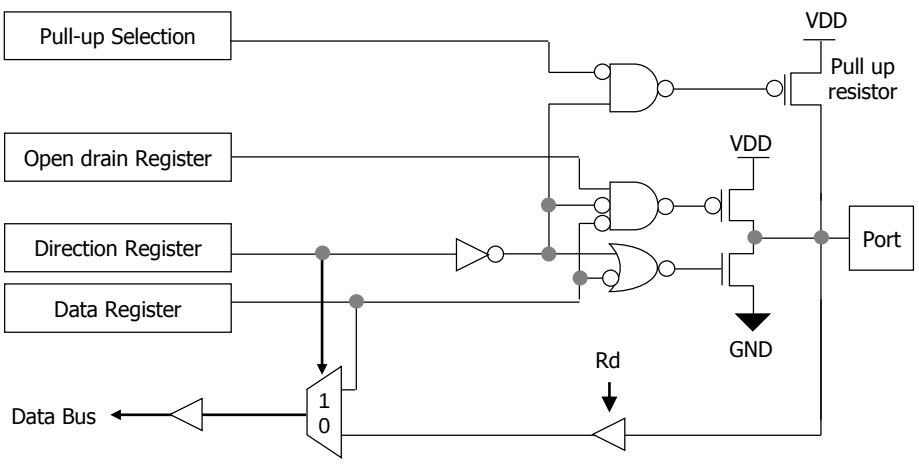
Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
KSCN	**	**	Port	Data	KSB1		Disable
RESETB	Input	On	Unknown	Data	RESETB	Schmitt input with pull-up	RESETB

** : It is depend on user definition.

Pin Name	Circuit Type	RESET
PB3		Input (without Pull-up)
Shared Function	KSCN	

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
KSCN	**	**	Port	Data	KSB3		Disable

** : It is depend on user definition.

Pin Name	Circuit Type	RESET
PD0 **PD1** **PD2** **PD3**		Input (without Pull-up)
Shared Function	---	

1.7. Electrical Characteristics

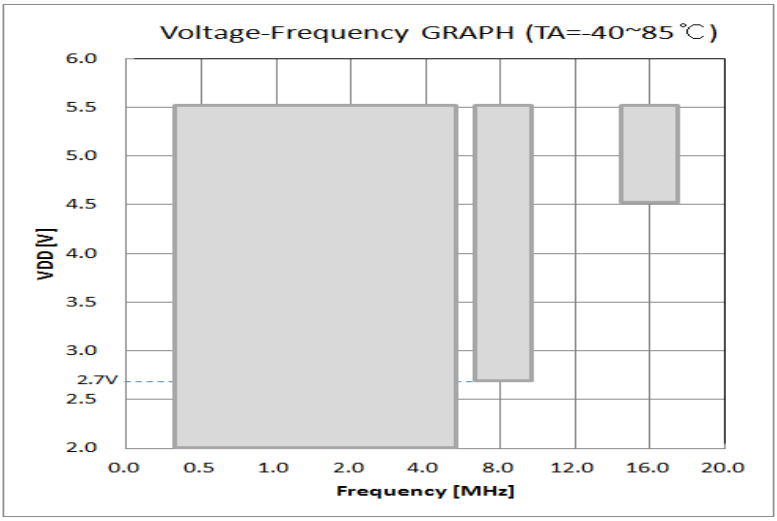
1.7.1. Absolute Maximum Ratings (Ta = 25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +6.0	V
Input Voltage	V_I	-0.3 ~ VDD + 0.3	V
Output Voltage	V_O	-0.3 ~ VDD + 0.3	V
Storage Temperature	T_{STG}	-65 ~ 150	°C
Power Dissipation	P_D	700	mW

1.7.2. Recommended Operating Ranges

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX	UNIT
Supply Voltage	V_{DD}	f_{OSC} = 0.5M ~ 4MHz	2.0	-	5.5	V
		f_{OSC} = 8MHz	2.7	-	5.5	V
		f_{OSC} = 16MHz	4.5	-	5.5	V
Operating Temperature	T_{OPR}		-40	-	85	°C
Oscillation Frequency	f_{OSC}	Calibrated Internal RC Oscillator (Ta=-20 ~ 70℃)	15.68	16.00	16.32	MHz
			7.84	8.00	8.16	
			3.92	4.00	4.08	
			1.96	2.00	2.04	
			0.98	1.00	1.02	
			0.490	0.500	0.510	
			(-2%)	-	(+2%)	
		Calibrated Internal RC Oscillator (Ta=-40~85℃)	15.52	16.00	16.48	MHz
			7.76	8.00	8.24	
			3.88	4.00	4.12	
			1.94	2.00	2.06	
			0.97	1.00	1.03	
			0.485	0.500	0.515	
			(-3%)	-	(+3%)	

▶ Voltage-Frequency Graph :



1.7.3. DC Characteristics (Ta = 25℃)

PARAMETER	Symbol	Condition			Specification			UNIT
					MIN.	TYP.	MAX.	
High level input voltage	V_{IH1}	RESETB, INT0/EC0			0.8VDD		VDD	V
	V_{IH2}	PA, PB, PD			0.7VDD		VDD	V
Low level input voltage	V_{IL1}	RESETB, INT0/EC0			0		0.2VDD	V
	V_{IL2}	PA, PB, PD			0		0.3VDD	V
High level input leakage current	I_{IH}	PA, PB, PD		VIH = VDD			1	uA
Low level input leakage current	I_{IL}	PA, PB, PD		VIL = 0V			-1	uA
High level output voltage	V_{OH1}	PA, PB, PD (Except PB1)	VDD = 5V	IOH = -10mA	VDD-1.0			V
Low level output voltage	V_{OL1}	PA, PB, PD	VDD = 5V	IOL = 15mA			1.0	V
High level output leakage current	I_{OHL}	PA, PB, PD		VOH = VDD			1	uA
Low level output leakage current	I_{OLL}	PA, PB, PD		VOL = 0V			-1	uA
Input Pull-up Current	I_{PU}	PA, PB, PD	VDD = 5V		-100	-50	-25	uA
Input Pull-down Current	I_{PD}	PA	VDD = 5V		25	50	100	uA
Power supply current	I_{DD}	Operating Mode	VDD = 5V	fXIN = 16MHz	-	2.4	-	mA
			VDD = 5V	fXIN = 8MHz	-	1.8	-	mA
			VDD = 3V		-	0.9	-	
			VDD = 5V	fXIN = 4MHz	-	1.2	-	mA
			VDD = 3V		-	0.6	-	
			VDD = 5V	fXIN = 2MHz	-	0.9	-	mA
			VDD = 3V		-	0.5	-	
			VDD = 5V	fXIN = 1MHz	-	0.8	-	mA
			VDD = 3V		-	0.4	-	
			VDD = 5V	fXIN = 0.5MHz	-	0.7	-	mA
			VDD = 3V		-	0.3	-	
	I_{STOP}	Stop Mode (Oscillator Stop)	VDD = 5V	RCWDT On	-	8	-	uA
			VDD = 3V		-	5	-	
			VDD = 5V	LVD On	-	2	-	uA
			VDD = 3V		-	1	-	
			VDD=5V/3V	LVD Off		-	1	uA
RCWDT Frequency	F_{RCWDT}	RCWDT	VDD = 5V		32	64	128	KHz
			VDD = 3V		16	32	64	
RAM retention supply voltage	V_{RET}				0.7			V
Low Voltage Detection	LVD	LVDS=1 (in the Configuration Bits), Ta=25℃			1.6	1.8	2.0	V
		LVDS=0 (in the Configuration Bits), Ta=25℃			2.0	2.2	2.6	V
Voltage Detection Indication Level	V_{VDI1}	Voltage detection indicator level 1			-	2.2	-	V
	V_{VDI2}	Voltage detection indicator level 2			-	3.3	-	V

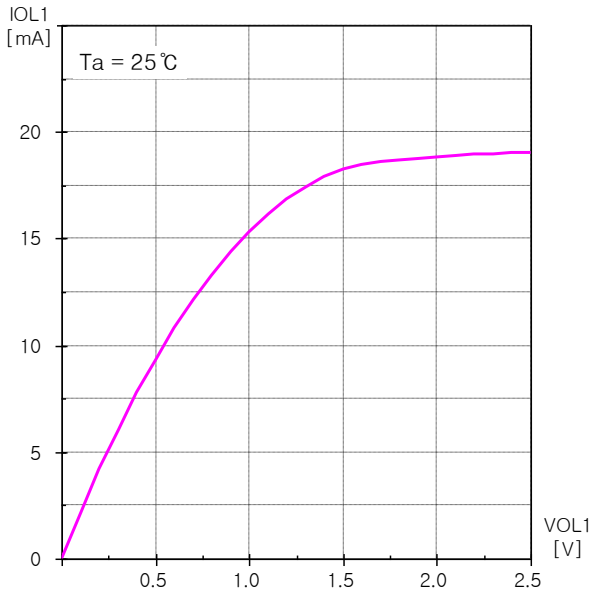
※ Typical Characteristics

This graphs provided in this section are for design guidance only and are not tested or guaranteed.

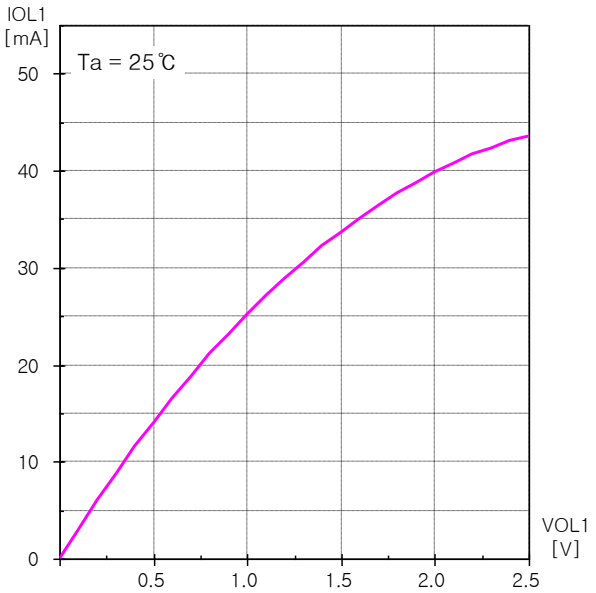
The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean – 3σ) respectively where σ is standard deviation.

▶ IOL1 vs. VOL1 (at T=25℃)

IOL1-VOL1, VDD=3.0V

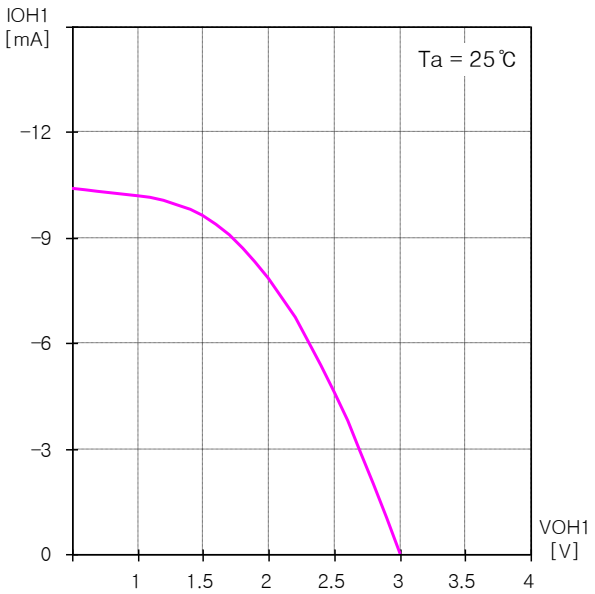


IOL1-VOL1, VDD=5.0V

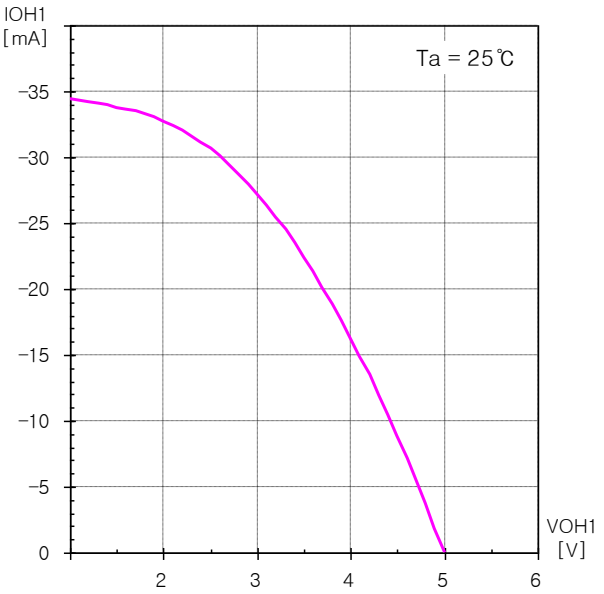


▶ IOH1 vs. VOH1 (at T=25℃)

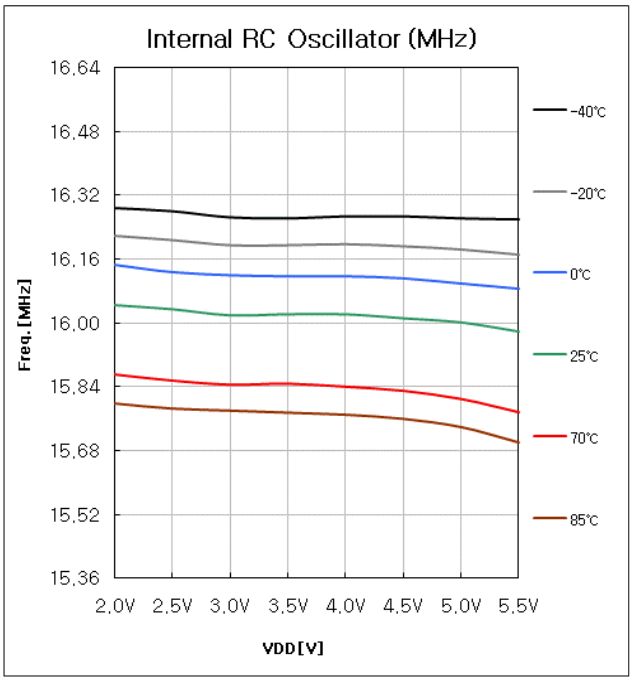
IOH1-VOH1, VDD=3.0V

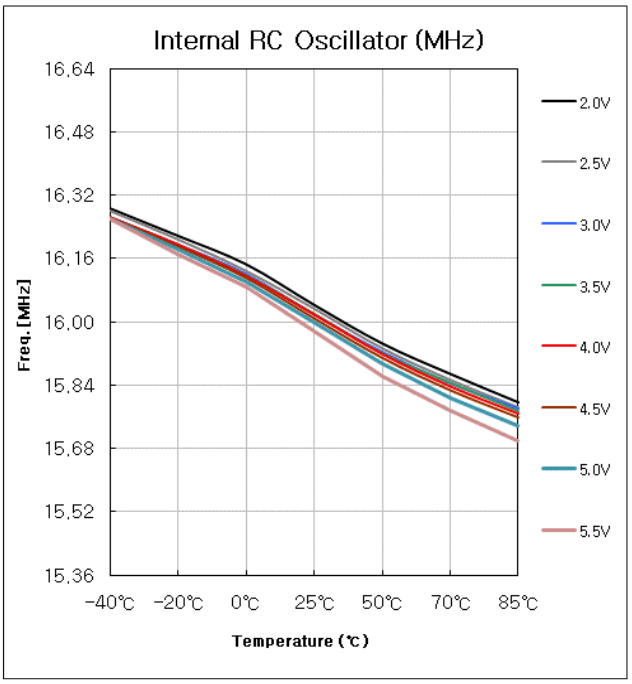


IOH1-VOH1, VDD=5.0V

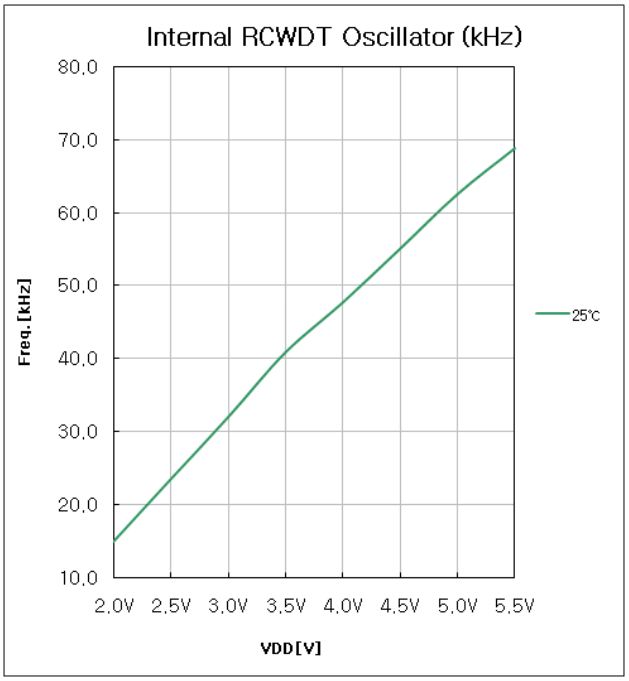


▶ Internal RC Oscillator Characteristics

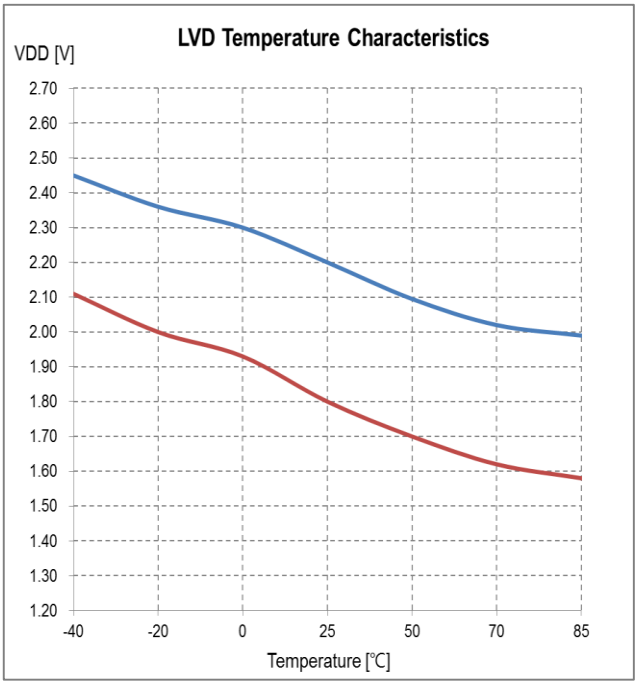




▶ Internal RCWDT Oscillator Characteristics



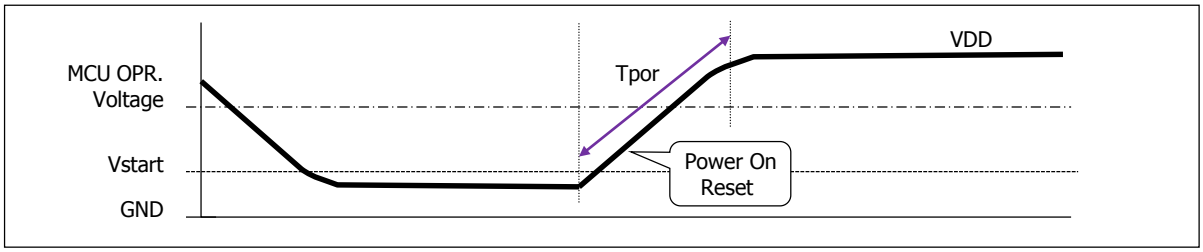
▶ Low Voltage Detection (Temperature Characteristics)



1.7.5. POR(Power on Reset) Electrical Characteristics (VDD=5.5V~2.0V, VSS=0V, Ta = -40℃~85℃)

Parameter	Symbol	Condition	Specification			Unit
			MIN	TYP	MAX	
POR Start voltage	Vstart*	Tpor > 0.35V/ms	VSS	-	0.2	V
		Tpor > 0.05V/ms	-	-	VSS	V
VDD Voltage Rising Time	Tpor*		0.05	-	-	V/ms

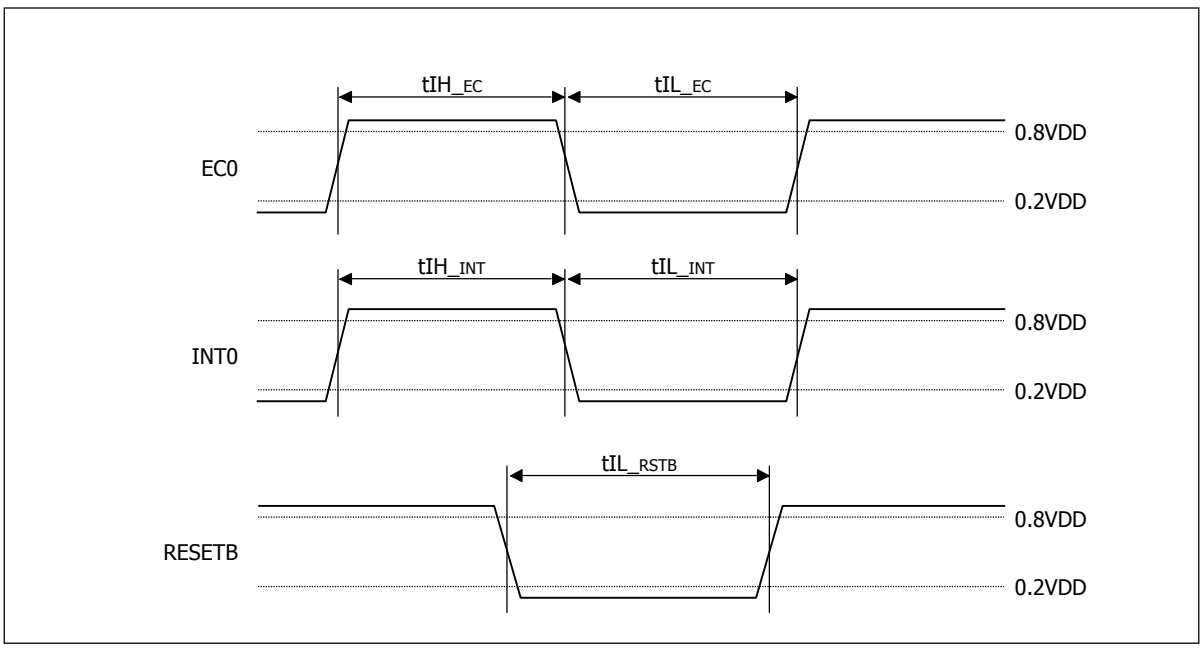
*) These parameters are presented for design guidance only and not tested or guaranteed.



1.7.6. AC Characteristics (Ta = 25℃)

Parameter	Symbol	Pin	Specification			Unit
			min.	typ.	max.	
Internal clock cycle time	tCP	-	62.5	250	1000	ns
System clock cycle time	tSYS	-		4		tCP
External pulse width High	tIH_{EC}	EC0	1			tCP
External pulse width Low	tIL_{EC}	EC0	1			tCP
Externa pulse width Low	tIL_{RSTB}	RESETB	8			tSYS
Interrupt pulse width High	tIH_{INT}	INT0	2			tSYS
Interrupt pulse width Low	tIL_{INT}	INT0	2			tSYS

Minimum pulse width



2.1. Program Memory

The ADAM46P20XX can address maximum 2Kbytes (1K words × 16bits) for program memory. Program counter PC (A0~A9) is used to address the whole area of program memory having an instruction (16bits) to be next executed.

The program memory consists of 1K words.

The program memory is composed as shown below.

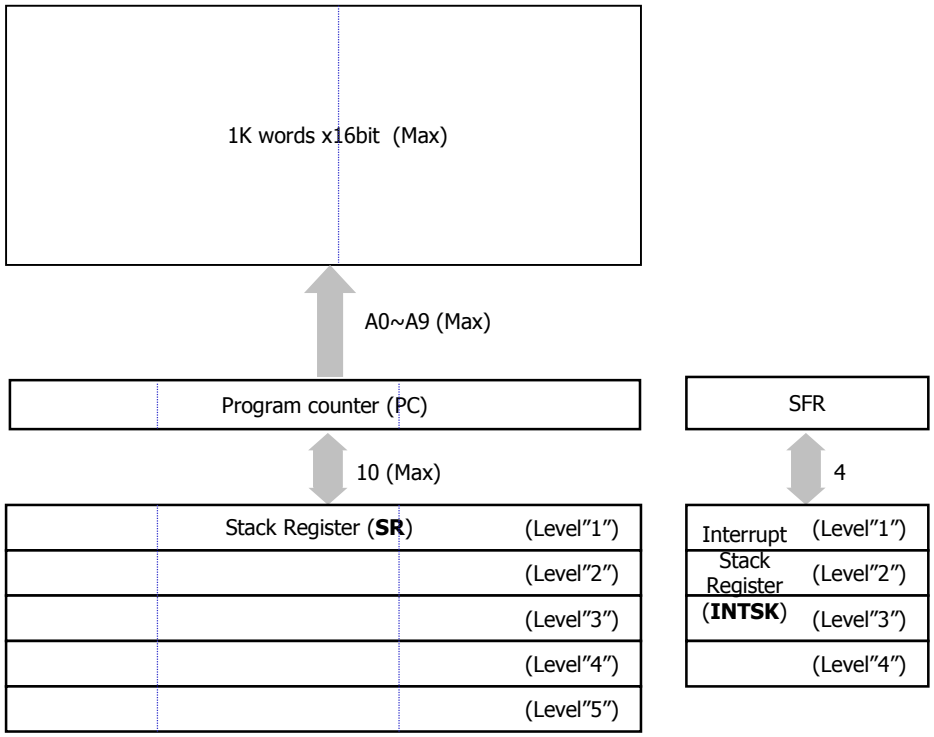


Fig 2-1 Configuration of Program Memory

2.2. Address Register

The following registers are used to address the ROM.

- **Program counter (PC) :**
  Available for addressing word on each page.
- **Stack register (SR) :**
  Stores returned-word address in the subroutine call mode.

2.2.1 Program counter :

This 10-bit binary counter increments for fetching a word to be addressed in the currently addressed page having an instruction to be next executed.
For easier programming, at turning on the power, the program counter is reset to the zero location(0000H). Then the program counter specifies the next address.
When BR, CAL or RET instructions are decoded, the switches on each step are turned off not to update the address. Then, for BR or CAL, address data are taken in from the instruction operands (A0 to A9), or for RET, and address including page address is fetched from stack register No. 1.

2.2.2. Stack register (SR)

The address stack register (ADS) stores a return address when the subroutine call instruction is executed or interrupt is acknowledged.
If subroutine or interrupts are nested to more than 5 levels, internal reset is occurred.
The interrupt stack register(INTSK) saves the contents of Status Flag Register (SFR) when an interrupt is acknowledged.
The saved contents are restored when an interrupt return(RETI) instruction is executed.
INTSK saves data each time an interrupt is acknowledged.
The programmer must keep in mind that the level of INTSK is 4. So, if more over 4 levels of interrupt occur, the first stored data is lost. There is different result between Stack overflow and interrupt stack overflow.
When clearing SP (Stack Pointer) with using "SPC" instruction, interrupt processing must be inhibited before "SPC".

2.3. Data Memory (RAM)

64 nibbles (64 × 4bits) is incorporated for storing data.

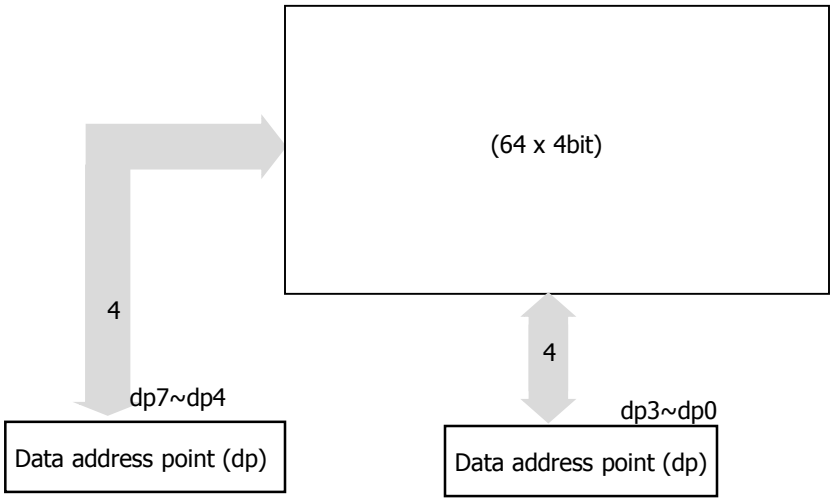
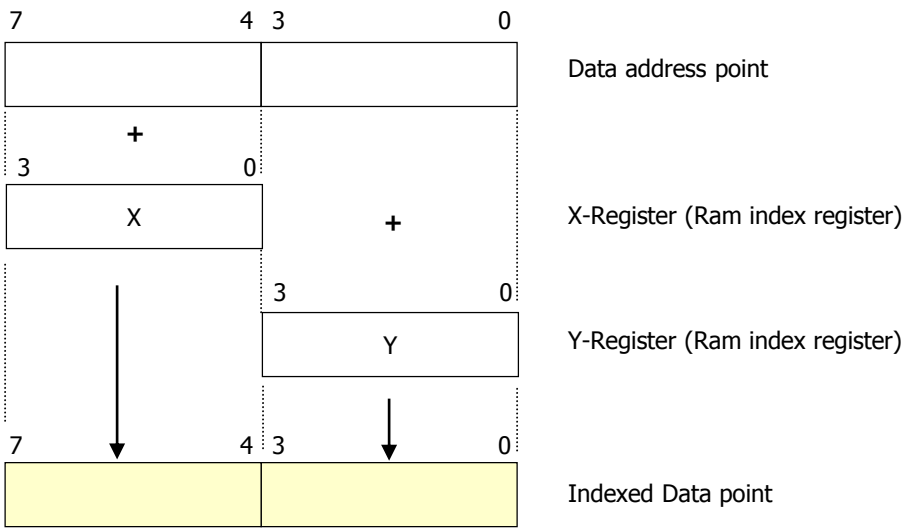


Fig 2-2 Data Memory

2.3.1. Data memory(RAM) addressing method

The whole data memory area is directly addressed by 8-bit ram data address point (dp).

Index data memory addressing is available using X-register and Y-register.
In this case, X-register is added upper 4bit of data point and Y-register is added lower 4bit of data point.



2.3.2. Data memory(RAM) data addressing example Program

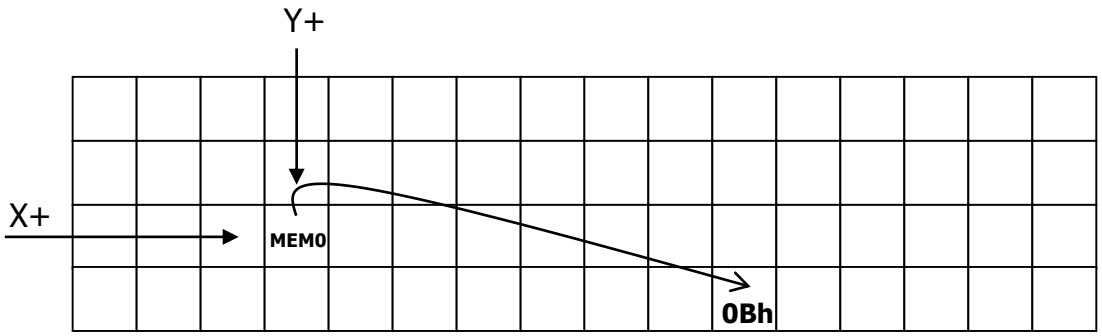


Fig 2-3 Data Memory Map

Below program example is guidance for understanding the flow of index data memory addressing.

```
MEM0 EQU    023h                ; Defining RAM Address

       LDM    MEM0,#0Bh         ; [23h]  = #0Bh
       LYI    #7                ; Setting Y register as #07h
       LXI    #1                ; Setting X register as #01h
       LDA    MEM0              ; A = #0Bh == [MEM0]
       EIX                      ; Index Enable
       LDM    MEM0,A            ; [3Ah] == [Indexed Addressed Ram] = A
       DIX                       ; Index Disable
```

Result after executing is
MEM0 = #0Bh
[MEM0 + X + Y] = = [3Ah] = #0Bh

2.4. General Function Registers

2.4.1. X-register (X)

X-register is consist of 4 bits, X-register is used for data memory indexing register.

2.4.2. Y-register (Y)

Y-register is consist of 4 bits. It can used for a general-purpose register.
Y-register also used for data memory indexing register.

2.4.2. Accumulator (ACC)

The 4-bit register for holding data and calculation results.

2.4.3. Peripheral Address Register(PAR)

The 6-bit address register for addressing peripheral registers including
address buff register(ABR) , data buff register (DBR).

2.4.4. Address Buff Register (ABR)

The 16-bit register for address buffer.
It is composed of 4 registers(ABR0, ABR1, ABR2, ABR3).
It is written-only registers and can not used the instruction of bit manipulation.
The address of Address Buffer Register (ABR) is 38h ~3Bh on the peripheral register (PAR).
The most important function of ABR is ROM address pointer.
If ROM address point is 345h, each ABR must be written as ABR3=0h, ABR2=3h, ABR1=4h, ABR0=5h.
ABR must be used for reading data from ROM. The data pointed by ABR is read to DBR.
* Caution : Before using ABR, ABR3 register must be always initialized("LRI ABR3,#0").

2.4.5. DATA Buff Register (DBR)

The 16-bit register for Data buffer.
It is composed of 4 registers(DBR0, DBR1, DBR2, DBR3) x 4bit.
The address of Data Buffer Register (DBR) is 3Ch ~3Fh on the peripheral register (PAR).
It is read-only registers and can not used the instruction of bit manipulation.

2.5. Function of Data Buff Register(DBR)

The most important function of DBR is intermediate (window) buffer for transferring data between peripheral registers and reading data from ROM.
When the data of ROM is read by "LDW @ABR", one word of ROM is fetched to DBR.
The MSB of ROM data is written to DBR3 and LSB to DBR0.
If the data of pointed ROM is 1234h, each DBR has the data as DBR0 = 4h, DBR1 = 3h, DBR2 = 2h and DBR3 = 1h.
DBR is also used for reading some peripheral register data by 8bit unit.
The peripheral registers is T0CR.

Note) HEX. File maps the data as big endian type. Be careful to read the ROM data.
When the programmer assigns the data like below, the ROM data is mapped as below.
DB 12h, 34h → ROM data = 1234h

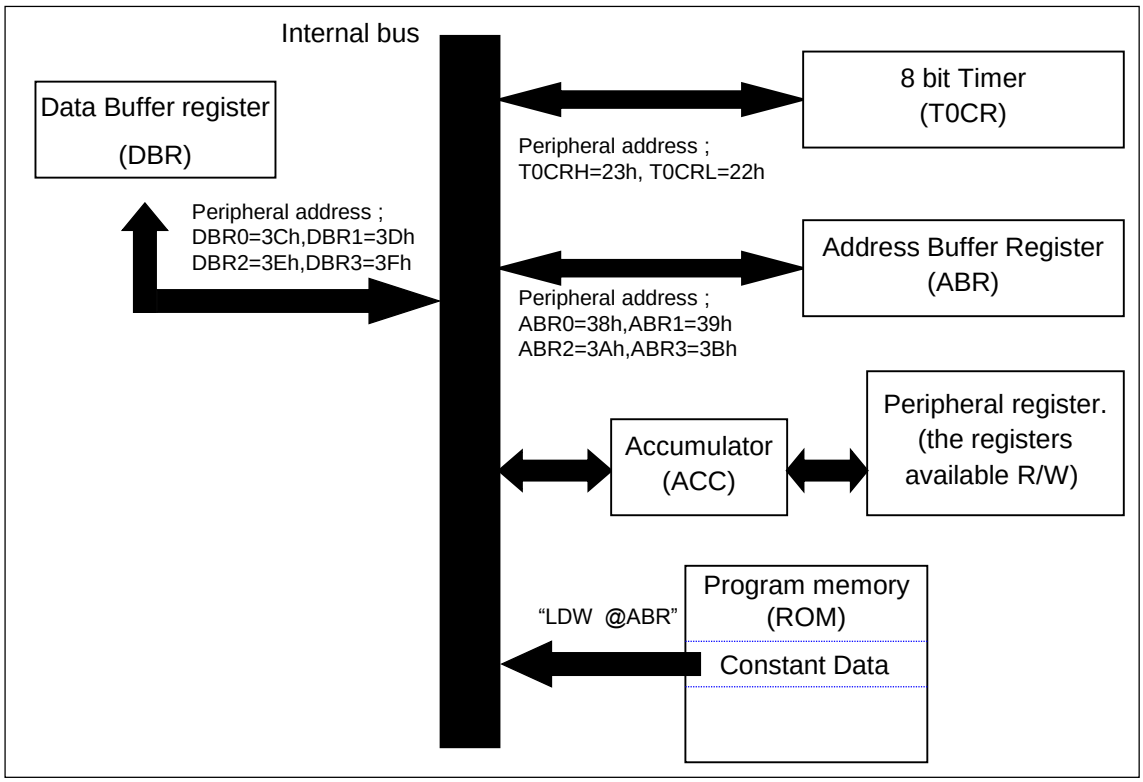


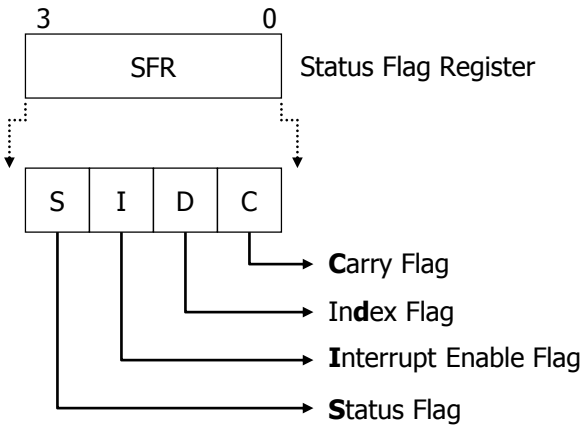
Fig 2-4 The internal Data flow among DBR, ABR, registers and ROM

2.6. Status Flag Registers (SFR)

Status Flag Register (SFR) consists of 4-bit register.

Each of the flags show the post state of operation and the flags determining the CPU operation, initialized as 8h in reset state.

When an interrupt is occurred, the value of SFR keep the value of pre-interrupt except for I flag. So, be careful to initialize the SFR status for getting reliable result in Interrupt sub-routine.



2.6.1 Carry flag (C)

- Carry flag bit is set when there is carry or borrow After executing ADDC / SUBC / ARRC/ARLC instructions.
- Set by SETC and clear by CLRC.
- Load from the assigned bit of Peripheral Registers by LDC
- Transfer to the assigned bit of Peripheral Registers by STC

2.6.2 Index flag (D)

- The control bit of ram data address point indexed or not.
- X-register and Y-register is used for index addressing.
- Set and cleared by EIX, DIX.

2.6.3 Interrupt enable flag (I)

- Master enable flag of interrupt.
- Set and cleared by EI, DI
- This Flag immediately becomes "0" when an interrupt is served.

2.6.4 Status flag (S)

- According to the condition after executing an instruction , set or clear.
- Can not be set or clear by any instruction.
- This Flag decides whether operation of BR and CALL would be done or not.
- Initialized as "1" in reset state.

2.7. Peripheral Registers

Peripheral Address	Function Registers	Read Write	Symbol	RESET Value 3 2 1 0
00 h	PORT PA DATA REG.	R/W	*PADR	F
01 h	PORT PA PULL-UP SELECTION REG.	W	PAPU	F
02 h	PORT PA OPEN DRAIN SELECTION REG.	W	PAOD	F
03 h	PORT PA DIRECTION REG.	R/W	PADD	0
04 h	PORT PA STOP RELEASE SELECTION REG.	W	PAST	F
05 h	PORT PA FUNCTION SELECTION REG.	W	PAFN	0
06 h	PORT PA PULL-DOWN SELECTION REG.	W	PAPD	0
07 h	*Reserved*			
08 h	PORT PB DATA REG.	R/W	*PBDR	F
09 h	PORT PB PULL-UP SELECTION REG.	W	PBPU	F
0A h	PORT PB OPEN DRAIN SELECTION REG.	W	PBOD	F
0B h	PORT PB DIRECTION REG.	R/W	PBDD	0
0C h	PORT PB STOP RELEASE SELECTION REG.	W	PBST	F
0D h	PORT PB FUNCTION SELECTION REG.	W	PBFN	0
0E h	*Reserved*			
0F h	*Reserved*			
10 h	PORT PD DATA REG.	R/W	*PDDR	F
11 h	PORT PD PULL-UP SELECTION REG.	W	PDPU	F
12 h	*Reserved*			
13 h	*Reserved*			
14 h	*Reserved*			
15 h	*Reserved*			
16 h	EXT. INTERRUPT EDGE SELECTION REG.	W	IEDS0	0
17 h	SYSTEM CONTROL REG.	W	SCTLR	0
18 h	PORT PD OPEN DRAIN SELECTION REG.	W	PDOD	F
19 h	PORT PD DIRECTION REG.	R/W	PDDD	0
1A h	*Reserved*			
1B h	*Reserved*			
1C h	INTERRUPT REQUEST FLAG REG. 0	R/W	IRQR0	0
1D h	*Reserved*			
1E h	INTERRUPT ENABLE REG. 0	R/W	IENR0	0
1F h	*Reserved*			

Note1> '-' is reserved bit , it must be read to "0".
Note2> * Using the bit access Instruction, bit is read-modified operation (SETR1/CLRR1/STC Instructions)

Peripheral Address	Function Registers	Read Write	Symbol	RESET Value
				3 2 1 0
20 h	TIMER-0 MODE REG. 0	R/W	T0MR0	0
21 h	TIMER-0 MODE REG. 1	W	T0MR1	0
22 h	TIMER-0 DATA 0 LOW REG.	W	T0D0L	undefined
	TIMER-0 COUNT REG. LOW	R	T0CRL	undefined
	TIMER-0 CAPTURE LOW REG.	R	T0CPL	undefined
23 h	TIMER 0 DATA 0 HIGH REG.	W	T0D0H	undefined
	TIMER 0 COUNT REG. HIGH	R	T0CRH	undefined
	TIMER-0 CAPTURE HIGH REG.	R	T0CPH	undefined
24 h	TIMER-0 DATA 1 LOW REG.	W	T0D1L	undefined
25 h	TIMER-0 DATA 1 HIGH REG.	W	T0D1H	undefined
26 h	*Reserved*			
27 h	*Reserved*			
28 h	*Reserved*			
29 h	*Reserved*			
2A h	*Reserved*			
2B h	*Reserved*			
2C h	*Reserved*			
2D h	*Reserved*			
2E h	*Reserved*			
2F h	*Reserved*			
30 h	*Reserved*			
31 h	*Reserved*			
32 h	*Reserved*			
33 h	VTG. DETECTION INDICATOR ENABLE REG.	W	VDIER	0
	VTG DETECTION INDICATOR FLAG REG.	R	VDIR	- - 0 0
34 h	*Reserved*			
35 h	*Reserved*			
36 h	*Reserved*			
37 h	WATCH-DOG TIMER CONTROL REG.	W	WDTCR	0
38 h	ADDRESS BUFF REGISTER 0	W	ABR0	undefined
39 h	ADDRESS BUFF REGISTER 1	W	ABR1	undefined
3A h	ADDRESS BUFF REGISTER 2	W	ABR2	undefined
3B h	ADDRESS BUFF REGISTER 3	W	ABR3	undefined
3C h	DATA BUFF REGISTER 0	R	DBR0	undefined
3D h	DATA BUFF REGISTER 1	R	DBR1	undefined
3E h	DATA BUFF REGISTER 2	R	DBR2	undefined
3F h	DATA BUFF REGISTER 3	R	DBR3	undefined

Note1> '-' is reserved bit , it must be read to "0".
Note2> 'ABR3' must be initialized before using ABR (LDW @ABR, BR @ABR, CALL @ABR).

3. I/O Ports

The ADAM46P20XX has 12 I/O ports which are PA (4 I/O), PB (4 I/O), PD (4 I/O).
PA and PB Port have Stop Release selection register.
Pull-up resistor of PA, PB and PD ports can be selectable by program.
Pull-down resistor of PA ports can be selectable by program.
PA, PB and PD ports contains data direction register which controls I/O and data register which stores port data.
PA, PB and PD Ports have Open Drain selection register and Data register.

*PB1 is Open Drain output only.

I/O Ports Registers

Port	Data Reg.	Pull-up Reg.	Open-Drain Reg.	Direction Reg.	Stop Release Reg.	Function Reg.	Pull-down Reg.
port PA	PADR	PAPU	PAOD	PADD	PAST	PAFN	PAPD
port PB	PBDR	PBPU	PBOD	PBDD	PBST	PBFN	-
port PD	PDDR	PDPU	PDOD	PDDD	-	-	-

R/W	R/W	W	W	R/W	W	W	W
Initial value	1111	1111	1111	0000	1111	0000	0000
default	fh	disable	disable	input	disable	I/O ports	disable

3. I/O Ports

3.1. Port PA

Pin Name	Port Selection	Function Selection
PA0/KSA0	PA0 (I/O)	KSA0 Input
PA1/KSA1	PA1 (I/O)	KSA1 Input
PA2/KSA2/INT0(EC0)	PA2 (I/O)	KSA2 Input/ External Interrupt Input/ Event counter input
PA3/KSA3	PA3 (I/O)	KSA3 Input

3.1.1. PA Data Register (PADR)

bit	3	2	1	0	
PADR	PADR3	PADR2	PADR1	PADR0	00h
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

PA data register (PADR) is 4-bit register to store data of port PA.
When set as the output state by PADD, and data is written in PADR, data is outputted into PA pin.
When set as the input state, input state of pin is read. The initial value of PADR is "Fh" in reset state.
At output state, if port PA is read, PA Data Register (PADR) is read instead of port PA.

3.1.2. PA Pull-up Resistor Control Register (PAPU)

bit	3	2	1	0	
PAPU	PAPU3	PAPU2	PAPU1	PAPU0	01h
Initial value	1	1	1	1	
R/W	W	W	W	W	

PA pull-up resistor control register (PAPU) is 4-bit register and can control pull-up on or off each bit, if corresponding port is selected as input. If PAPU is selected as "0", pull-up is enabled and if selected as "1", it is disabled. PAPC is write-only register and initialized as "Fh" in reset state. The pull-up is automatically disabled, if corresponding port is selected as output.

3.1.3. PA Open Drain Assign Register (PAOD)

bit	3	2	1	0	
PAOD	PAOD3	PAOD2	PAOD1	PAOD0	02h
Initial value	1	1	1	1	
R/W	W	W	W	W	

PA Open Drain Assign Register (PAOD) is 4-bit register, and can assign PA port as open drain output port each bit If PAOD is selected as "0", port PA is open drain output, and if selected as "1", it is push-pull output. PAOD is write-only register and initialized as "Fh" in reset state.

3.1.4. PA I/O Data Direction Register (PADD)

bit	3	2	1	0	
PADD	PADD3	PADD2	PADD1	PADD0	03h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

PA I/O Data Direction Register (PADD) is 4-bit register, and can assign input state or output state to each bit. If PADD is "0", port PA is in the input state, and if "1", it is in the output state. Since PADD is initialized as "0h" in reset state, the whole port PA becomes input state.

3.1.5. PA Stop Release Selection Register (PAST)

bit	3	2	1	0	
PAST	PAST3	PAST2	PAST1	PAST0	04h
Initial value	1	1	1	1	
R/W	W	W	W	W	

PA Stop Release Selection Register (PAST) is 4-bit register, and can assign stop release pin or not. If PAST is selected as "0", stop release function is enabled and if selected as "1", it is disabled. PAST is write-only register and initialized as "Fh" in reset state. The Stop Release function is automatically disabled, if corresponding port is selected as output.

3.1.6. PA Function Selection Register (PAFN)

bit	3	2	1	0	
PAFN	-	PAFN2	-	-	05h
Initial value	-	0	-	-	
R/W	W	W	W	W	

Selection Mode of PAFN

Bit Name	Selection Mode		Remarks
–	–	–	
PAFN2	0	I/O	
	1	Interrupt & Event count Selection	INT0(EC0)
–	–	–	
–	–	–	

3.1.7. PA Pull-Down Resistor Selection Register (PAPD)

bit	3	2	1	0	
PAPD	PAPD3	PAPD2	PAPD1	PAPD0	06h
Initial value	0	0	0	0	
R/W	W	W	W	W	

PA pull-down resistor control register (PAPD) is 4-bit register and can control pull-down on or off each bit. If PAPD is selected as "1", pull-down is enabled and if selected as "0", it is disabled. PAPD is write-only register and initialized as "0h" in reset state.

3.2. Port PB

Pin Name	Port Selection	Function Selection
PB0/PWM0/KSB0	PB0 (I/O)	PWM0 Output / KSB0 Input
PB1/RESETB/KSB1	PB1 (I/O)	RESETB Input / KSB1 Input
PB2/CLO/KSB2	PB2 (I/O)	CLO Output / KSB2 Input
PB3/KSB3	PB3 (I/O)	KSB3 Input

3.2.1. PB Data Register (PBDR)

bit	3	2	1	0	
PBDR	PBDR3	PBDR2	PBDR1	PBDR0	08h
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

PB data register (PBDR) is 4-bit register to store data of port PB.
When set as the output state by PBDD, and data is written in PBDR, data is outputted into PB pin.
When set as the input state, input state of pin is read. The initial value of PBDR is "Fh" in reset state.
At output state, if port PB is read, PB Data Register (PBDR) is read instead of port PB.

3.2.2. PB Pull-up Resistor Control Register (PBPU)

bit	3	2	1	0	
PBPU	PBPU3	PBPU2	PBPU1	PBPU0	09h
Initial value	1	1	1	1	
R/W	W	W	W	W	

PB pull-up resistor control register (PBPU) is 4-bit register and can control pull-up on or off each bit, if corresponding port is selected as input. If PBPU is selected as "0", pull-up is enabled and if selected as "1", it is disabled. PBPU is write-only register and initialized as "Fh" in reset state. The pull-up is automatically disabled, if corresponding port is selected as output.

3.2.3. PB Open Drain Assign Register (PBOD)

bit	3	2	1	0	
PBOD	PBOD3	PBOD2	PBOD1	PBOD	0Ah
Initial value	1	1	1	1	
R/W	W	W	W	W	

PB Open Drain Assign Register (PBOD) is 4-bit register, and can assign PB port as open drain output port each bit If PBOD is selected as "0", port PB is open drain output, and if selected as "1", it is push-pull output. PBOD is write-only register and initialized as "Fh" in reset state.

3.2.4. PB I/O Data Direction Register (PBDD)

bit	3	2	1	0	
PBDD	PBDD3	PBDD2	PBDD1	PBDD0	0Bh
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

PB I/O Data Direction Register (PBDD) is 4-bit register, and can assign input state or output state to each bit. If PBDD is "0", port PB is in the input state, and if "1", it is in the output state. Since PBDD is initialized as "0h" in reset state, the whole port PB becomes input state.

3.2.5. PB Stop Release Selection Register (PBST)

bit	3	2	1	0	
PBST	PBST3	PBST2	PBST1	PBST0	0Ch
Initial value	1	1	1	1	
R/W	W	W	W	W	

PB Stop Release Selection Register (PBST) is 4-bit register, and can assign stop release pin or not.
If PBST is selected as "0", stop release function is enabled and if selected as "1", it is disabled. PBST is write-only register and initialized as "Fh" in reset state. The Stop Release function is automatically disabled, if corresponding port is selected as output.

3.2.6. PB Function Selection Register (PBFN)

bit	3	2	1	0	
PBFN	-	PBFN2	-	PBFN0	0Dh
Initial value	-	0	-	0	
R/W	W	W	W	W	

Selection Mode of PBFN

Bit Name	Selection Mode		Remarks
–	–	–	
PBFN2	0	I/O	
	1	CLO(fosc) Output Selection	CLO
–	–	–	
PBFN0	0	I/O	
	1	PWM0 (Timer0) Output Selection	PWM0

3.3. Port PD

Pin Name	Port Selection	Function Selection
PD0	PD0 (I/O)	–
PD1	PD1 (I/O)	–
PD2	PD2 (I/O)	–
PD3	PD3 (I/O)	–

3.3.1. PD Data Register (PDDR)

bit	3	2	1	0	
PDDR	PDDR3	PDDR2	PDDR1	PDDR0	10h
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

PD data register (PDDR) is 4-bit register to store data of port PD.
When set as the output state by PDDD, and data is written in PDDR, data is outputted into PD pin.
When set as the input state, input state of pin is read. The initial value of PDDR is "Fh" in reset state.
At output state, if port PD is read, PD Data Register (PDDR) is read instead of port PD.

3.3.2. PD Pull-up Resistor Control Register (PDPU)

bit	3	2	1	0	
PDPU	PDPU3	PDPU2	PDPU1	PDPU0	11h
Initial value	1	1	1	1	
R/W	W	W	W	W	

PD pull-up resistor control register (PDPU) is 4-bit register and can control pull-up on or off each bit, if corresponding port is selected as input. If PDPU is selected as "0", pull-up is enabled and if selected as "1", it is disabled. PDPU is write-only register and initialized as "Fh" in reset state. The pull-up is automatically disabled, if corresponding port is selected as output.

3.3.3. PD Open Drain Assign Register (PDOD)

bit	3	2	1	0	
PDOD	PDOD3	PDOD2	PDOD1	PDOD0	18h
Initial value	1	1	1	1	
R/W	W	W	W	W	

PD Open Drain Assign Register (PDOD) is 4-bit register, and can assign PD port as open drain output port each bit If PDOD is selected as "0", port PD is open drain output, and if selected as "1", it is push-pull output. PDOD is write-only register and initialized as "Fh" in reset state.

3.3.4. PD I/O Data Direction Register (PDDD)

bit	3	2	1	0	
PDDD	PDDD3	PDDD2	PDDD1	PDDD0	19h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

PD I/O Data Direction Register (PDDD) is 4-bit register, and can assign input state or output state to each bit. If PDDD is "0", port PD is in the input state, and if "1", it is in the output state. Since PDDD is initialized as "0h" in reset state, the whole port PD becomes input state.

4. Oscillation Circuit

4.1. Oscillation Circuit

Clock from oscillation circuit makes CPU clock via clock pulse generator, and then provide peripheral hardware clock.

There is 1 type of Oscillation circuit and it can be divided in 6 different oscillator option modes. The user can used OTP Configuration Option Bits (OSCS2 through OSCS0) to select one of these 6 types. Refer to Table 4.1.

• IRC : Internal RC Oscillator (6 modes)

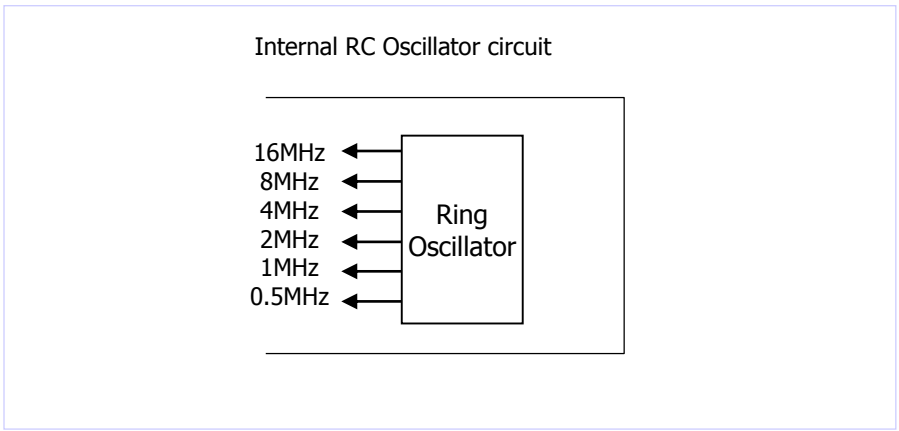


Fig.4.1 Oscillator configurations

It is Internal RC Oscillator circuit. The Internal Oscillator is calibrated by calibration option bits.
In STOP mode, Internal RC oscillator is stopped.

Below table shows the selection of the oscillator type by OTP Configuration Option Bits (Address 8000h, OSCS2 ~ OSCS0). (Refer to 13.2. Configuration Option Bit Description)

Table. 4.1 Oscillator Type and Modes Selection

OSCS[2:0]			Oscillator Modes
OSCS[2]	OSCS[1]	OSCS[0]	
1	1	1	Internal RC 4MHz
1	1	0	Internal RC 8MHz
1	0	1	Internal RC 16MHz
1	0	0	Internal RC 1MHz
0	1	1	Internal RC 0.5MHz
0	1	0	Internal RC 2MHz
0	0	1	*Setting is prohibited*
0	0	0	

5.1. Watch Dog Timer (WDT)

Watch dog timer is organized binary of 19 steps. The signal of $f_{OSC}/4$ cycle comes in the first step of WDT after WDT reset. If this counter was overflowed, reset signal automatically come out so that internal circuit is initialized. The overflow time is initially $2^{18} \times 4/f_{OSC}$ (262.144ms at f_{OSC} = 4.0MHz), it is selectable by WDT Control Register (WDTCR). Normally, the binary counter must be reset before the overflow by using reset instruction (WDTC), Power-on reset pulse or Low VDD detection pulse. It is constantly reset in STOP mode. When STOP is released, counting is restarted.

If it's executed the STOP instruction after setting the bit RWDTEN of WDTCR to "1", the Internal RC-Ring Oscillated Watch-dog Timer (RCWDT) mode is activated.

5.1.1. WDT Control Register

bit	3	2	1	0	
WDTCR	WDTRST	RWDTEN	WDTCK1	WDTCK0	*37h*
Initial value	1	0	0	0	
R/W	W	W	W	W	

WDTRST	0	WDT interrupt enable, when WDT Overflow is occurred.
	1	System Reset enable, when WDT Overflow is occurred. (default)
RWDTEN	0	RCWDT mode disable (Tck = fosc/4)
	1	RCWDT Oscillator Enable & RCWDT mode enable
WDTCK1 & WDTCK0	00	WDT Overflow Time is 2^{18} x Tck
	01	WDT Overflow Time is 2^{17} x Tck
	10	WDT Overflow Time is 2^{16} x Tck
	11	WDT Overflow Time is 2^{15} x Tck

Reset or Interrupt Wakeup Time (Example)

	Tck * 2^{18}	Tck * 2^{17}	Tck * 2^{16}	Tck * 2^{15}	Unit
Tck = 1us	262.144	131.072	65.536	32.768	ms
Tck = 16us	4,194.304	2,097.152	1,048.076	524.288	

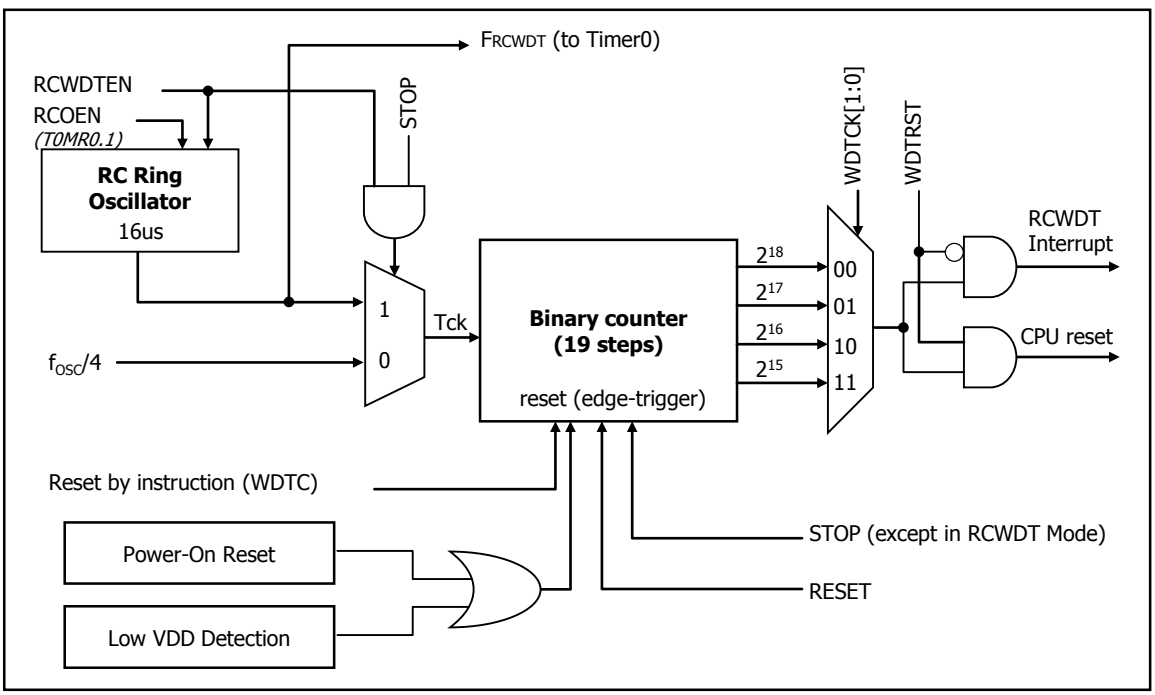


Fig.5.1 Block Diagram of Watch-dog Timer

6.1. Timer

6.1.1. Timer operation mode

Timer is basically made of Timer Data Register, Timer Mode Register and control circuit. The type of Timer is 8bit binary counter Timer0 (T0).

Timer0 Data Register consists of Timer0 Data 0 High Register (T0D0H), Timer0 Data 0 Low Register (T0D0L), Timer0 Data 1 High Register (T0D1H) and Timer0 Data 1 Low Register (T0D1L).

Timer0	-. 8-bit Interval Timer -. 8-bit Event Counter -. 8-bit Capture Timer -. 8-bit rectangular-wave output

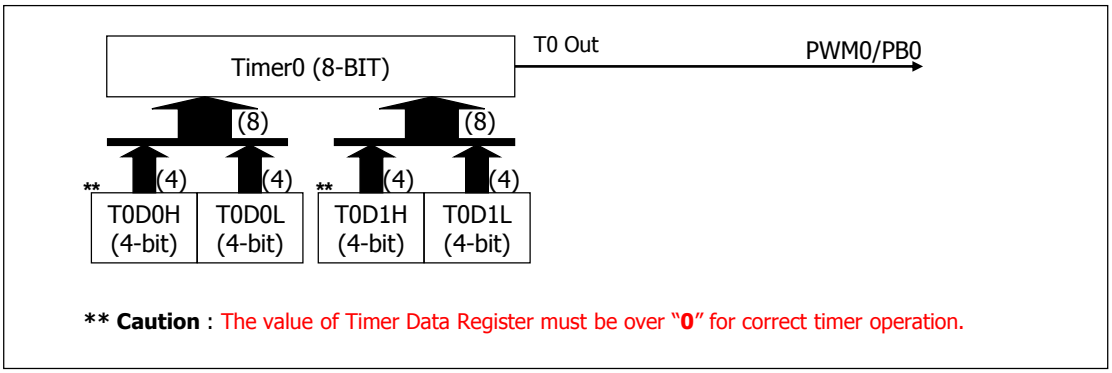
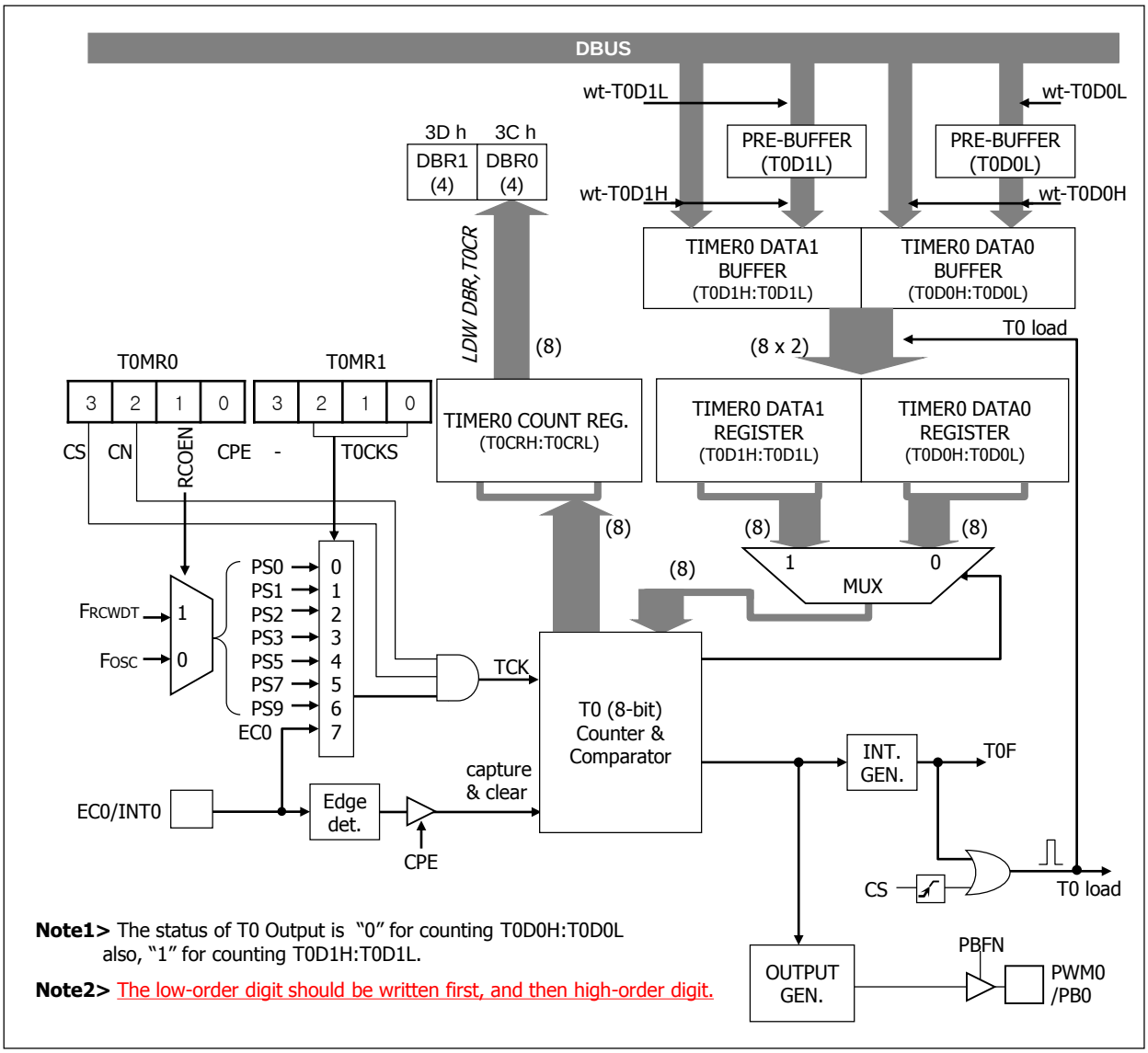


Fig. 6.1 Timer/Counter Block diagram (8-Bit Mode)

6.2. Timer0

6.2.1. Timer0(T0) Block Diagram



Note1> The status of T0 Output is "0" for counting T0D0H:T0D0L also, "1" for counting T0D1H:T0D1L.

Note2> The low-order digit should be written first, and then high-order digit.

6.2.2. Timer0 Control Register

• Timer0 Mode Register 0 (T0MR0)

	3	2	1	0	
T0MR0	T0CS	T0CN	RCOEN	T0CPE	20h
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of T0MR0

Bit Name			Selection Mode	Remarks
T0CS	Timer0 Clear / start Control	0	Timer0 Stop	
		1	Timer0 Clear and Start	
T0CN	Timer0 Pause / Continue Control	0	Timer0 Pause	
		1	Timer0 continue	
RCOEN	Input Clock Source selection	0	System clock (Fosc)	
		1	RCWDT clock (FRCWDT=Typ. 64kHz)	
T0CPE	Input capture Mode selection	0	Timer/Counter Mode	
		1	Capture Mode	

Note: Timer 0 only counts with 'T0D0H+T0D0L' and can occur the interrupt in every counter overflow, if timer0 operates at 8-bit Capture mode.

• Timer0 Mode Register 1 (T0MR1)

	3	2	1	0	
T0MR0	–	T0CK2	T0CK1	T0CK0	21h
initial value	–	0	0	0	
R/W	W	W	W	W	

Selection Mode of T0MR1

Bit Name			Selection Mode		Remarks
–	–	–	–		
T0CK2 T0CK1 T0CK0	Input clock selection		RCOEN = 0	RCOEN=1	
		000	*PS0 (=Fosc/2^0)	FRCWDT/2^0	
		001	PS1 (=Fosc/2^1)	FRCWDT/2^1	
		010	PS2 (=Fosc/2^2)	FRCWDT/2^2	
		011	PS3 (=Fosc/2^3)	FRCWDT/2^3	
		100	PS5 (=Fosc/2^5)	FRCWDT/2^5	
		101	PS7 (=Fosc/2^7)	FRCWDT/2^7	
		110	PS9 (=Fosc/2^9)	FRCWDT/2^9	
		111	EC0		

Caution : PS0 must be used only in the case of fosc ≤ 8MHz.

• Timer0 Data0 Register Low (T0D0L)

	3	2	1	0	
T0D0L	T0D0L3	T0D0L2	T0D0L1	T0D0L0	22h
initial value	–	–	–	–	
R/W	W	W	W	W	

• Timer0 Count Register Low (T0CRL)

	3	2	1	0	
T0CRL	T0CRL3	T0CRL2	T0CRL1	T0CRL0	22h
initial value	–	–	–	–	
R/W	R	R	R	R	

• Timer0 Data0 Register High (T0D0H)

	3	2	1	0	
T0D0H	T0D0H3	T0D0H2	T0D0H1	T0D0H0	23h
initial value	–	–	–	–	
R/W	W	W	W	W	

• Timer0 Count Register High (T0CRH)

	3	2	1	0	
T0CRH	T0CRH3	T0CRH2	T0CRH1	T0CRH0	23h
initial value	–	–	–	–	
R/W	R	R	R	R	

Note: The T0D0x, T0CRx(Timer0 Count Reg.) and T0CPx(Timer0 Capture Reg.) are in same address.
In the capture mode, reading operation is read the T0CPx, not T0CRx because path is opened to the T0CPx, and T0D0x is only for writing operation.

• Timer0 Data1 Register Low (T0D1L)

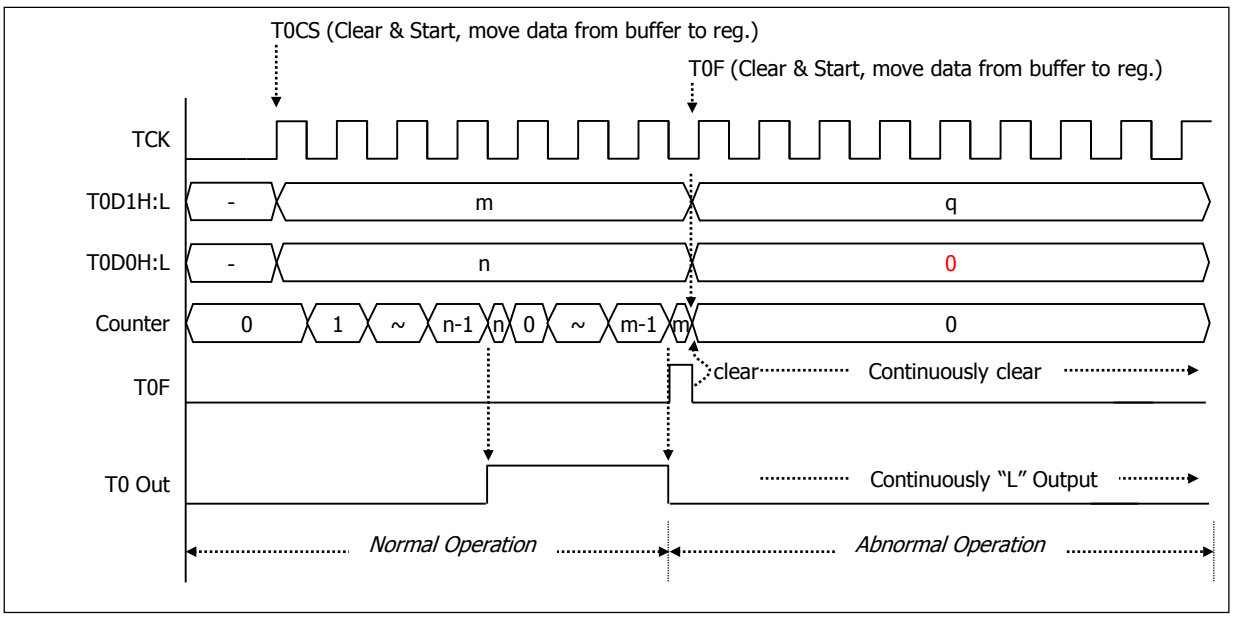
	3	2	1	0	
T0D1L	T0D1L3	T0D1L2	T0D1L1	T0D1L0	24h
initial value	–	–	–	–	
R/W	W	W	W	W	

• Timer0 Data1 Register High (T0D1H)

	3	2	1	0	
T0D1H	T0D1H3	T0D1H2	T0D1H1	T0D1H0	25h
initial value	–	–	–	–	
R/W	W	W	W	W	

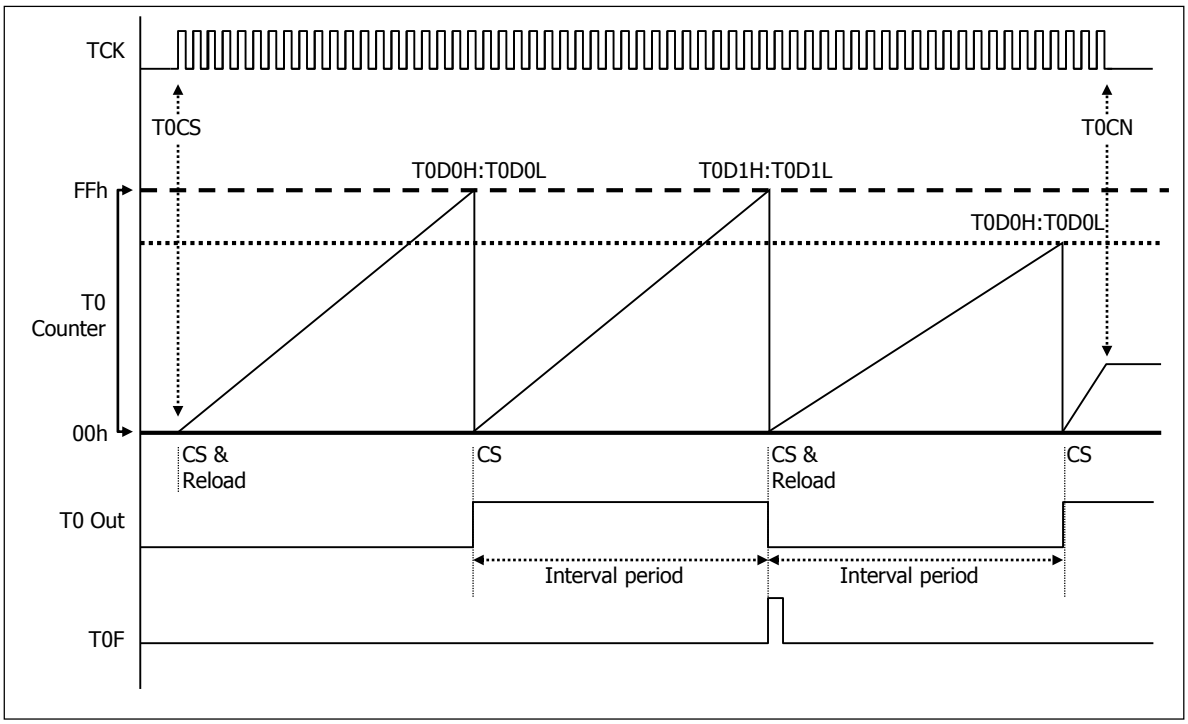
6.2.3. Timer0 Caution

The value of Timer Data Register must be over "**0**" for correct timer operation.



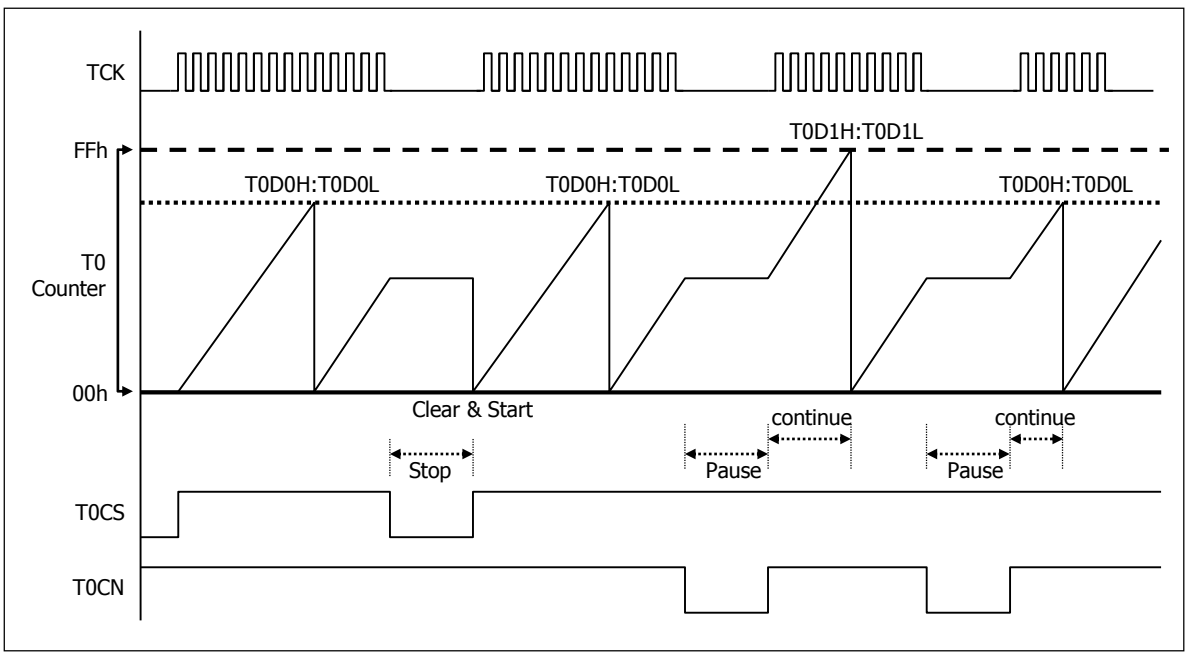
6.2.4. Timer0 Timing Diagram

* 8-bit Timer/Counter mode Timing Diagram

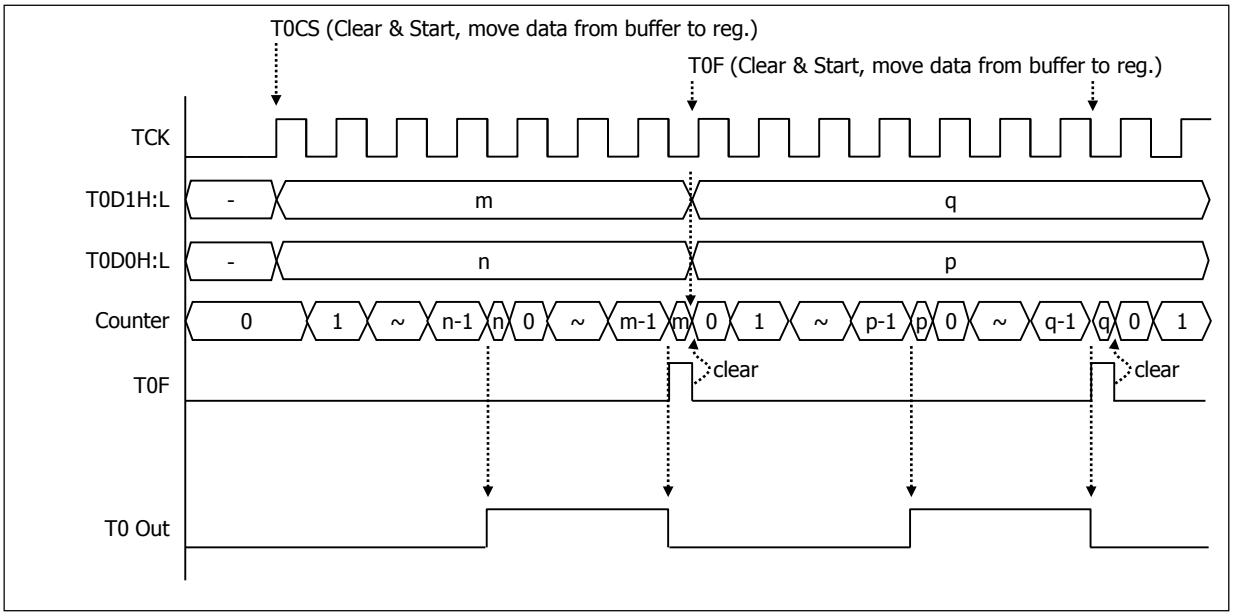


Note > CS : Timer0 Counter Clear & Start.
Reload : Timer0 Data move from Data buffer to Data register.

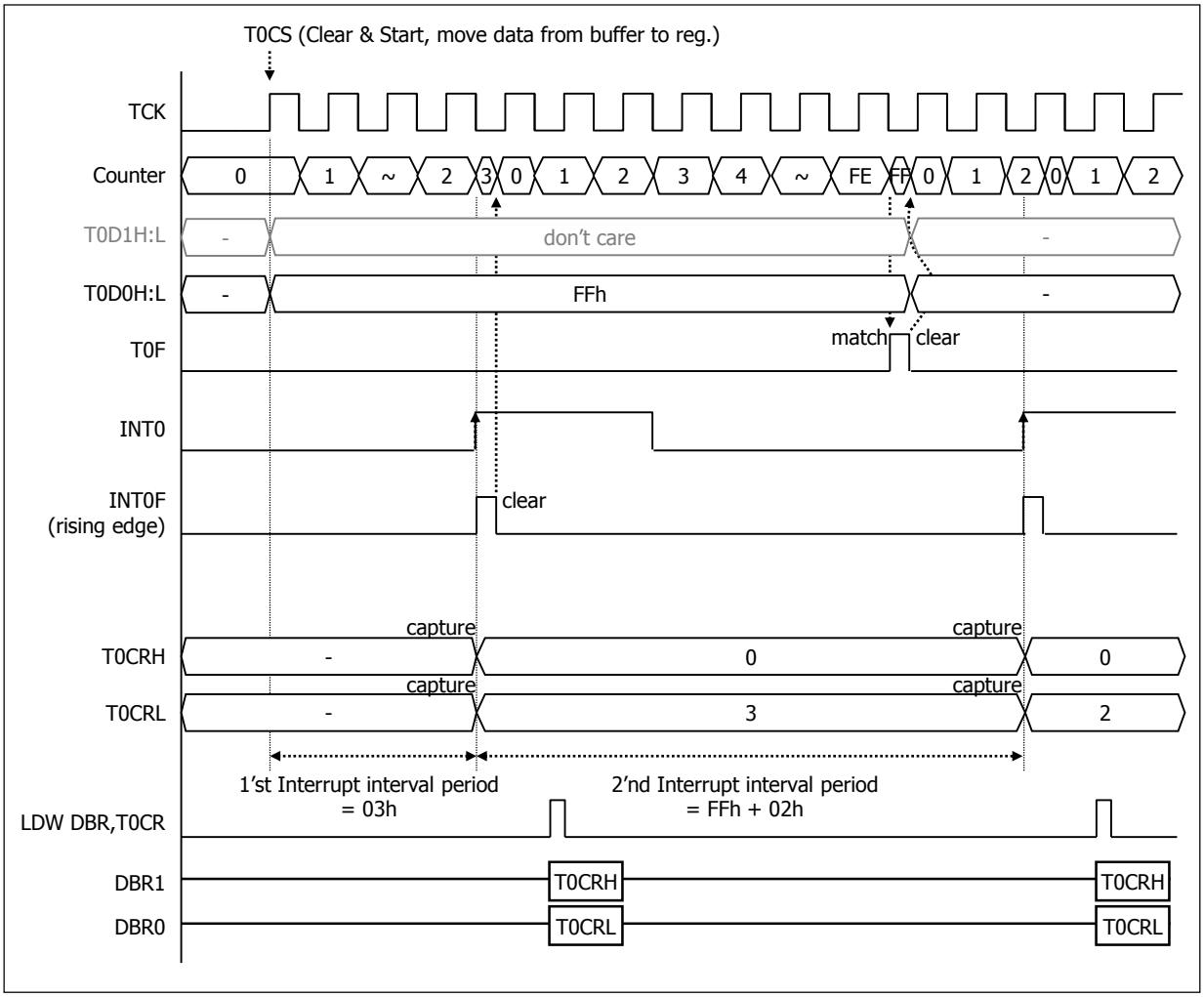
* Start / Stop operation



* 8-bit Timer/Counter mode Timing Diagram



* 8-bit Capture mode Timing Diagram



* 8-bit PWM mode

Timer0 make the PWM (Pulse Width Modulation) functions without additional mode setting, because they have the Data L Registers(T0D0H+T0D0L) and the Data H Registers(T0D1H+T0D1L). The low pulse width of the PWM output determined by the Data L Registers, and the high pulse width of the PWM output determined by the Data H Registers. The period of the PWM output is the sum of the Data L Registers value and the Data H Registers value.

PWM Period = Low pulse width + High pulse width

	Timer0
Low pulse width	(T0D0H,T0D0L) x Source Clock
High pulse width	(T0D1H,T0D1L) x Source Clock

When main frequency is 4MHz, maximum PWM frequency is shown as below Table.

freq = 4MHz

Source Clock	**Pulse Width Range**		**Duty ratio**	**Max. PWM Frequency**
	Low	**High**		
PS0 (000) : 0.25us	01h ~ FFh	01h ~ FFh	1/256 ~ 255/256	15.6250 kHz
PS1 (001) : 0.5us	↑	↑	↑	7.8125 kHz
PS2 (010) : 1.0us	↑	↑	↑	3.9063 kHz
PS3 (011) : 2.0us	↑	↑	↑	1.9531 kHz
PS5 (100) : 8.0us	↑	↑	↑	0.4883 kHz
PS7 (101) : 32.0us	↑	↑	↑	0.1220 kHz
PS9 (110) : 128.0us	↑	↑	↑	0.0305 kHz
EC0 (111)	↑	↑	↑	depends on EC0

The ADAM46P20XX contains 4 interrupt sources; 1 externals and 3 internals.
Nested interrupt services with priority control is also possible.

- 4 interrupt source (1Ext, 1Timer, 1VDI, 1WDT)
- 4 interrupt vector
- 4 level nested interrupt control is possible.
- Read of interrupt request flag are possible.
- In interrupt accept, request flag is automatically cleared.

Interrupt Enable Register (IENR0), Interrupt Request Register (IRQR0) and priority circuit.
Interrupt function block diagram is shown in Fig. 7.1

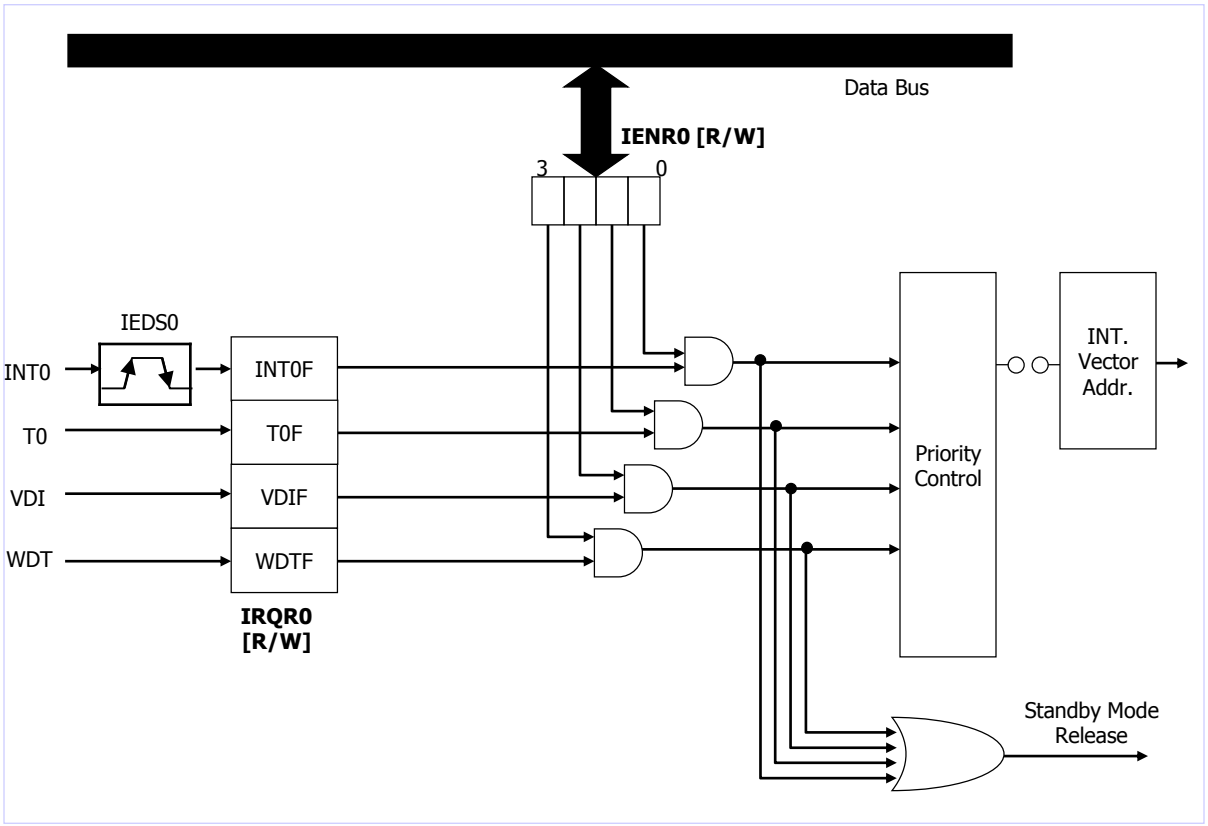


Fig. 7.1 Interrupt Source

7. Interrupt

7.1. Interrupt Source

Each interrupt vector is independent and has its own priority.

	Mask	Priority	Interrupt Source	INT Vector Addr.
Hardware Interrupt	Non-maskable	-	RESET	0000h
	maskable	1	INT0 (External Interrupt 0)	0002h
		2	T0 (Timer0)	0004h
		3	VDI (Voltage Detection Indicator)	0006h
		4	WDT (Watch-Dog Timer)	0008h

Table 7.1 Interrupt Source

7.2. Interrupt Control Register

I flag of SFR is a interrupt mask enable flag. When I flag = ``0``, all interrupts become disable.
When I flag = ``1``, interrupts can be selectively enabled and disabled by contents of corresponding Interrupt Enable Register(IENR0).
When interrupt is occurred, interrupt request flag is set,and Interrupt request is detected at the edge of interrupt signal. The accepted interrupt request flag is automatically cleared during interrupt cycle process. The interrupt request flag maintains ``1`` until the interrupt is accepted or is cleared in program. In reset state, interrupt request flag register (IRQR0) is cleared to ``0``.
It is possible to read the state of interrupt register and to manipulate the contents of register.

- External Interrupt Edge selection Register 0 (IEDS0)

	3	2	1	0	
IEDS0	-	-	IED0H	IED0L	16h
initial value	-	-	0	0	
R/W	W	W	W	W	

Bit Name	Selection Mode		Remarks
-	-	-	
-	-	-	
IED0H IED0L	00	-	INT0
	01	Falling Edge Selection (1-to-0 transition)	
	10	Rising Edge Selection (0-to-1 transition)	
	11	Both Edge Selection (Falling & Rising)	

• Interrupt Enable Register 0 (IENR0)

	3	2	1	0	
IENR0	WDTE	VDIE	T0E	INT0E	1Eh
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of IENR0

Bit Name	Selection Mode		Remarks
WDTE	1	WDT Timer overflow Interrupt enable	
VDIE	1	Voltage Detection Interrupt enable	
T0E	1	Timer0 Interrupt enable	
INT0E	1	External Interrupt 0 enable	

• Interrupt Request Flag Register (IRQR0)

	3	2	1	0	
IRQR0	WDTF	VDIF	T0F	INT0F	1Ch
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of IRQR0

Bit Name	Selection Mode		Remarks
WDTF	1	WDT Timer overflow Interrupt Flag enable	
VDIF	1	Voltage Detection Interrupt Flag enable	
T0F	1	Timer0 Interrupt Request Flag enable	
INT0F	1	External Interrupt 0 Request Flag enable	

7.3. Interrupt Timing

Interrupt Request Sampling Time :
-. Maximum 2 machine cycle (When execute LDW @ABR Instruction)
-. Minimum 0 machine cycle

Interrupt preprocess step is 1 machine cycle

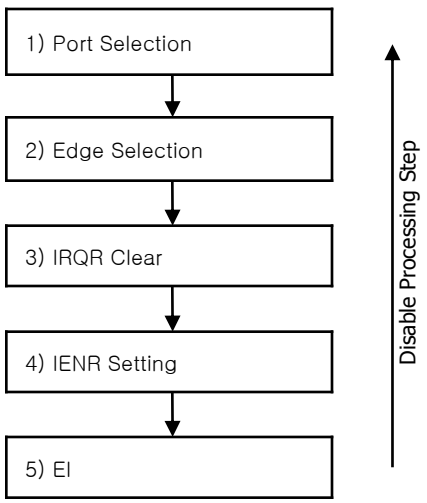
7.4. The valid timing after executing Interrupt control instructions

I flag is valid just after executing of EI/DI on the contrary.

7.5. Multiple Interrupt

If there is an interrupt, Interrupt Mask Enable Flag is automatically cleared before entering the Interrupt Service Routine. After then, no interrupt is accepted. If EI instruction is executed, interrupt mask enable bit becomes "1", and each enable bit can accept interrupt request.
When two or more interrupts are generated simultaneously, the highest priority interrupt is accepted.

External Interrupt Enable Processing Step



7.6. Interrupt Processing Sequence

When an interrupt is accepted, the on-going process is stopped and the interrupt service routine is executed. After the interrupt service routine is completed it is necessary to restore everything to the state before the interrupt occurred.
As soon as an interrupt is accepted, the content of the program counter is saved in the stack register which is 5 level stack area, and the contents of status flag register (SFR) is saved on the interrupt stack register (INTSK) which is 4 level stack area.
At the same time, the content of the vector address corresponding to the accepted interrupt, which is in the interrupt vector table, enters into the program counter and interrupt service is executed. In order to execute the interrupt service routine, it is necessary to write the jump addresses in the vector table corresponding to each interrupt.

Interrupt Processing Step

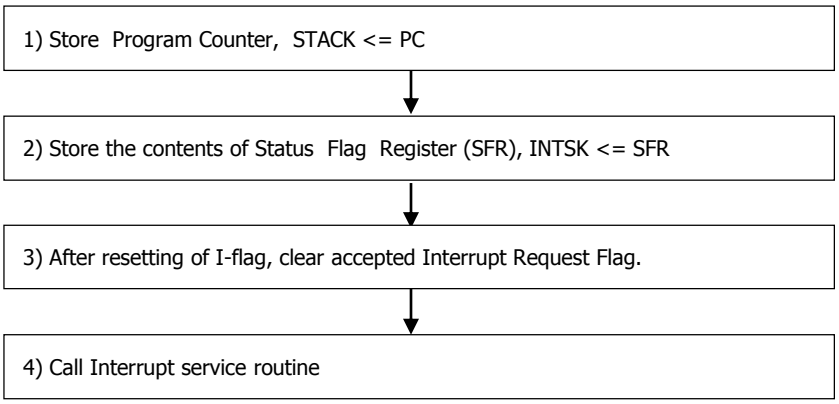
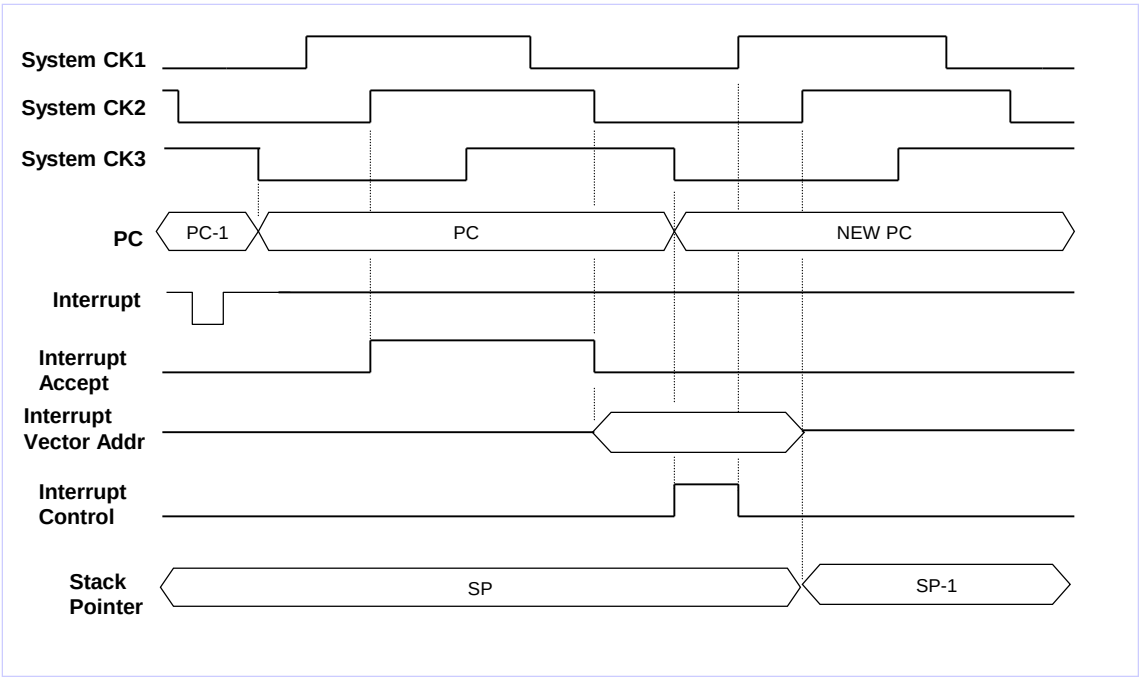


Fig. Interrupt Processing Step Timing



8. POWER-DOWN FUNCTION

In power-down mode, power consumption is reduced considerably that in battery operation battery life time can be extended a lot. For applications where power consumption is a critical factor, ADAM46P20XX provides two kinds of power-down functions, STOP mode and RCWDT mode. In this 2 Modes, program processing is stopped.

8.1. Stop Mode

STOP mode can be entered by STOP instruction during program.
In STOP mode, oscillator is stopped to make all clocks stop, which leads to less power consumption. All registers and RAM data are preserved.
"NOP" instruction should be follows STOP instruction for pre-charge time of Data Bus line.

```
ex)  STOP : STOP instruction execution
     NOP  : NOP instruction
```

8.1.1. Stop Mode Release

Release of STOP mode is executed by Power on reset , Key input Port(one of PA, PB) which is selected by PAST and PBST register for stop release is Low, external interrupt and Low voltage detection (LVD) mode release .
When there is a release signal of STOP mode, if the Bit1(SROPT) of SCTLR is "1", the instruction execution starts after no waiting time. But if the Bit1(SROPT) of SCTLR is "0",the instruction execution after stabilization oscillation time($2^{14} \times 4/fOSC$ = 16.384ms at fOSC = 4.0MHz). The Bit1(SROPT) is default "0".

Release Factor	Release Method	Release Time
Power on Reset	By Power on reset, Stop mode is release and system is initialized.	7.2ms + $57 \times 2^{10} \times 4/fosc$ = 65.6ms at fosc = 4.0MHz (Option read time : about 7.2ms)
Release from LVD detection	Stop mode is release when release from LVD detection.	
PA, PB port (key input)	Stop mode is released by low input of selected pin by PAST and PBST register.	1) if SROPT=0 (default) : $2^{14} \times 4/fosc$ = 16.384ms at fosc = 4.0MHz 2) if SROPT=1 : $4/fosc$ = 1us
External interrupt	Stop mode is released external interrupt input.	
Timer0 interrupt	Stop mode is released by interrupt of Timer0(T0). (only when RCOEN is selected)	
WDT Overflow	Stop mode is released by reset or interrupt of WDT. (in RCWDT Mode only)	
External Reset	Stop mode is released by external RESETB pin.	

8.2. RCWDT Mode

Additionally, if it's executed the STOP instruction after setting the bit RCWDTEN of WDTCR to "1", the Internal RC-Oscillated Watchdog Timer mode is activated. In the Internal RC-Oscillated Watchdog Timer mode, STOP mode is also released by occurring of WDT Time-out selected by WDTCK[1:0].

The Ring-OSC oscillation period is vary with temperature, VDD and process variations from part to part. According to the bit WDTCK of WDTCR, the RCWDT oscillated watchdog timer time-out is shown at Chapter 5. Watch Dog Timer.

"NOP" instruction should be follows STOP instruction for pre-charge time of Data Bus line.

```
ex)  LRI    WDTCR, #0100b   : set the bit of RCWDTEN
     WDTC                   : WDT clear
     STOP                   : STOP instruction execution
     NOP                    : NOP instruction
```

• System Control Register (SCTLR)

	3	2	1	0	
SCTLR	LVDOFF	–	SROPT	NFOPT	17h
initial value	0	–	0	0	
R/W	W	W	W	W	

Selection Mode of SCTLR

Bit Name	Selection Mode		Remarks
LVDOFF	0	LVD Enable	
	1	LVD Disable	
–	–	–	
SROPT	0	STOP Release Time is Long for oscillation stabilization. (2^{14}×4/fosc)	
	1	STOP Release Time is Short. (4/fosc)	
NFOPT	0	Oscillation Clock Input Noise Filtering time is short for High Frequency operation. (fosc > 12MHz)	
	1	Oscillation Clock Input Noise Filtering time is long for Low Frequency operation. (fosc < 12MHz)	

8.3. Operation States in Stop Mode

Internal Circuit	STOP Mode	RCWDT Mode
Oscillator	Stop	Stop
Internal CPU clock	Stop	Stop
Address Bus Data Bus	Retained	Retained
Registers	Retained	Retained
RAM	Retained	Retained
I/O port	Retained	Retained
Timer	Stop & Counter clear (only operate when RCOEN is selected)	Stop & Counter clear (only operate when RCOEN is selected)
Watch dog Timer	Stop	Operate
RCWDT	Stop	Operate continuously
VDI	Operates continuously	Operates continuously
Release Method	RESETB, Power-on-reset, Release from LVD, Ext. Interrupt, T0(RCOEN) interrupt, Key-input interrupt.	RESETB, Power-on-reset, Release from LVD, WDT(RCWDT), Ext. Interrupt, T0(RCOEN) interrupt, Key-input interrupt.

Table 8.1 Operation States in Stop Mode and RCWDT Mode

9. RESET FUNCTION

9.1. Internal Power On RESET

Power On Reset circuit automatically detects the rise of power voltage
(the rising time should be within 50ms). Until the power voltage reaches a certain voltage level, internal reset signal is maintained at ″L″ Level until oscillator is stable.
After power applies, this reset state is maintained for the configuration option reading time (about 7.2ms at VDD=5.0V) and the oscillation stabilization time. ($4/f_{OSC} \times 57 \times 2^{10}$ = about 58.368ms at 4MHz).

Fig. Block Diagram of Power On Reset Circuit

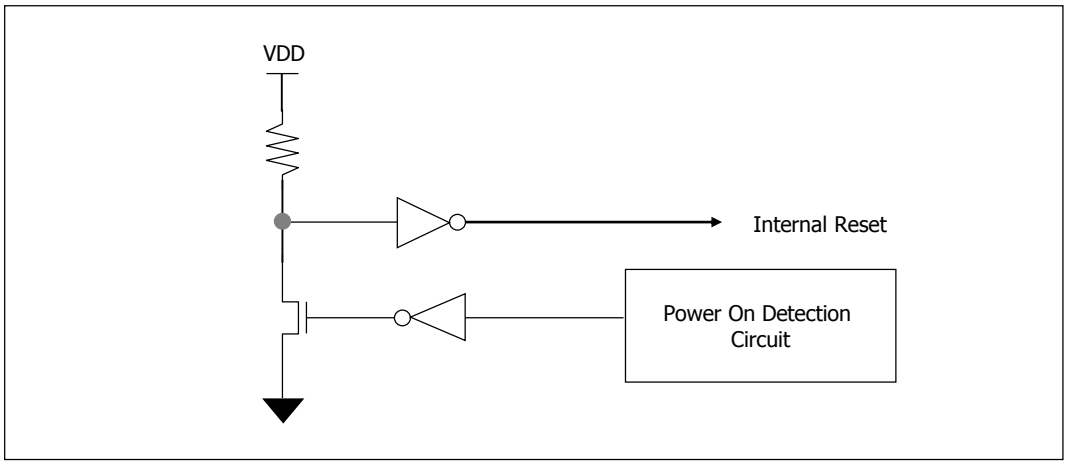
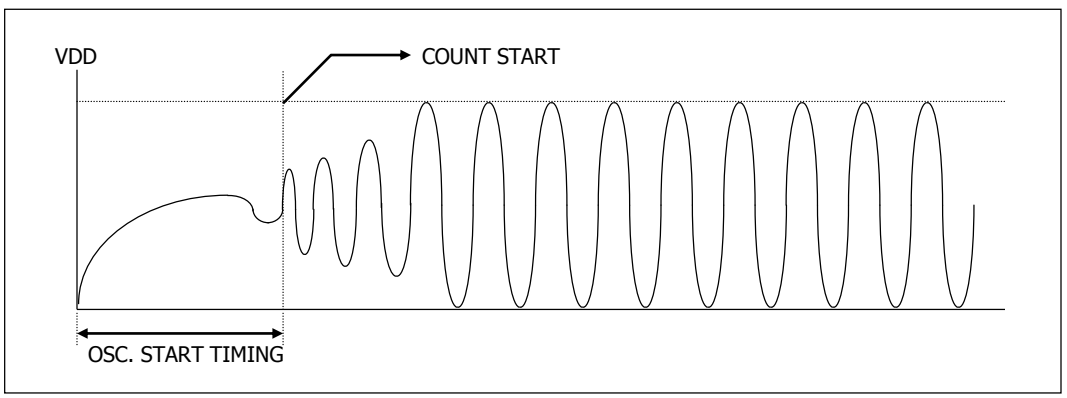


Fig. Oscillator stabilization diagram

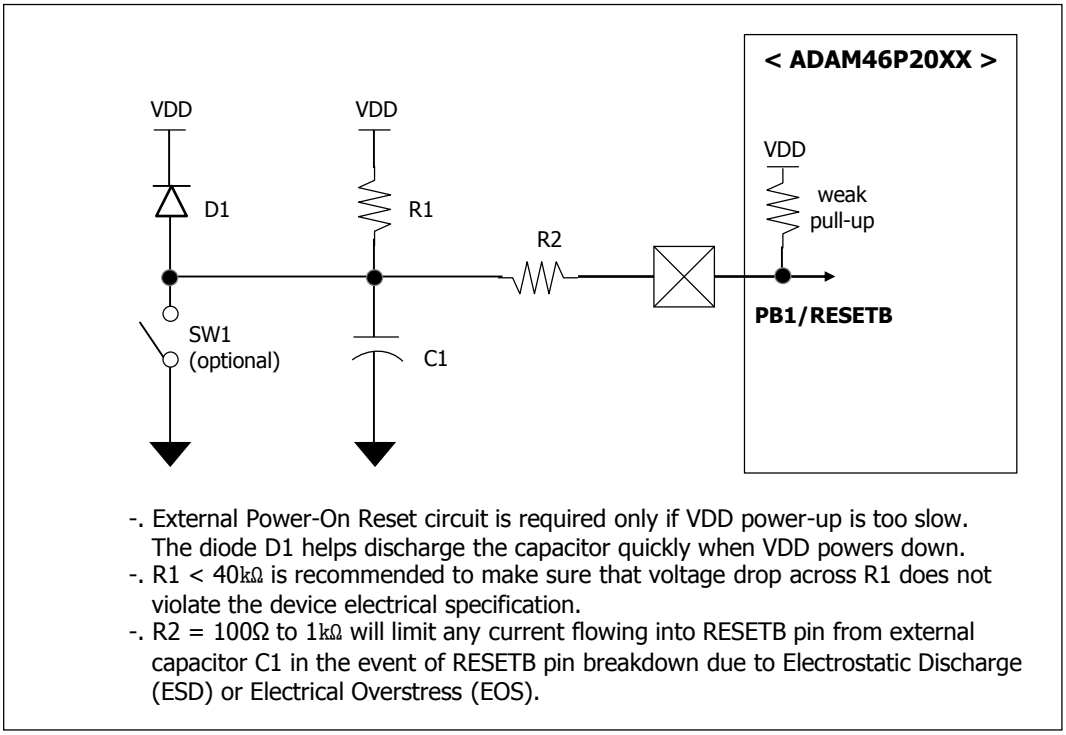


Note) When Power On Reset, oscillator stabilization time doesn't include OSC. Start time.

9.2. External Reset (RESETB)

The reset input is the RESETB pin, which is the input to a schmitt Trigger.
A reset in accomplished by holding the RESETB pin low for at least 8 oscillator periods, while the oscillator running.
An Internal RESETB option is enabled by setting the RSTS bit in the Configuration Option Bits (Refer to 13.2. Configuration Option Bit Description). When RSTS=0, the Reset signal to the chip is generated internally. When the RSTS=1, the PB1/RESETB pin becomes an external Reset input. In this mode, the PB1/RESETB pin has a weak pull-up to VDD internally.

Fig. Recommended RESETB Circuit



-. External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D1 helps discharge the capacitor quickly when VDD powers down.
-. R1 < 40㏀ is recommended to make sure that voltage drop across R1 does not violate the device electrical specification.
-. R2 = 100Ω to 1㏀ will limit any current flowing into RESETB pin from external capacitor C1 in the event of RESETB pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

10. Low Voltage Detection Mode

10.1. Low Voltage Detection Condition

An on board voltage comparator checks that V_{DD} is at the required level to ensure correct operation of the device.
If V_{DD} is below a certain level, Low voltage detector forces the device into low voltage detection mode.

10.2. Low Voltage Detection Mode

There is no power consumption except stop current.
1. STOP mode release function is disabled.
2. I/O port is configured as input mode (without pull-up and pull-down resistor).
3. Data memory is retained until voltage through external capacitor is worn out.
4. Interrupt disabled.
5. Oscillator is stop.

10.3. Release of Low Voltage Detection Mode

Reset signal result from new battery or any other power (normally 3V/5V) wakes the low voltage detection mode and come into normal reset state. It depends on user whether to execute RAM clear routine or not.

10.4. Low Voltage Detection voltage selection (option)

User can select the voltage of Low Voltage detection voltage level by OTP Configuration Bits (LVDS). One is high voltage version (typ. 2.2V, if LVDS is "0"),
another is low voltage version (typ. 1.8V, if LVDS is "1").

11. Voltage Detection Indicator Mode

11.1. Voltage Detection Indicator Register

Voltage Detection indicator (VDI) are controlled by two registers. It is useful to display the consumption of Batteries.

If VDD power level is low and higher than low voltage detection (LVD) level (refer to Fig 11.1), the bit of VDIR register could be set according to the VDD level sequentially.

The VDD detection levels for Indication are three , that is , VDIR1(Typ. 3.3V) and VDIR0 (Typ. 2.2V) of VDIR register.

11.1.1. Voltage Detection Indicator Enable Register (VDIER)

bit	3	2	1	0	
VDIER	VDIM	-	VDIER1	VDIER0	*33h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

VDIM	VDI Mode Selection	0	System Reset Selection
		1	Interrupt Selection
–	–	–	–
VDIER1	detection level 1 (typ. 3.3V) selection	0	disable
		1	enable
VDIER0	detection level 0 (typ. 2.2V) selection	0	disable
		1	enable

Voltage Detection Indicator Enable Register (VDIER) is 4-bit register, and can assign Indicator is enable or not.

If VDIER1 ~ VDIER0 is selected as "0", Voltage detection for Indication function is disabled and if selected as "1", it is enable. If VDIM is selected as "0" and enable one of VDIER1~VDIER0, when the corresponding voltage detection for Indication is occurred, it makes the system reset. If LVIM is selected as "1", it makes the VDI interrupt.

VDIER is write-only register and initialized as ``0 h`` in reset state.

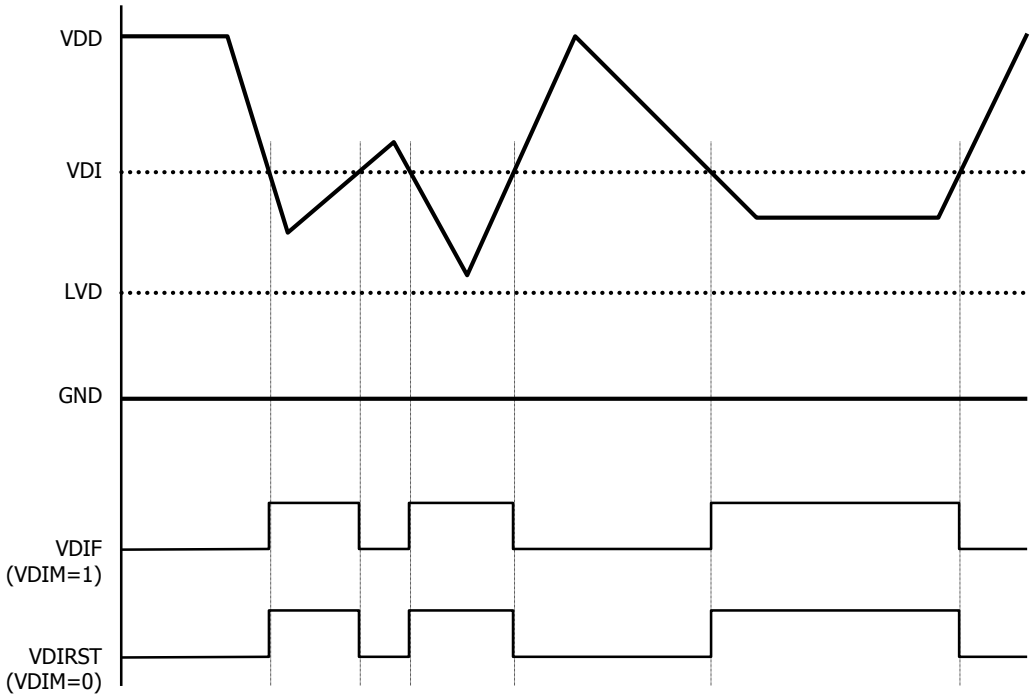
In the in-circuit emulator, VDI function is not implemented and user can not experiment with it. Therefore after final development of user program, this function may be experimented or evaluated.

11.1.2. Voltage Detection Indicator Data Register (VDIR)

bit	3	2	1	0	
VDIR	-	-	VDIR1	VDIR0	*33h*
Initial value	0	0	0	0	
R/W	R	R	R	R	

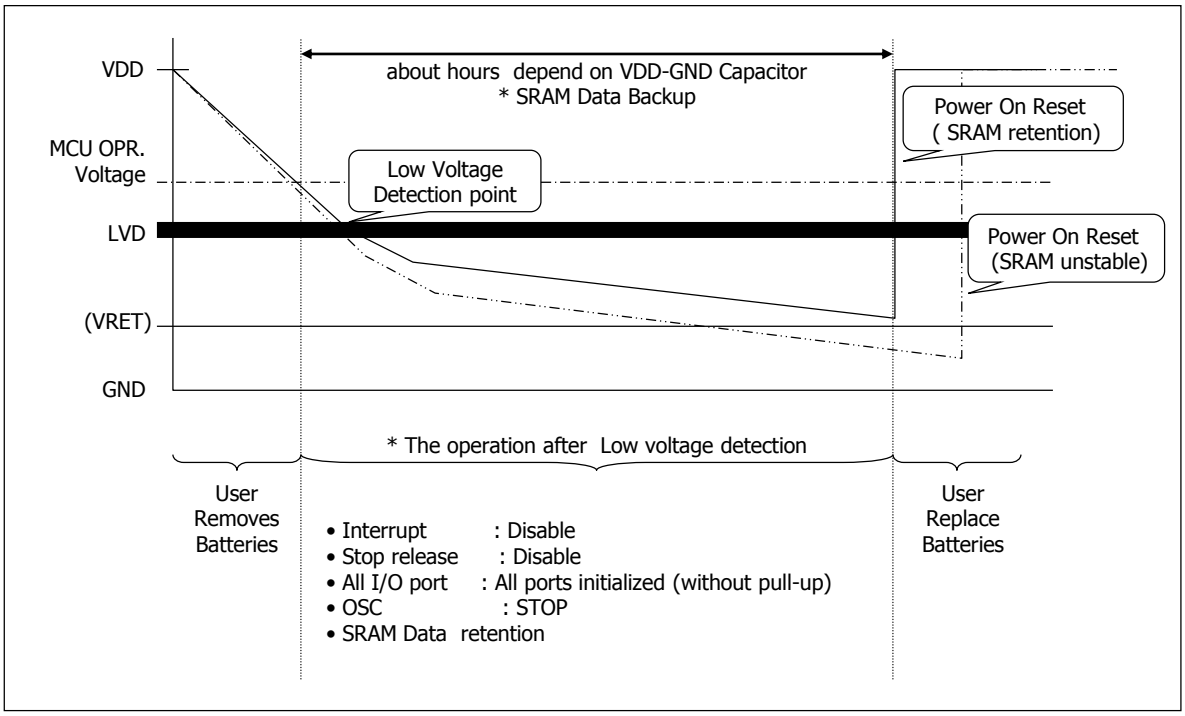
Voltage Detection Indicator Data Register (VDIR) is 2-bit register to store data of low voltage level. VDIR is read only register and initialized as "0h" in reset state.

11.2. Timming Diagram



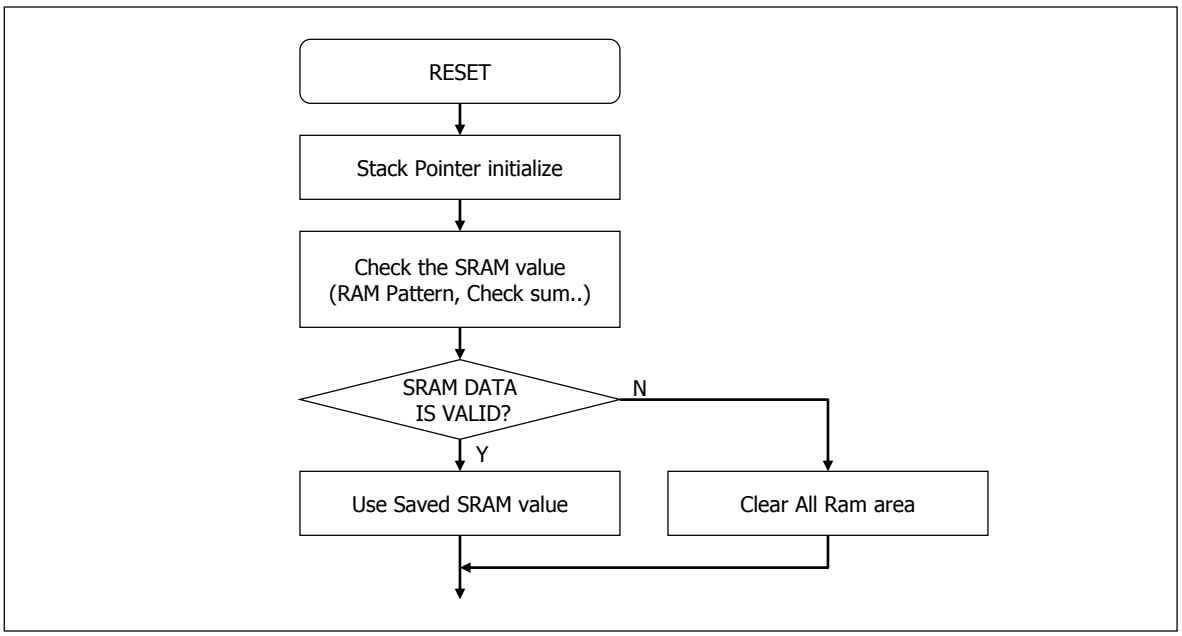
12.1 SRAM DATA BACK-UP after Low Voltage Detection

Fig. Low Voltage Detection and Protection



12.2. S/W flow chart example after Reset using SRAM DATA Back-up

Fig. S/W Flow Chart Example for SRAM Back-up

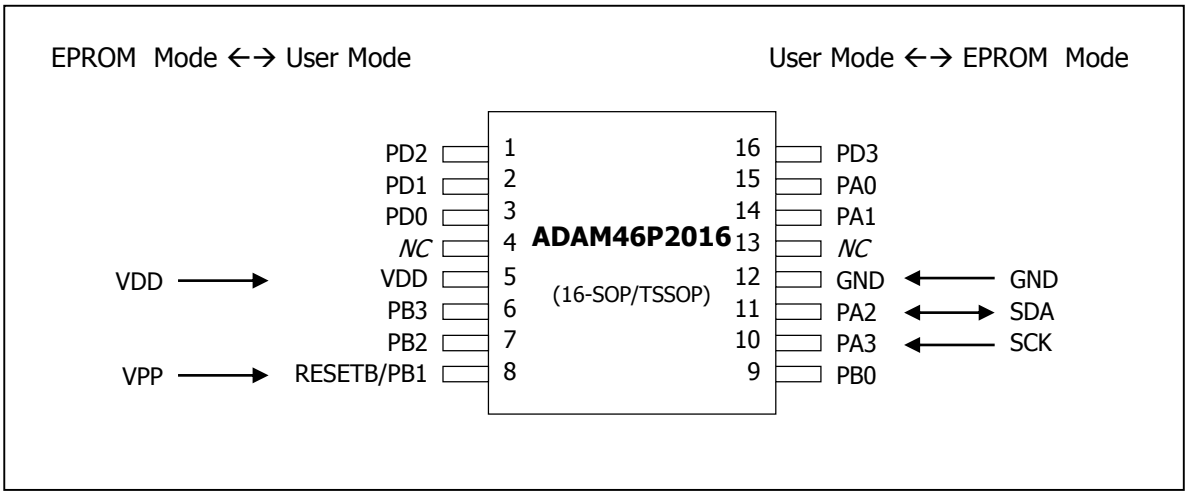


13. OTP Programming

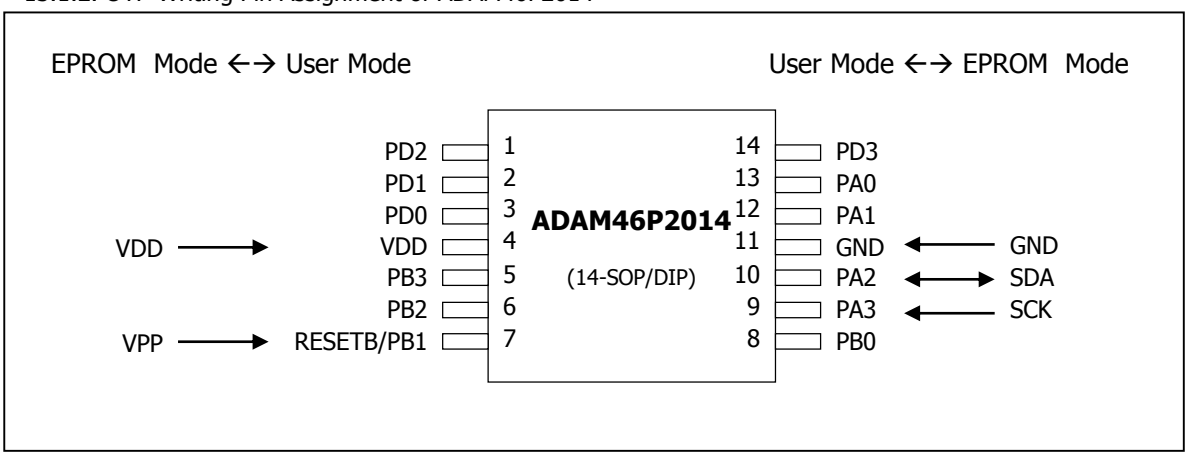
13.1. OTP Writing Pin Assignments

Symbol	User Mode	EPROM Mode
VDD	Power	VDD Power (typ. 5V)
GND	Ground	Ground (0V)
VPP	PB1	Program/Verify Power (typ. 11.5V)
SCK	PA3	Serial Clock Input
SDA	PA2	Serial Data Input/Output (Open-Drain Output)

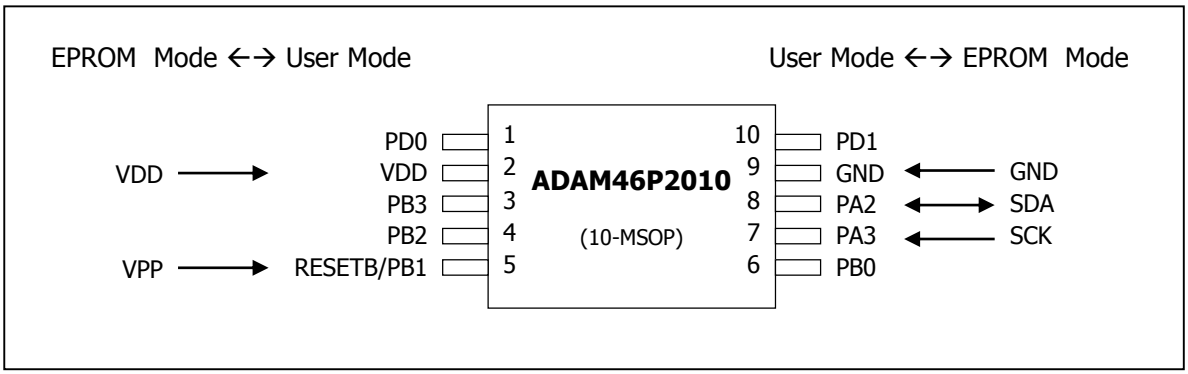
13.1.1. OTP Writing Pin Assignment of ADAM46P2016



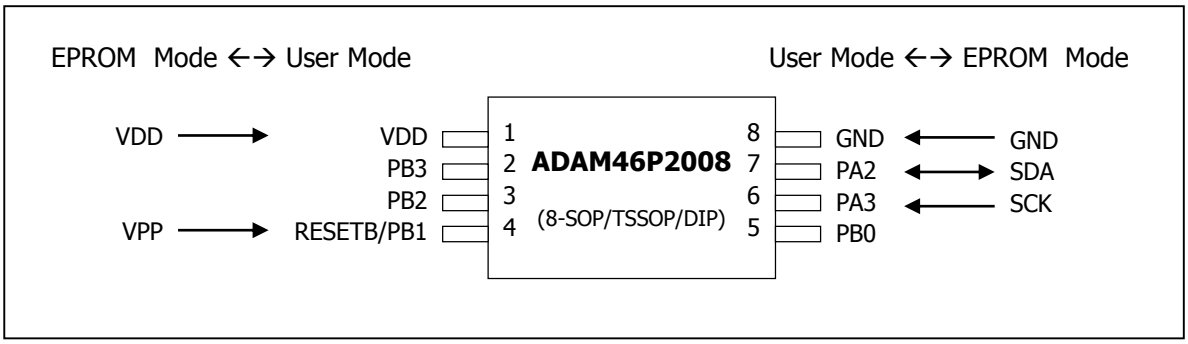
13.1.2. OTP Writing Pin Assignment of ADAM46P2014



13.1.3. OTP Writing Pin Assignment of ADAM46P2010



13.1.4. OTP Writing Pin Assignment of ADAM46P2008



13.2. Configuration Option Bit Description

pgm/vfy Address : 8000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPTION	LOCK	–	–	–	RSTS	OSCS[2:0]			LVDS	–	---					
Initial	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	OTP Code Option Description	Option Value	Remarks
15	LOCK	LOCK Definition (disable or enable reading user code)	1	Enable reading User code
			0	Disable reading User code (But Device ID and Configuration Option is readable)
14	–	–	–	
13	–	–	–	
12	–	–	–	
11	RSTS	RESETB/PB1 Selection	1	RESETB
			0	PB1
10:8	OSCS	Oscillator Type Selection	OSCS[2:0]	
		Internal RC 4MHz	111	
		Internal RC 8MHz	110	
		Internal RC 16MHz	101	
		Internal RC 1MHz	100	
		Internal RC 0.5MHz	011	
		Internal RC 2MHz	010	
		prohibited	001	
		prohibited	000	
7	LVDS	LVD Level Selection	1	LVD=1.8V
			0	LVD=2.2V
6	–	–	–	
5:0	–	Internal RC Oscillator Calibration Bits (Bit5 ~ Bit0)	–	–. Don't care at verify mode and never write `0` data at program mode. –. IRC Calibration can be done using our OTP Writer

14.1. Legend

A : accumulator(4bit)

r : peripheral address register(6bit)

[r] : data addressed by peripheral address register (4bit)

X : X register(4bit)

Y : Y register(4bit)

ABRn : address buffer register #0~3(4bit)

[@ABR] : data addressed by ABR(16bit)

DBR : data buffer register(16bit)

DBRn : data buffer register #0~3(4bit)

T0CR : Timer 0 count register(8bit)

#n4 : 0~Fh

#n2 : 0~3

#n1 : 0~1

dp : data address point(8bit)

ADS : address stack register

!abs : address

14.2. Instruction Set Table

NO	INSTRUCTION GROUP	MNEMONIC	USAGE	OPERATION	S	CY
1	Arithmetic & Logic	ADDC	ADDC m(dp),#n4	A = m(dp)+#n4+CY A = m(dp+X+Y)+#n4+CY at D flag of SFR is set. "S" set if overflow.	C	O
2			ADDC A,#n4	A = A+#n4+CY, "S" set if overflow	C	O
3			ADDC m(dp), A	A = m(dp) +A+CY, A = m(dp+X+Y) +A+CY at D flag of SFR is set. "S" set if overflow	C	O
4			ADDC Y,#n4	Y = Y + #n4 + CY, "S" set if overflow	C	O

5		SUBC	SUBC m(dp),#n4	A = m(dp) - #n4-CY,
				A = m(dp+X+Y)- #n4-CY at D flag of SFR is set.
				"S" clear if underflow
					B	W

6			SUBC A,#n4	A = A - #n4-CY, "S" clear if underflow	B	W
7			SUBC m(dp), A	A = m(dp) – A-CY, A = m(dp+X+Y)- A-CY at D flag of SFR is set. "S" clear if underflow	B	W
8			SUBC Y, #n4	Y = Y- #n4-CY, "S" clear if underflow	B	W
9		ARRC	ARRC	A = A rotate right with CY	T	R
10		ARLC	ARLC	A = A rotate left with CY	T	R
11		CMPL	CMPL	A = $\overline{A}$ + 1	Z	.
12		XOR	XOR m(dp)	A = A ⊕ m(dp) , A = A ⊕ m(dp+X+Y) at D flag of SFR is set	S	.
13		AND	AND m(dp)	A = A ^ m(dp) , A = A ^ m(dp+X+Y) at D flag of SFR is set	S	.
14		OR	OR m(dp)	A = A v m(dp) , A = A v m(dp+X+Y) at D flag of SFR is set	S	.
15	Compare	CALE	CALE #n4	"S" set if A <= #n4	E	.
16			CALE m(dp)	"S" set if A <= m(dp), "S" set if A <= m(dp+X+Y) at D flag of SFR is set.	E	.
17		CAGE	CAGE #n4	"S" set if A >= #n4	E	.
18		CANE	CANE #n4	"S" set if A != #n4	N	.
19			CANE m(dp)	"S" set if A != m(dp), "S" set if A != m(dp+X+Y) at D flag of SFR is set.	N	.
20		CYGE	CYGE #n4	"S" set if Y >= #n4	E	.
21		CYNE	CYNE #n4	"S" set if Y != #n4	N	.
22			CYNE A	"S" set if Y != A	N	.
23	Bit Manipulation	SET1	SET1 m(dp).#n2	Set bit m(dp).#n2, Set bit m(dp+X+Y).#n2 at D flag of SFR is set.	S	.
24		CLR1	CLR1 m(dp).#n2	Clear bit m(dp).#n2, Clear bit m(dp+X+Y).#n2 at D flag of SFR is set.	S	.
25		TM	TM m(dp).#n2	"S" set if m(dp) Bit = 1 "S" set if m(dp+X+Y) Bit = 1 at D flag of SFR is set.	E	.
26		SETR1	SETR1 r. #n2	Set bit [r]. #n2	S	.
27		CLRR1	CLRR1 r. #n2	Clear bit [r]. #n2	S	.
28		TSTR	TSTR r. #n2	"S" set if [r]. #n2 Bit = 1	E	.
29		NOTA1	NOTA1 #n2	A.#n2 ← ~(A.#n2)	S	.
30	Carry Manipulation	CLRC	CLRC	Carry Bit of SFR is clear.	S	0
31		SETC	SETC	Carry Bit of SFR is set.	S	1
32		TSTC	TSTC	"S" set if Carry Test = 1.	E	.
33		LDC	LDC r.#n2	CY ← [r].#n2	S	.
34		STC	STC r.#n2	[r].#n2 ← CY	S	.
35	DATA Transfer	LDM	LDM m(dp),#n4	m(dp) = #n4 m(dp+X+Y) = #n4 at D flag of SFR is set.	S	.
36			LDM m(dp), A	m(dp) ← A m(dp+X+Y) ← A at D flag of SFR is set.	S	.

14. Instruction Set

NO	INSTRUCTION GROUP	MNEMONIC	USAGE	OPERATION	S	CY
37	DATA Transfer	LDA	LDA #n4	A = #n4	S	.
38			LDA m(dp)	A ← m(dp) A ← m(dp+X+Y) at D flag of SFR is set.	S	.
39			LDA X	A ← X	S	.
40			LDA Y	A ← Y	S	.
41		LDY	LDY #n4	Y = #n4	S	.
42			LDY A	Y ← A	S	.
43		LDX	LDX #n4	X = #n4	S	.
44			LDX A	X ← A	S	.
45		XMA	XMA m(dp)	A <=> m(dp) A <=> m (dp+X+Y) at D flag of SFR is set.	S	.
46		LDW	LDW @ABR	DBR ← (@ABR) **[Note]	S	.
47			LDW DBR,T0CR	DBR1,DBR0 ← T0CR	S	.
48		LRA	LRA r	[r] ← A	S	.
49		LAR	LAR r	A ← [r]	S	.
50		LRI	LRI r,#n4	[r] = #n4	S	.
51	Branch	BR	BR !abs	If S bit of SFR =1 , Absolute branch, PC ← !abs	S	.
52			BR @ABR	If S bit of SFR =1 , Indirect branch, PC ← ABR	S	.
53	Subroutine	CALL	CALL !abs	If S bit of SFR =1 , ADS ← PC, SP ← SP – 1 , PC ← !abs	S	.
54			CALL @ABR	If S bit of SFR =1 , ADS ← PC, SP ← SP – 1 , PC ← ABR	S	.
55		RET	RET	SP ← SP +1, PC ← ADS	S	.
56		RETI	RETI	SPSFR ← SPSFR +1, SFR ← M(SPSFR) SP ← SP +1, PC ← ADS	S	.
57	Etc	NOP	NOP		S	.
58		STOP	STOP		S	.
59		WDTC	WDTC	Watchdog Timer Clear	S	.
60		SPC	SPC	Stack Pointer Clear	S	.
61		EIX	EIX	Index bit of SFR is set	S	.
62		DIX	DIX	Index bit of SFR is clear	S	.
63		EI	EI	Interrupt bit of SFR is set	S	.
64		DI	DI	Interrupt bit of SFR is clear	S	.

**[Note] The Instruction “LDW @ABR” execution time is 2cycle and execution process is as follow.
SP = SP-1 , ADS← PC ,
PC ← ABR , DBR ← (PC) , PC ← ADS , SP = SP+1
.

** CARRY BIT(CY) hold previous value before execution CLRC/SETC instruction .
Symbols have meaning as follows.
- O : Carry bit is only set when overflow has occurred in operation.
- W : Carry bit is only set when borrow has occurred in operation.
- R : Carry bit is only set or reset according to shift bit.

** STATUS BIT(S) indicates conditions for changing status. Symbols have meaning as follows.
- S : On executing an instruction, status bit is unconditionally set.
- C : Status bit is only set when overflow has occurred in operation.
- B : Status bit is only set when underflow has not occurred in operation.
- E : Status bit is only set when equality is found in comparison.
- N : Status bit is only set when equality is not found in comparison.
- Z : Status bit only set when the result is zero.
- T : Status bit only set when the carry has occurred in operation.