ADAM85F2316

Data Sheet

(V1.6-2013.07)

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ABOV Semiconductor

0. Revision History

7. [V1.6-2013.07]
   Change items
   -. Port Structure

6. [V1.5-2012.09] ← [V1.1-2012.06]
   Change items

5. [V1.4-2012.08]
   Change items

4. [V1.3-2012.07]
   Change items

3. [V1.2-2012.07]
   Change items

2. [V1.1-2012.06], [V1.5-2012.09]
   Change items

1. [V1.0-2011.11]
   Change items

0. [V0.0-2011.10]
   → 1'st release

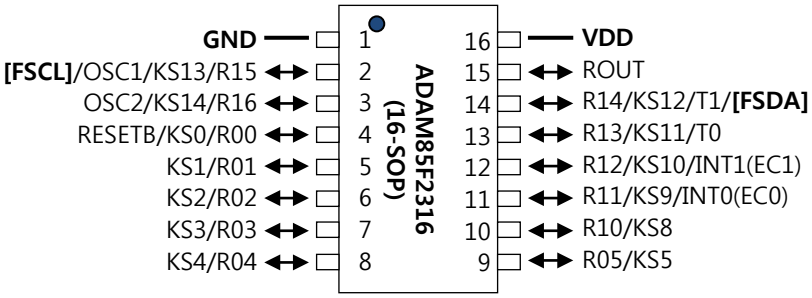
1. OVERVIEW

The ADAM85F is the High Speed and Low Voltage operating 8-bit single chip microcomputer. The ADAM85F contains ADAM85F CPU, FLASH, SRAM, 16-bit Timer, Watch Dog Timer, Key Scan (@STOP mode), Interrupt, Internal RC Oscillator, Internal WDTRC Oscillator, Infrared Receiver, Transistor for I.R LED Driver, POR, LVDR, VDI and Input/Output Port.

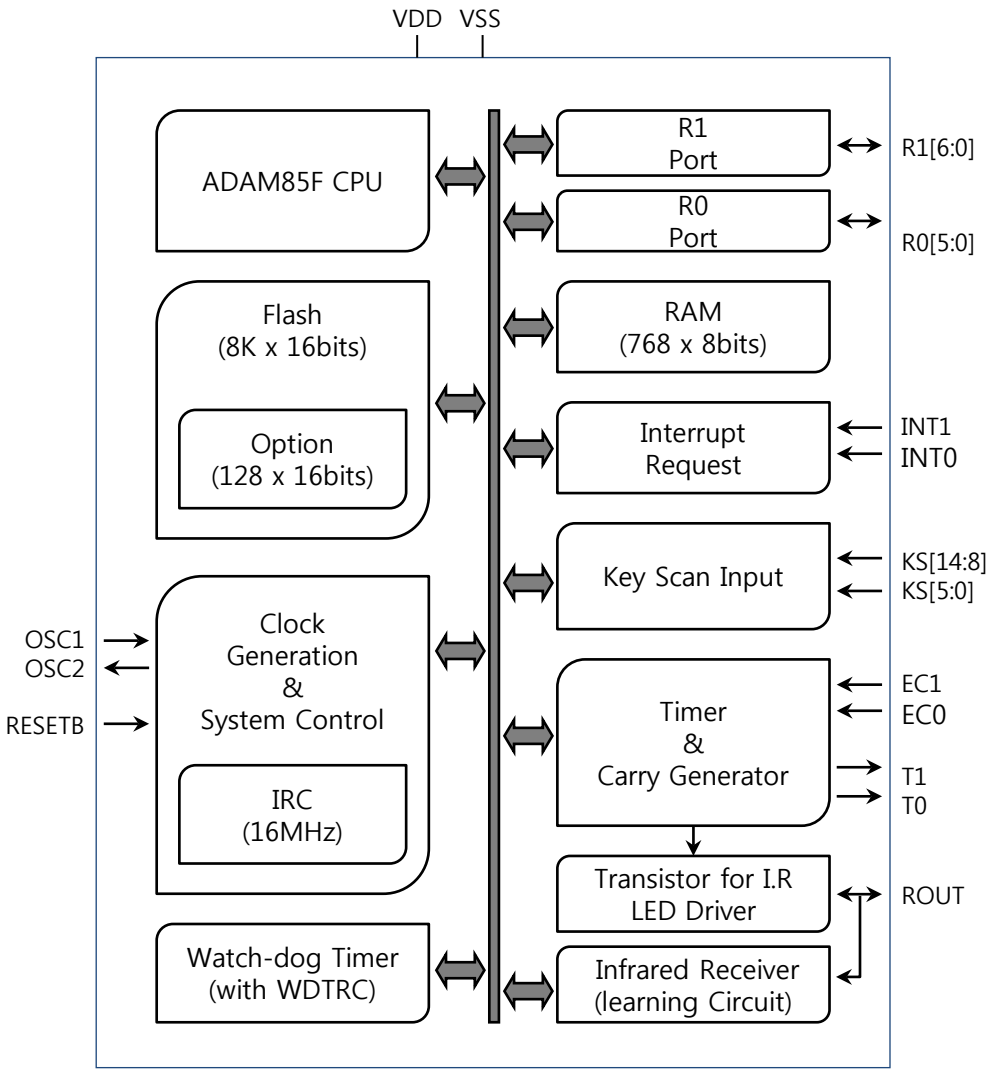
1.1. Features

✓ **High Performance 8-bit RISC CPU** • General Purpose Registers • Program Stack Level • Interrupt Stack Level • SRAM Indirect Addressing Register (X, A) • SRAM Indirect Addressing Pointer (Y)	55 - Instructions (most single cycle) 8bit x 8 (A, B, C, D, E, F, G, H) 16 level 8 level 8bit x 1 (Addressing 256bytes) 8bit x 1 (Addressing 256bytes)
✓ **Instruction Execution Time**	0.5us @8MHz
✓ **Program Memory(FLASH)** • Programmable code protection • High Endurance Flash/EEPROM cell -. 1,000 write Flash endurance -. 10,000 write EEPROM endurance -. Flash/Data EEPROM Retention: > 10 years	8K x 16bits
✓ **Data Memory(SRAM)**	768 x 8bits
✓ **Timer / Counter** • Include function : Timer/Counter/Capture/Buzzer/PWM	16bit x 2ch
✓ **Carry Generator** • Shared function with Timer0	8bit
✓ **Watch Dog Timer** • with WDTRC Oscillator (8KHz ±50%)	19bit
✓ **Key Scan (@STOP mode)** • with WDTRC Oscillator (8KHz ±50%) •)	KS channel
✓ **Interrupt Source**	External 3ch (KS, INT0, INT1) Internal 5ch (T0, T1, Y, WDT, VDI)
✓ **Internal RC Oscillator (IRC)**	On-chip (16/8/4MHz) • ±1.5% (@0℃~+40℃) • ±2.0% (@-20℃~+70℃)
✓ **Transistor for I.R LED Driver (ROUT)**	On-chip
✓ **Infrared Receiver (learning Circuit)**	On-chip with IR-AMP
✓ **Power Saving Operation Modes** • Released STOP/SLEEP mode by key input • Released STOP/SLEEP mode by All Interrupt	STOP, SLEEP
✓ **Noise immunity circuit**	On-chip
✓ **Power-On Reset (POR)**	On-chip
✓ **Low Voltage Detector/RESET (LVDR)**	On-chip
✓ **Voltage Detection Indicator (VDI)**	6 level (2.1V/2.3V/2.5V/3.0V/3.5V/4.0V)
✓ **Operating Voltage**	1.8V ~ 5.5V @(1 ~ 4MHz) 2.0V ~ 5.5V @(1 ~ 16MHz) 2.2V ~ 5.5V @(1 ~ 20MHz)
✓ **Operating Temperature**	-20^{O}C ~ 70^{O}C
✓ **Package**	16-SOP/TSSOP

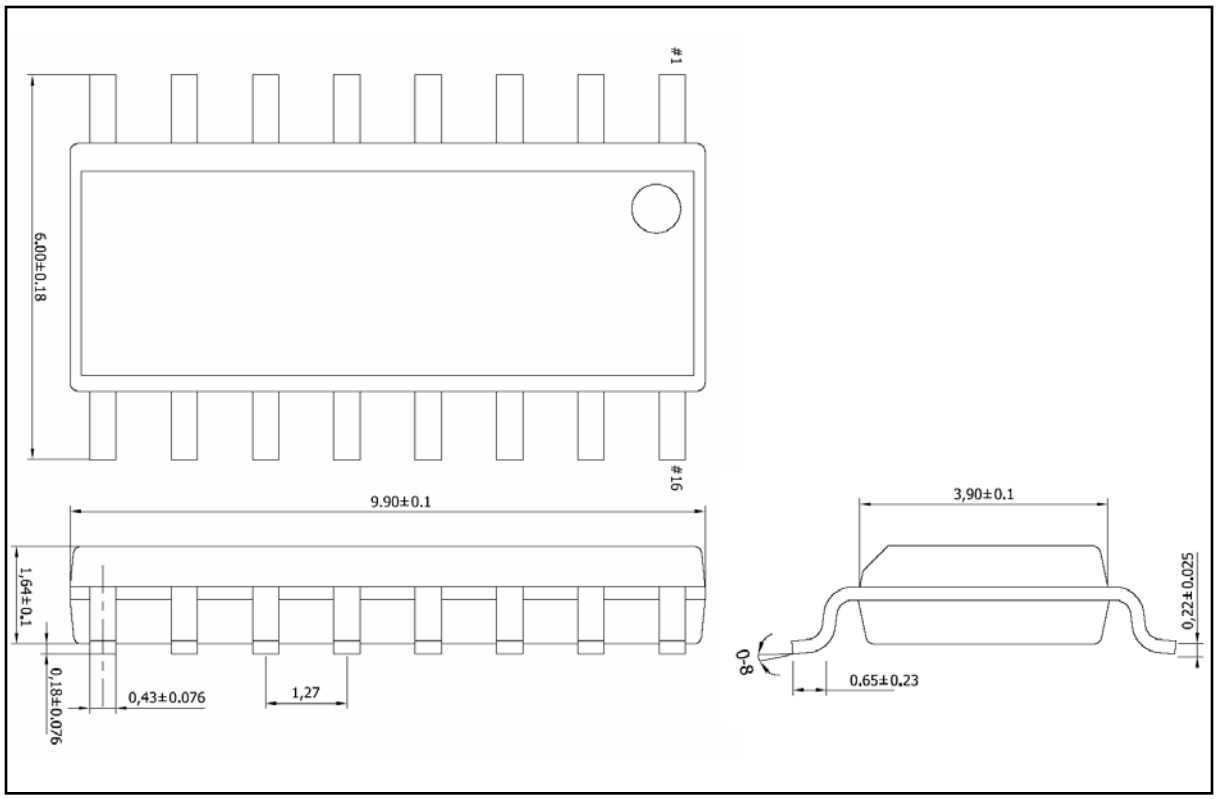
1.2. Pin Assignments



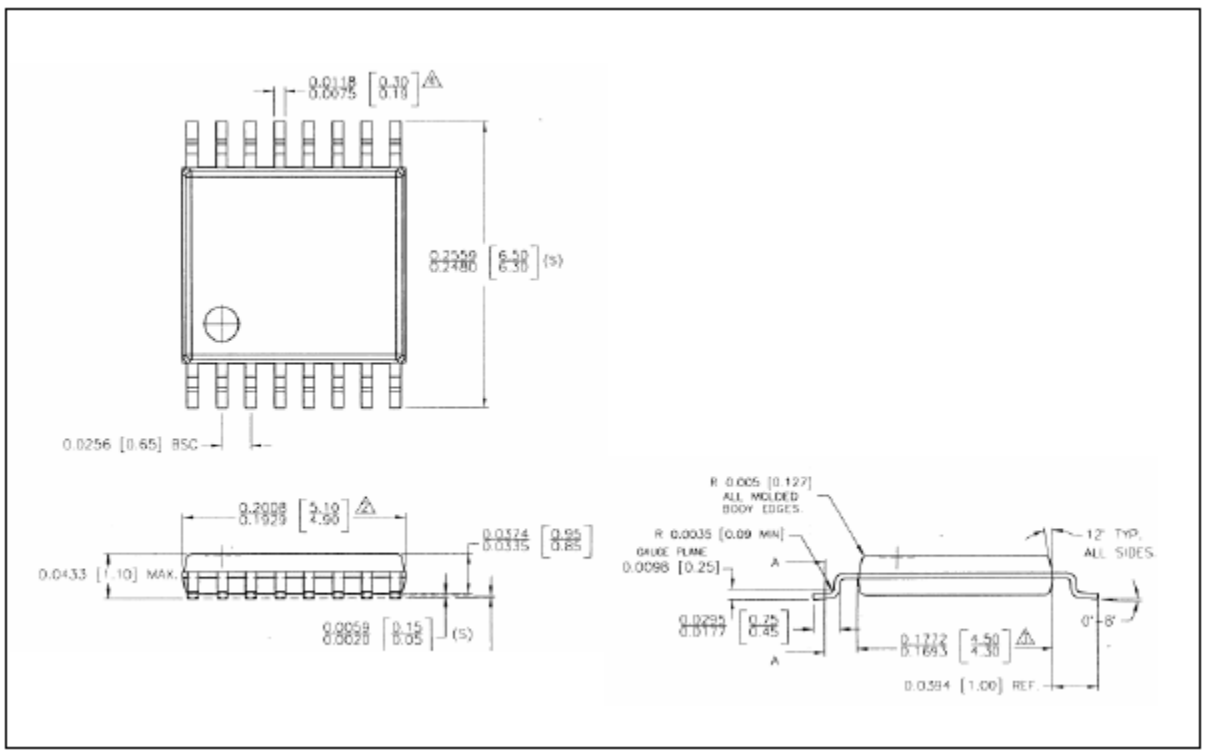
1.3. Block Diagram



1.4. Package Dimension



16-SOP (150MIL) Pin Dimension (dimensions in mm)



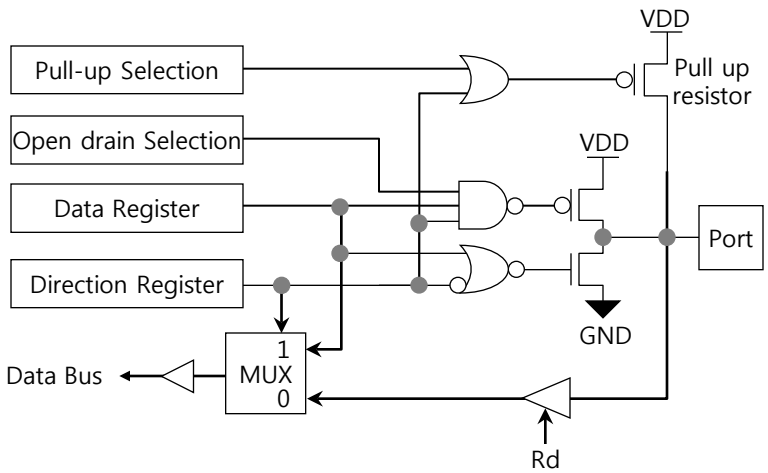
16-TSSOP (4.4mm) Pin Dimension (dimensions in mm)

1.5. Pin Function

Pin Name	I/O	Function	RESET	STOP
R05/KS5 R04/KS4 R03/KS3 R02/KS2 R01/KS1 R00/KS0/RESETB	I/O	-. 6-bit I/O Port. -. CMOS input with pull-up resistor. -. Pull-ups can be disabled by user Program. -. Push-pull output. -. Can be programmable as N-ch open drain output individually. -. Each pin can be set and reset by R0 Data register value. -. Direct Driving of LED (N-Tr). -. Can be selectable as Key Scan Input pin individually by user program.	Input	State of before STOP
R16/KS14/OSC2 R15/KS13/OSC1 R14/KS12/T1 R13/KS11/T0 R12/KS10/INT1(EC1) R11/KS9/INT0(EC0) R10/KS8	I/O	-. 7-bit I/O Port. -. CMOS input with pull-up resistor. -. Pull-ups can be disabled by user Program. -. Push-pull output. -. Can be programmable as N-ch open drain output individually. -. Each pin can be set and reset by R1 Data register value. -. Direct Driving of LED (N-Tr). -. Can be selectable as Key Scan Input pin individually by user program. -. Can be selectable as Timer Output pin individually by user program. -. Can be selectable as External Interrupt Input pin individually by user program.	Input	State of before STOP
ROUT	O	- High Current Output - Learning Circuit Input	Output	Hi-Z (Low)
VDD	P	- Positive Power Supply		
GND	P	- Ground		

1.6. Port Structure

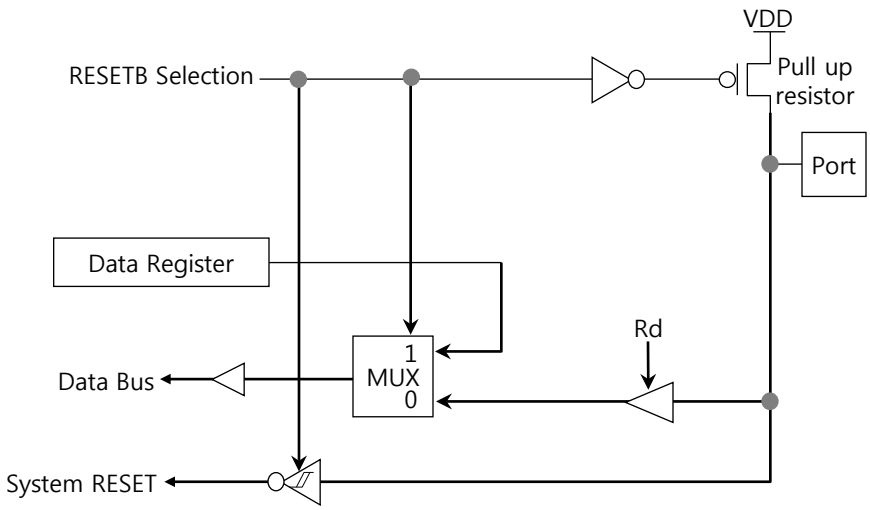
◆ Normal I/O mode with Pull-Up & Open-Drain

Pin Name	Circuit Type	RESET
R1[6:0] R0[5:0]		Input
Shared Function	KS/INT(EC)/TIMER OSC1/OSC2/RESETB	

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
KS	Input	*	Port	Data	KS		
INT(EC)	Input	*	Port	Data	INT(EC)		
TIMER	Output	Off	Port	Data	TIMER		
OSC1	Input	Off	Data	Data	OSC1	R1[5] RESET	
OSC2	Input	Off	Data	Data	OSC2	R1[6] RESET	

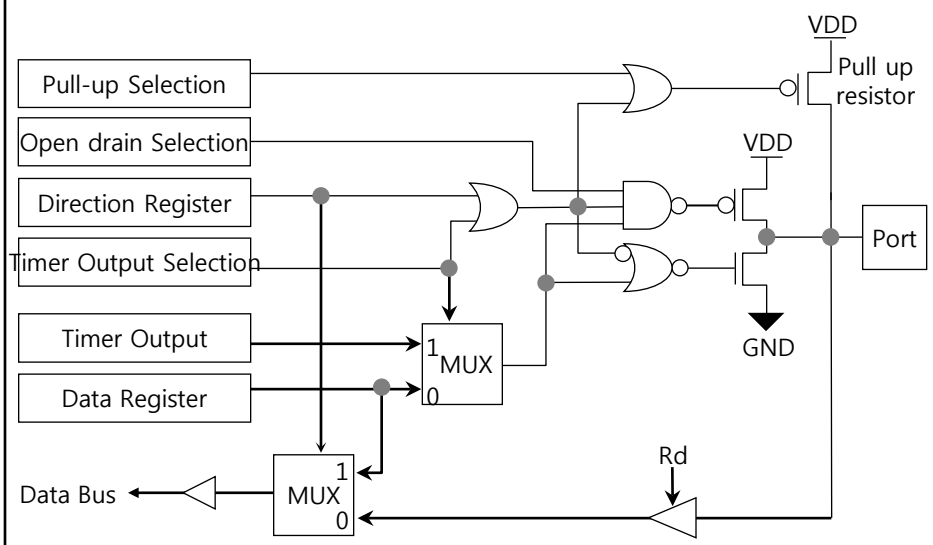
* : It is depend on user definition.

◆ RESETB (Input with Pull-up) mode

Pin Name	Circuit Type	RESET
RESETB		Input

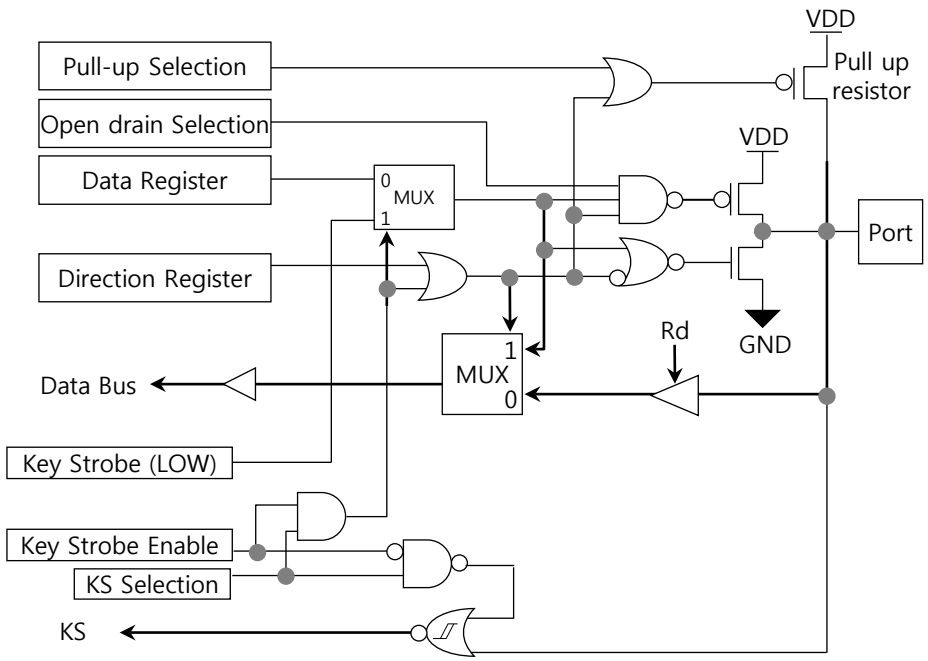
Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	-			
RESETB	Input	On	Data	-	Pull-up RESETB	R0[0] RESET	

◆ Timer output mode

Pin Name	Circuit Type	RESET
T1 T0		Input

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
TIMER	Output	Off	Port	Data	TIMER		

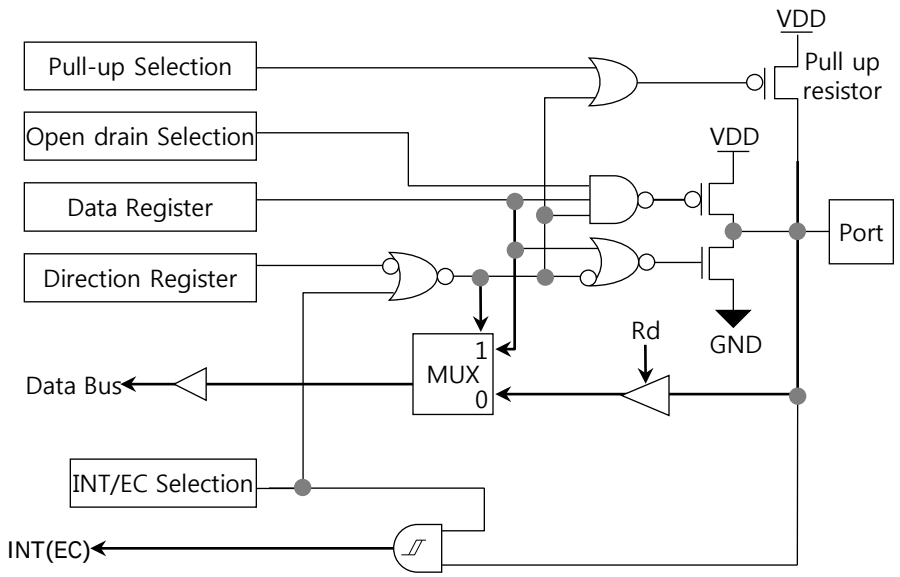
◆ Key-Scan mode

Pin Name	Circuit Type	RESET
KS[14:8] KS[5:0]		Input

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
KS	Input	*	Port	Data	KS		
Key Strobe	Output	Off	-	-	Key Strobe		

* : It is depend on user definition.

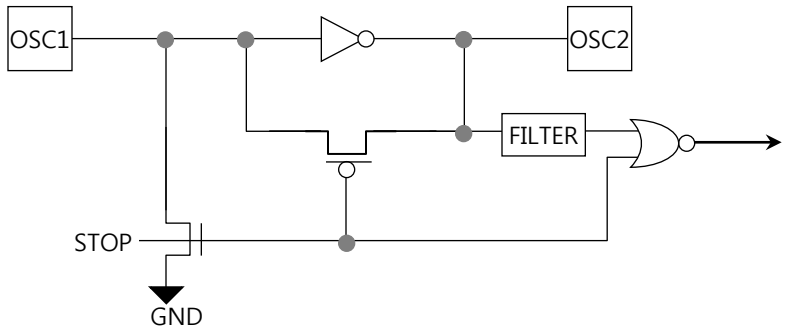
◆ External Interrupt [INT(EC)] mode

Pin Name	Circuit Type	RESET
INT0(EC0) INT1(EC1)		Input

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
INT(EC)	Input	*	Port	Data	INT(EC)		

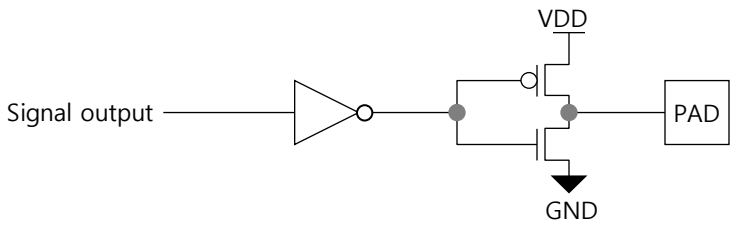
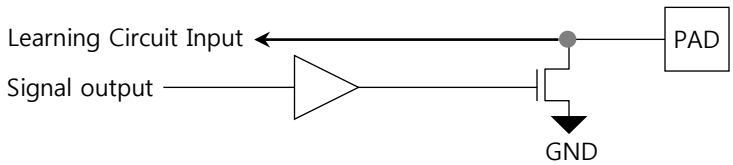
* : It is depend on user definition.

◆ OSC1/OSC2 mode

Pin Name	Circuit Type	RESET
OSC1 OSC2		Oscillation

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
OSC1	Input	Off	Data	Data	OSC1	R1[5] RESET	
OSC2	Input	Off	Data	Data	OSC2	R1[6] RESET	

◆ ROUT mode

Pin Name	Circuit Type	RESET
ROUT		Output
		Output

1.7. Electrical Characteristics

1.7.1. Absolute Maximum Ratings (Ta = 25^{O}C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	VDD	-0.3 ~ +6.0	V
Input Voltage	V_I	-0.3 ~ VDD + 0.3	V
Output Voltage	V_O	-0.3 ~ VDD + 0.3	V
Storage Temperature	T_{STG}	-65 ~ 150	^{O}C
Power Dissipation	P_D	700	mW

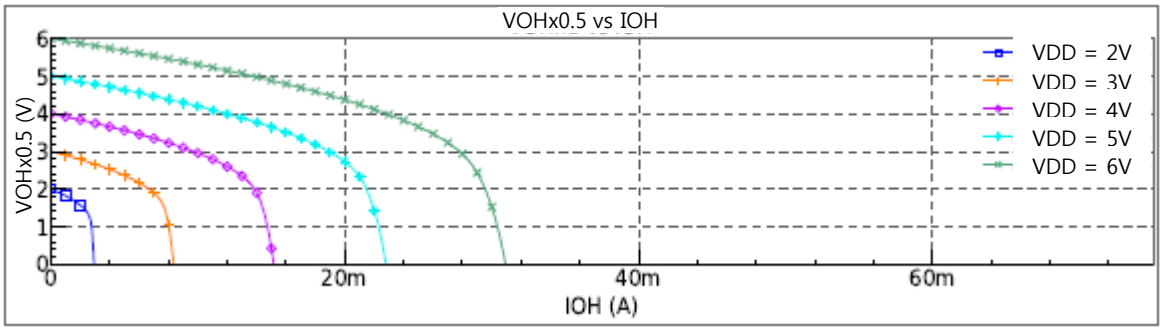
1.7.2. Recommended Operating Ranges

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX	UNIT
Supply Voltage	VDD	fXin = 4MHz	1.8	-	5.5	V
		fXin = 8MHz	2.0	-	5.5	V
		fXin = 20MHz	2.2	-	5.5	V
Oscillation Frequency	f_{OSC}		1	8	20	MHz
Operating Temperature	T_{OPR}		-20		70	^{O}C

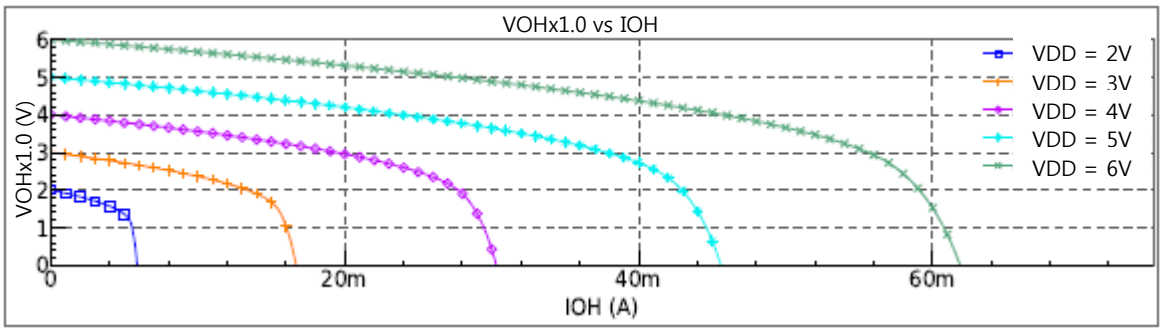
1.7.3. DC Characteristics (Ta = 25℃)

PARAMETER	Symbol	Condition			Specification			UNIT
					MIN.	TYP.	MAX.	
High level input voltage	VIHX	OSC1			0.9VDD		VDD	V
	VIH1	INT0, INT1, EC0, EC1			0.8VDD		VDD	V
	VIH2	R0, R1			0.7VDD		VDD	V
Low level input voltage	VILX	OSC1			0		0.1VDD	V
	VIL1	INT0, INT1, EC0, EC1			0		0.2VDD	V
	VIL2	R0, R1			0		0.3VDD	V
High level input leakage current	IIH	R0, R1		VIH = VDD			1	μA
Low level input leakage current	IIL	R0, R1		VIL = 0V			-1	μA
High level output voltage	VOH1	R0, R1	VDD = 3V	IOH = -5mA	VDD-0.7			V
	VOH2	OSC1, OSC2	VDD = 3V	IOH = -0.2mA	VDD-0.7			V
Low level output voltage	VOL1	R0, R1	VDD = 3V	IOL = 5mA			0.7	V
	VOL2	OSC1, OSC2	VDD = 3V	IOL = 0.2mA			0.7	V
High level output leakage current	IOHL	R0, R1		VOH = VDD			1	μA
Low level output leakage current	IOLL	R0, R1		VOL = 0V			-1	μA
High level output current	IOH	ROUT	VDD = 3V	VOH = 2V	-20	-15	-10	mA
Low level output current	IOL1	ROUT	VDD = 3V	VOL = 1V	3	3.5	4	mA
	IOL2	ROUT	VDD = 3V	VOL = 1V	200	250	300	mA
Input Pull-up current	IPU	R0, R1	VDD = 5V		-48	-60	-72	μA
			VDD = 3V		-20	-25	-30	
Power supply current	IDD	Operating current	VDD = 5V	f_{OSC} = 8MHz		2.5	4	mA
			VDD = 3V	f_{OSC} = 4MHz		1	2	
	ISLEEP	Sleep mode current	VDD = 5V	f_{OSC} = 8MHz		1	2	mA
			VDD = 3V	f_{OSC} = 4MHz		0.5	1	
	ISTOP	Stop mode current	VDD = 5V	Oscillator stop LVD on		2.5	5	μA
			VDD = 3V			1.5	2	
Voltage Detection Indicator	VDI_{40}	VDD Level			3.8	4.0	4.2	
	VDI_{35}				3.3	3.5	3.7	
	VDI_{30}				2.8	3.0	3.2	
	VDI_{25}				2.3	2.5	2.7	V
	VDI_{23}				2.1	2.3	2.5	
	VDI_{21}				1.9	2.1	2.3	
OSC FeedBack Resistor	R_{FD}		VDD = 3V		0.3	1	3	MΩ
RAM retention supply voltage	VRET				0.7			V

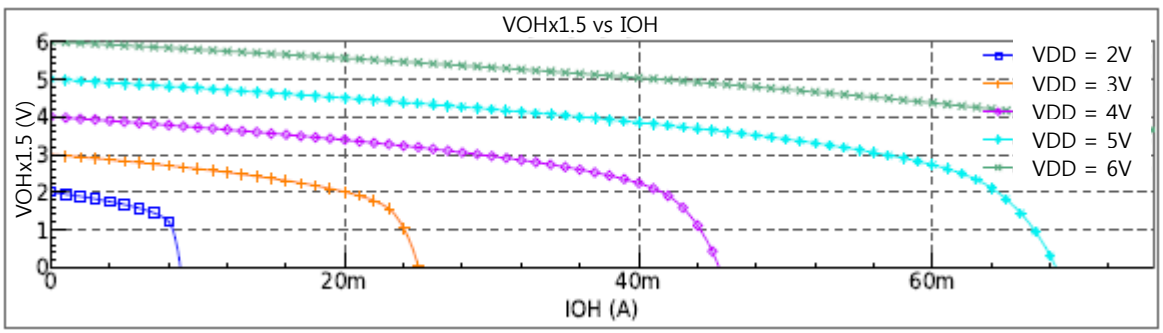
• **VOHx0.5 vs IOH Characteristics graph**



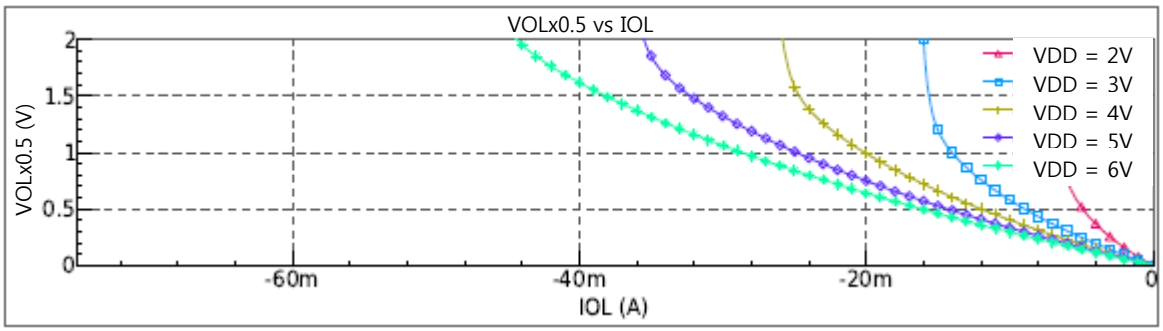
• **VOHx1.0 vs IOH Characteristics graph**



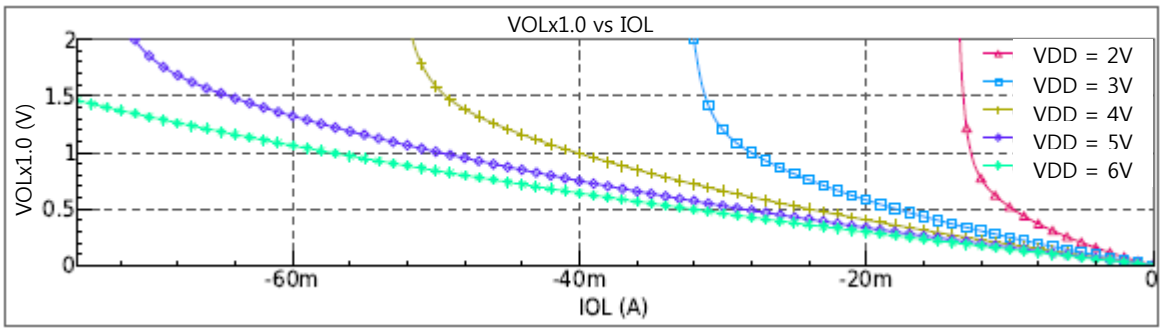
• **VOHx1.5 vs IOH Characteristics graph**



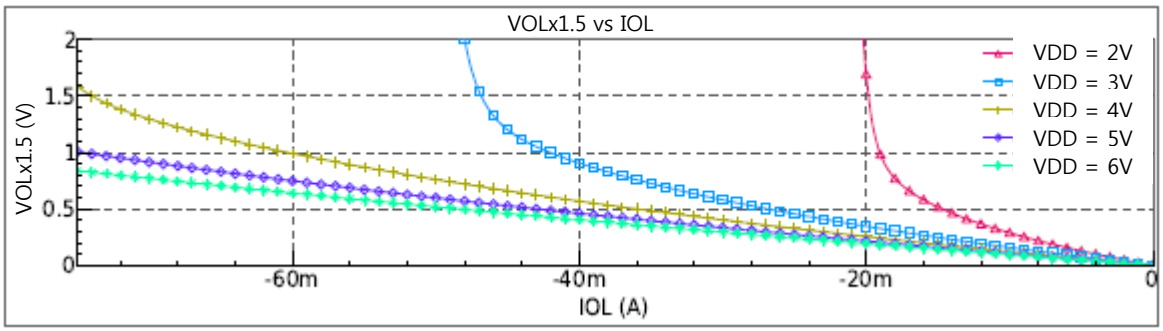
• **VOLx0.5 vs IOL Characteristics graph**



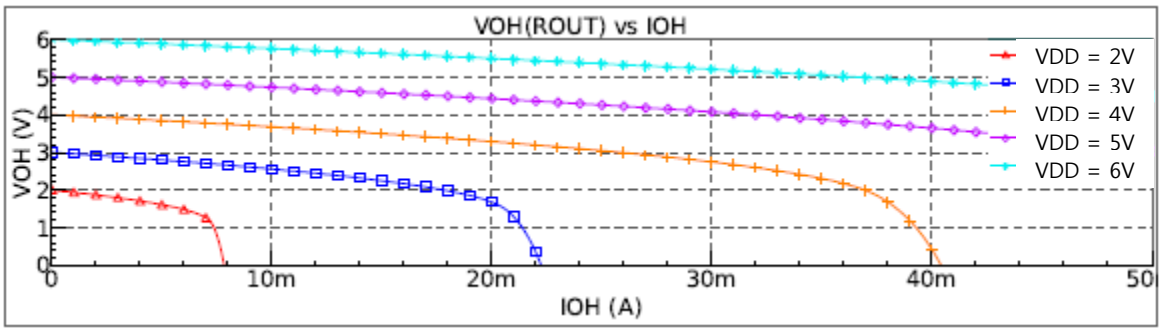
• **VOLx1.0 vs IOL Characteristics graph**



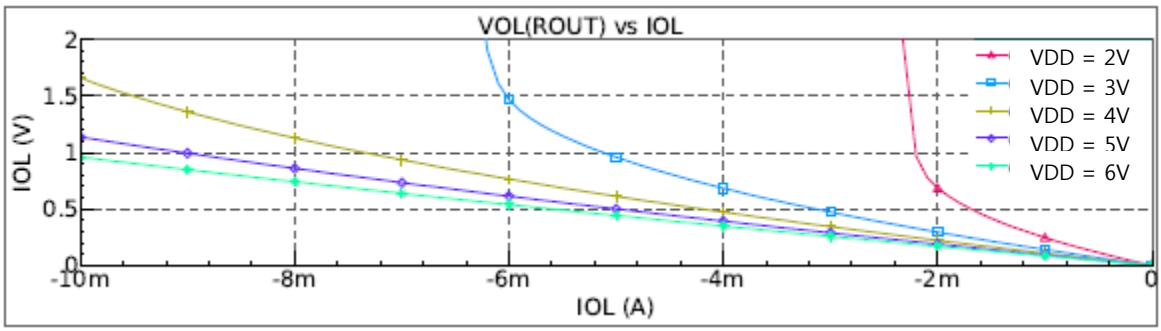
• **VOLx1.5 vs IOL Characteristics graph**



• **VOH(ROUT) vs IOH Characteristics graph**



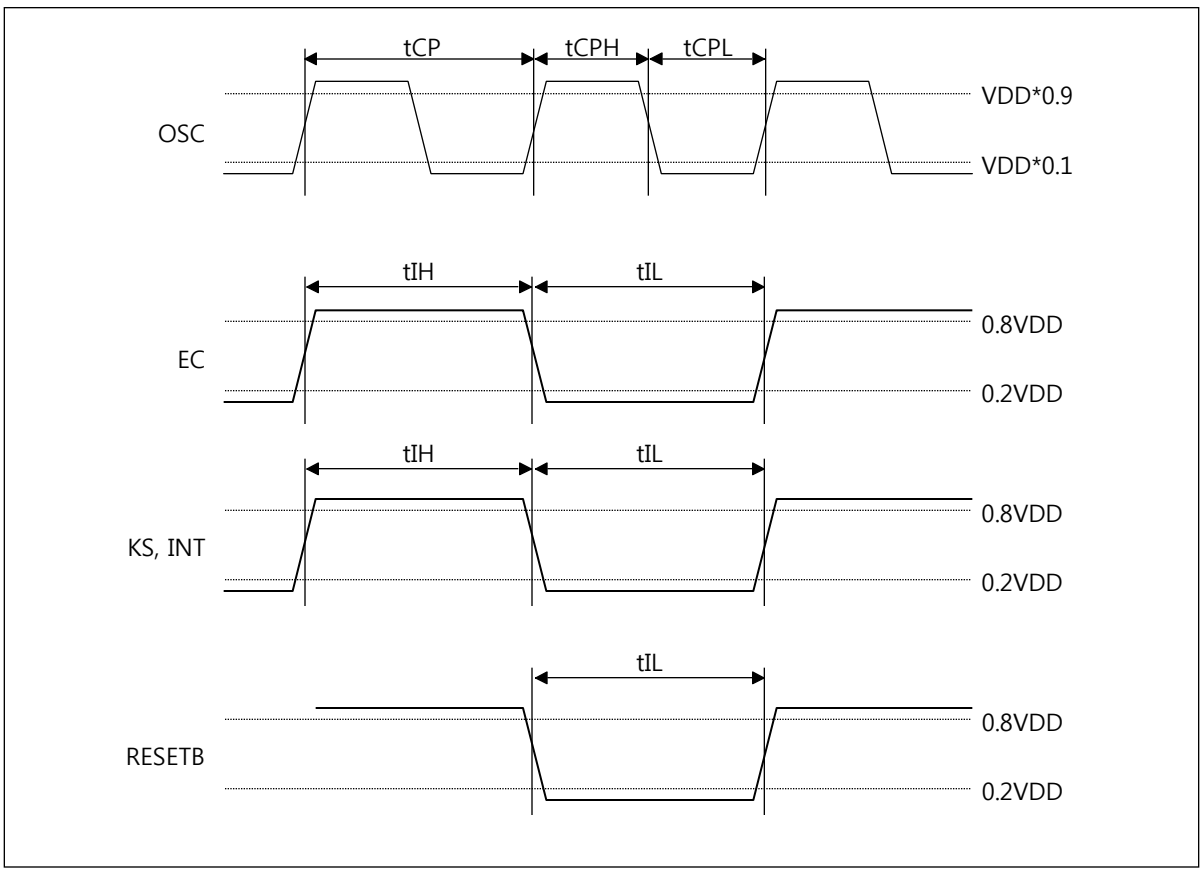
• **VOL(ROUT) vs IOL Characteristics graph**



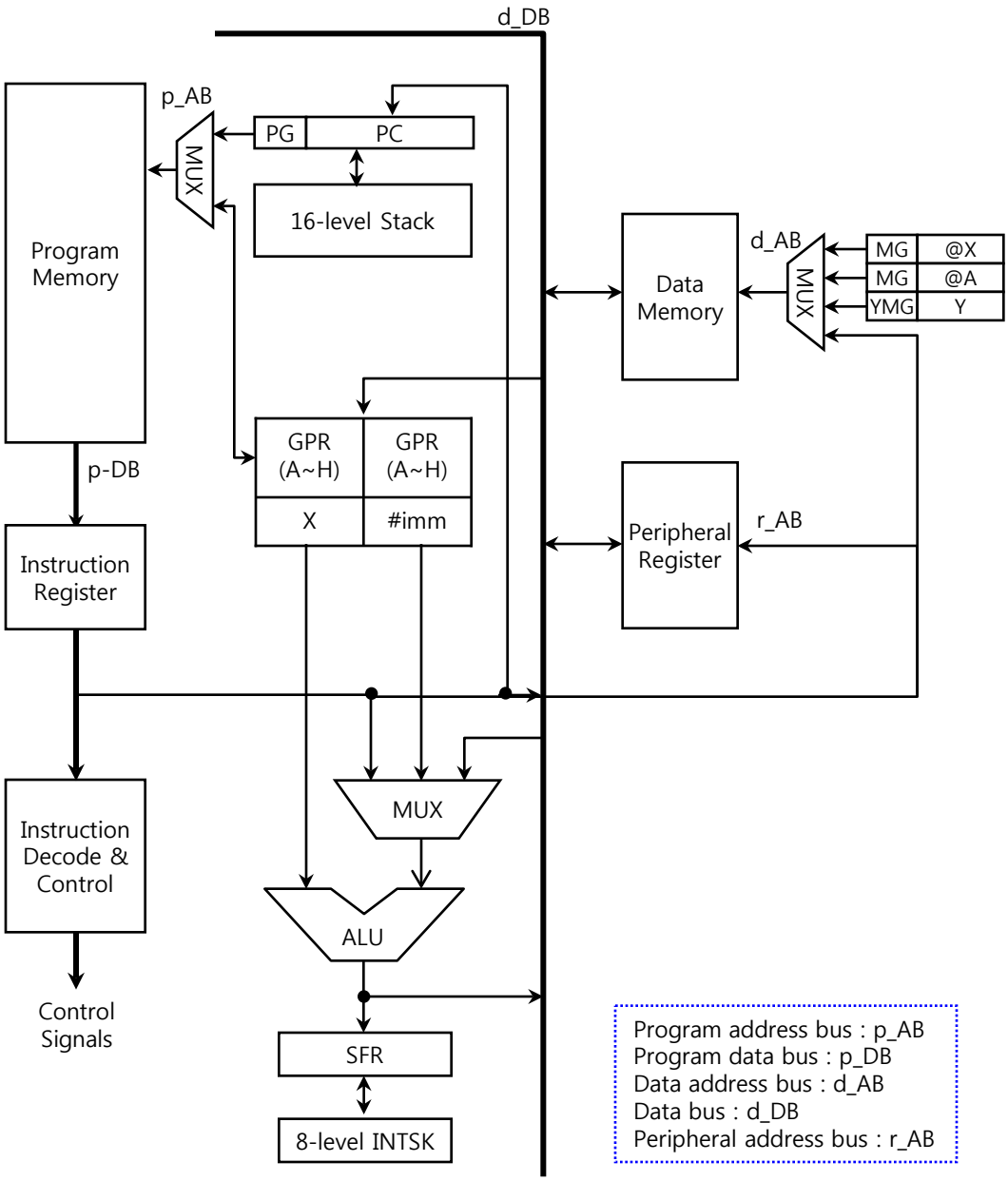
1.7.4. AC Characteristics (Ta = 25℃)

Parameter	Symbol	Pin	Specification			Unit
			min.	typ.	max.	
External clock input cycle time	tCP	OSC	125	250	1000	ns
External clock input High	tCPH	OSC		0.5		tCP
External clock input Low	tCPL	OSC		0.5		tCP
System clock cycle time	tSYS	-		4		tCP
External pulse width High	tIH	EC	1			tCP
External pulse width Low	tIL	EC	1			tCP
Interrupt pulse width High	tIH	KS, INT	2			tSYS
Interrupt pulse width Low	tIL	KS, INT	2			tSYS
RESETB pulse width Low	tIL	RESETB	8			tSYS

Minimum pulse width



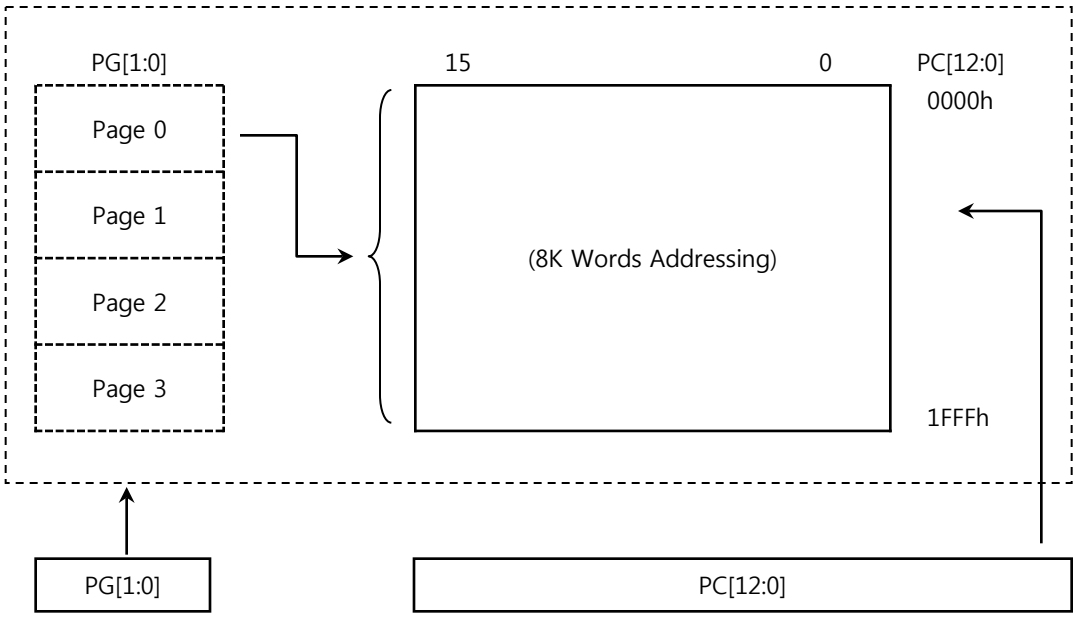
- **CPU Function Diagram**



2.1. Program Memory Map

The ADAM85F can address up to Maximum 64Kbytes (32K x 16bit) for Program Memory.
Program Counter(PC[12:0]) and Program Page Register(PG[1:0]) is used to address the whole area of Program Memory having an instruction (16bit) to be next executed.
The Program Memory consists of 8K words on each Page, and thus each Page can hold up to 8K steps of instructions.

• The program memory is composed as shown below.



Mode of Program Memory Addressing

8K words Addressing	12	11	10	9	8	7	6	5	4	3	2	1	0
	PC[12:0]												

2.2. Program Page Register

The following registers are used to address the Program Memory.

• Program Page Register (PG) :
Holds ROM's Page number (Page 0 ~ Page 3) to be addressed.
it is writable by MOVPG instruction Only.

* To change the Page,
1) MOVPG #PageNo.
2) CALL or BR instruction exeute.

	7	6	5	4	3	2	1	0	
PG	-	-	PG1	PG0	-	-	PC14	PC13	79h
initial value	0	0	0	0	0	0	0	0	
R/W	R	R	R	R	R	R	R	R	

Selection Mode of PG

Bit Name	Selection Mode		Remarks
-	0	-	
-	0	-	
PG1 PG0	00	Program Memory Page 0	read only
	01	Program Memory Page 1	
	10	Program Memory Page 2	
	11	Program Memory Page 3	
-	0	-	
-	0	-	
PC14 PC13	00	Program Counter	read only

• **Program counter (PC) :**
Available for addressing word on each Page.

This 13-bit binary counter increments for fetching a word to be addressed in the currently addressed Page having an instruction to be next executed. For easier programming, at turning on the power, the program counter is reset to the zero location(0000h). The PG is also set to "0h". Then the program counter specifies the next address. When BR, CALL or RET, RETI instructions are decoded, the switches on each step are turned off not to update the address. Then, for BR or CALL, address data are taken in from the instruction operands (A0 to A12), or for RET, RETI and address including Page address is fetched from stack register.

bit	12												0
PC	PC												
initial value	0000h												

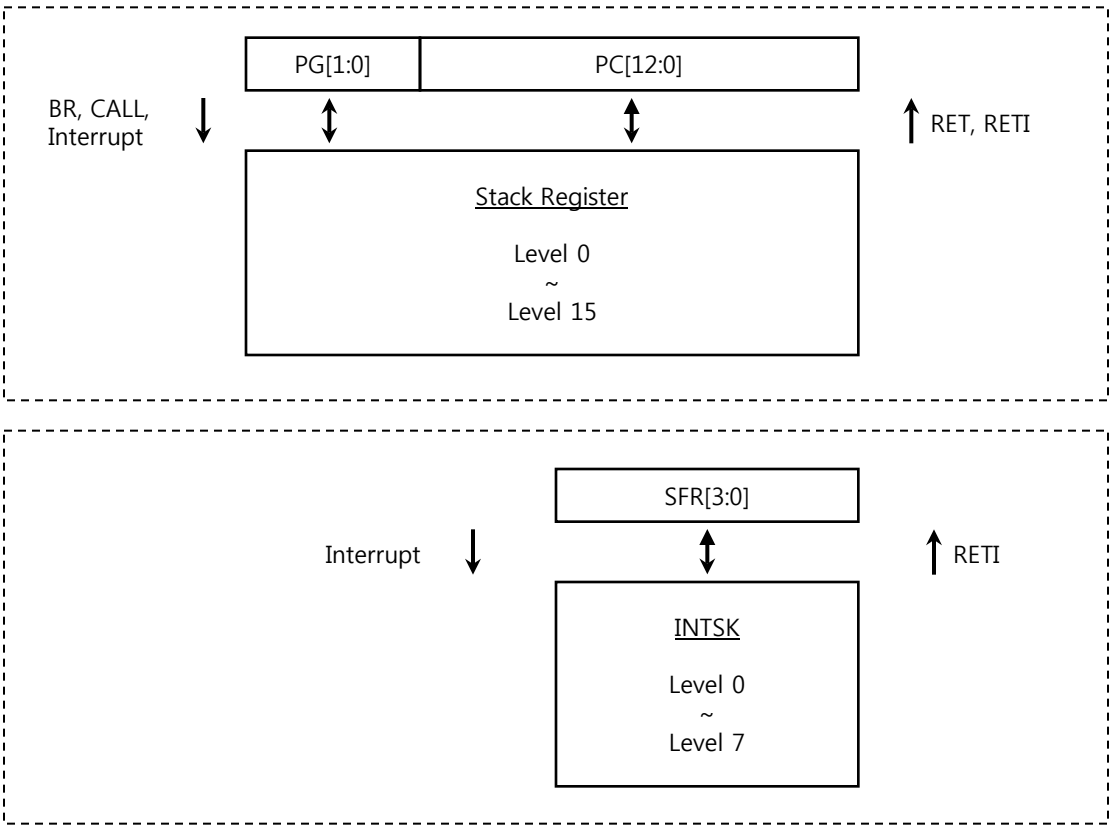
Selection Mode of PC

PC[12:0]	Program Counter	0000h ~ 1FFFh	8K words Addressing

• **Stack Register (SR) :**

Stores returned-word address in the subroutine call mode.

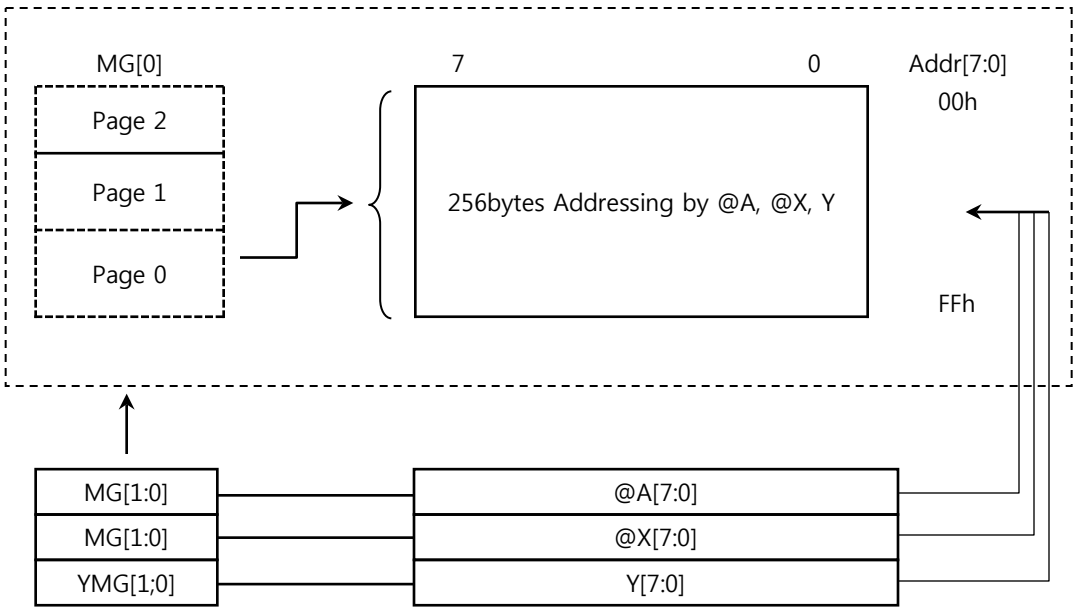
The Stack register stores a return address when the subroutine call instruction is executed or interrupt is acknowledged.
If subroutine or interrupts are nested to more than 16 levels, internal reset is occurred.
The interrupt stack register(INTSK) Saves the contents of Status flag register(SFR) when an interrupt is acknowledged.
The Saved contents are restored when an interrupt return(RETI) instruction is executed.
INTSK Saves data each time an interrupt is acknowledged. but the data stored first is lost if more than 8 levels of interrupts occur.



2.3. DATA Memory Map

The ADAM85F can address up to Maximum 768bytes for Data Memory.
Data Memory Address[7:0] and Data Page Register(MG[1:0]) is used to address the whole area of Data Memory .
The Data Memory consists of 256bytes on each Page.
Y register can address up to 256bytes (Page 0 : 00h ~ ffh) for SRAM backup mode.

• The data memory is composed as shown below.



The following register is used to address the SRAM.

• Memory Page Register (MG) :
Holds SRAM's Page number (Page 0 ~ Page 2) to be addressed.
It is writable with MOVMG instruction only.

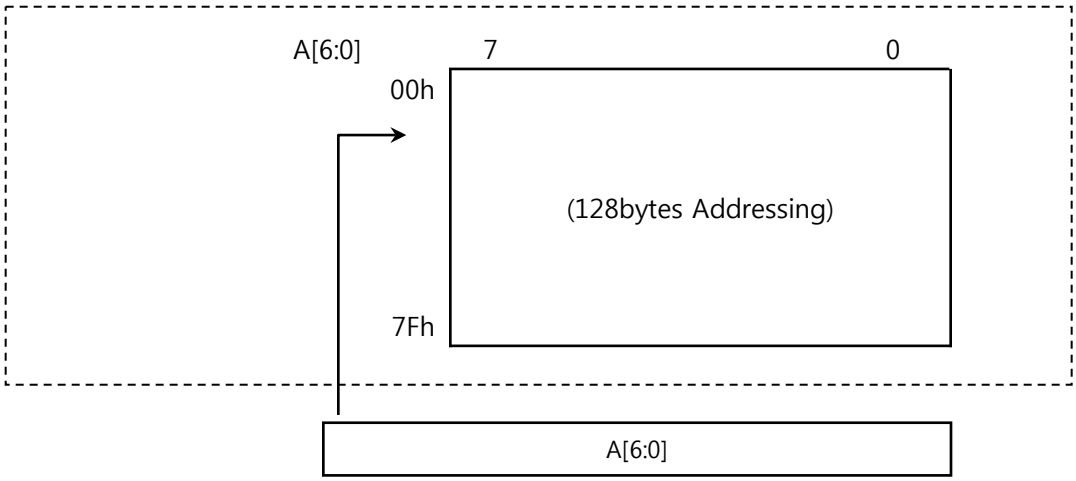
Selection Mode of MG

MG[1:0]	Data Memory Page Register	00	Page 0
		01	Page 1
		10	Page 2
		11	-

2.4. Peripheral Memory Map

The ADAM85F can address up to Maximum 128bytes for Peripheral Control Registers. Peripheral Address[6:0] is used to address the whole area of Registers .

• The Peripheral Register is composed as shown below.



2.5. General Purpose Registers

2.5.1. X-register (X)

X-register is consist of 8 bits. It can used for a general-purpose register.
X-register also used for data memory indirect addressing mode register.

2.5.2. Y-register (Y)

2.5.2.1. *main routine*

Y-register is consist of 8 bits.
Y-register used for data memory (0-Page) indirect addressing pointer.
Before Y interrupt setting, write value('hff ~ 'h01) except 'h00.

	7	6	5	4	3	2	1	0	
Y	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	78h
initial value	1	1	1	1	1	1	1	1	
R/W	W	W	W	W	W	W	W	W	

Selection Mode of Y

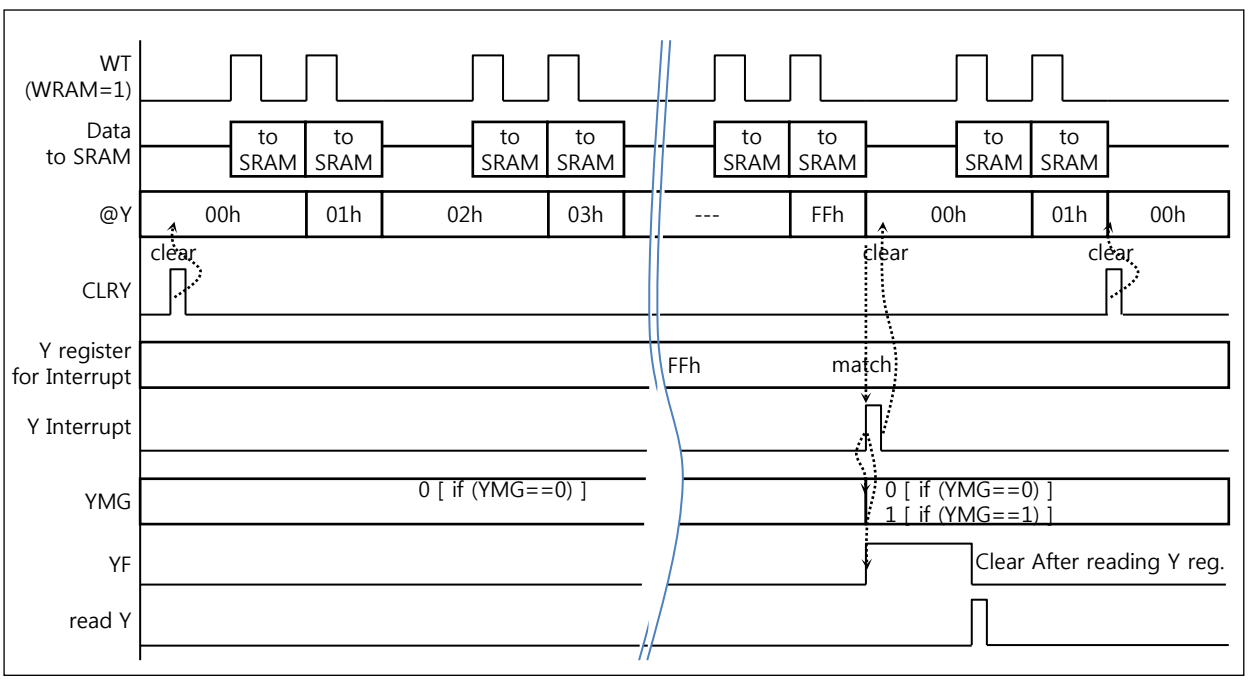
Bit Name	Selection Mode	Remarks
Y[7:0]	Addressing 256bytes SRAM Buffer	

2.5.2.2. *interrupt service routine*

Y-register is consist of 8 bits.
Y-register used for interrupt flag register.
Interrupt flag is cleared by reading Y register.

	7	6	5	4	3	2	1	0	
INTY	0	0	0	0	0	0	0	YF	78h
initial value	0	0	0	0	0	0	0	0	
R/W	R	R	R	R	R	R	R	R	

• Y Interrupt Timing Diagram



2.5.3. GPR (A, B, C, D, E, F, G, H)

GPR is consist of 8 x 8bits. It can used for a general-purpose register.
GPR also used for program memory indirect addressing mode register.
A (GPR) also used for data memory indirect addressing mode register.

2.5.4 PC & PG Buffer Register (read only)

it is writable by MOVPG instruction Only.

PC is the program counter, PG is the program Page buffer.
PG is updated to PC when call or br executed.

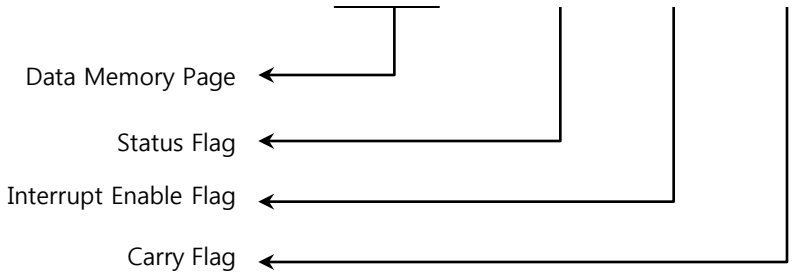
	7	6	5	4	3	2	1	0	
PG	-	-	PG1	PG0	-	-	PC14	PC13	79h
initial value	0	0	0	0	0	0	0	0	
R/W	R	R	R	R	R	R	R	R	

2.6. Status Flag Register (SFR)

Status Flag Register (SFR) is consist of 4-bit register.

Consisted of the flags showing the post state of operation and the flags determining the CPU operation, initialized as 0h in reset state.

	7	6	5	4	3	2	1	0	
SFR	-	-	-	MG1	MG0	S	I	Cy	7Ah
initial value	0	0	0	0	0	0	0	0	
R/W	R	R	R	R	R	R	R	R	



• Data Memory Page (MG)
  -. 00 : Page 0
  -. 01 : Page 1
  -. 10 : Page 2
  -. 11 : -

• Status flag (S)
  -. According to the condition after executing an instruction , set or clear.
  -. Can not be set or clear by any instruction.

• Interrupt enable flag (I)
  -. Master enable flag of interrupt.
  -. Set and cleared by EI, DI
  -. This Flag immediately becomes "0" when an interrupt is served.
  -. After interrupt service routine, restored I flag to INTSK.

• Carry flag (Cy)
  -. Carry flag bit is set when there is carry or borrow After executing ADD / SUB / SHIFT / ROTATE / LDC / STC instructions.
  -. Set by SETC and clear by CLRC.

2.7. Peripheral Registers

ADDR.	FUNCTIONAL DESCRIPTION								R/W	Symbol	RESET	Access Mode
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0			7 0	
00h	PORT R0 DATA REG.								R/W	R0	0011_1111	*bit/byte
	-	-	R05	R04	R03	R02	R01	R00				
01h	PORT R0 PULL UP SELECTION REG.								W	R0PU	0011_1111	byte
	-	-	R0PU5	R0PU4	R0PU3	R0PU2	R0PU1	R0PU0				
02h	PORT R0 OPEN DRAIN SELECTION REG.								W	R0OD	0000_0000	byte
	-	-	R0OD5	R0OD4	R0OD3	R0OD2	R0OD1	R0OD0				
03h	PORT R0 DIRECTION REG.								W	R0DD	0000_0000	byte
	-	-	R0DD5	R0DD4	R0DD3	R0DD2	R0DD1	R0DD0				
04h	PORT R0 FUNCTION SELECTION REG.								W	R0FN	0000_0000	byte
	-	-	R0FN5	R0FN4	R0FN3	R0FN2	R0FN1	R0FN0				
05h	-								-	-	-	-
06h	PORT R0 IOH/IOL CONTROL REG LOW.								W	R0IL	0000_0000	byte
	R03IL		R02IL		R01IL		R00IL					
07h	PORT R0 IOH/IOL CONTROL REG HIGH.								W	R0IH	0000_0000	byte
	-		-		R05IH		R04IH					
08h	PORT R1 DATA REG.								R/W	R1	0111_1111	*bit/byte
	-	R16	R15	R14	R13	R12	R11	R10				
09h	PORT R1 PULL UP SELECTION REG.								W	R1PU	0111_1111	byte
	-	R1PU6	R1PU5	R1PU4	R1PU3	R1PU2	R1PU1	R1PU0				
0Ah	PORT R1 OPEN DRAIN SELECTION REG.								W	R1OD	0000_0000	byte
	-	R1OD6	R1OD5	R1OD4	R1OD3	R1OD2	R1OD1	R1OD0				
0Bh	PORT R1 DIRECTION REG.								W	R1DD	0000_0000	byte
	-	R1DD6	R1DD5	R1DD4	R1DD3	R1DD2	R1DD1	R1DD0				
0Ch	PORT R1 FUNCTION SELECTION REG LOW.								W	R1FL	0000_0000	byte
	R13FL		R12FL		R11FL		R10FL					
0Dh	PORT R1 FUNCTION SELECTION REG HIGH.								W	R1FH	0000_0000	byte
	-		R16FH		R15FH		R14FH					
0Eh	PORT R1 IOH/IOL CONTROL REG LOW.								W	R1IL	0000_0000	byte
	R13IL		R12IL		R11IL		R10IL					
0Fh	PORT R1 IOH/IOL CONTROL REG HIGH.								W	R1IH	0000_0000	byte
	-		R16IH		R15IH		R14IH					

Caution :
Before operating pheriperals, Must be initialize undefined registers.
*bit is read-modified operation. (SETR1/CLRR1 instruction)

2.7. Peripheral Registers

ADDR.	FUNCTIONAL DESCRIPTION								R/W	Symbol	RESET	Access Mode
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0			7 0	
30h	EXTERNAL INTERRUPT EDGE SELECTION REG 0.								W	IEDS0	0000_0000	byte
	-		IEDI1		IEDI0		IEDK					
31h	-								-	-	-	-
32h	INTERRUPT ENABLE REG 0.								R/W	IENR0	0000_0000	bit/byte
	-	-	WVE	T1E	T0E	INT1E	INT0E	KSYE				
33h	INTERRUPT REQUEST FLAG REG 0.								R/W	IRQR0	0000_0000	bit/byte
	-	-	WVF	T1F	T0F	INT1F	INT0F	KSYF				
34h	-								-	-	-	-
35h	-								-	-	-	-
36h	-								-	-	-	-
37h	PROHIBIT								W	EPM8	-	-
38h	EP MODE REG 7.								W	EPM7	0000_0000	byte
	-	-	-	SELF	-	-	-	-				
39h	EP MODE REG 6.								W	EPM6	0000_0000	byte
	ERA	PGM	-	-	-	-	-	-				
3Ah	PROHIBIT								W	EPM5	-	-
3Bh									W	EPM4	-	-
3Ch	PROHIBIT								W	EPM3	-	-
3Dh									W	EPM2	-	-
3Eh	PROHIBIT								W	EPM1	-	-
3Fh									W	EPM0	-	-

Caution :
Before operating pheriperals, Must be initialize undefined registers.

2.7. Peripheral Registers

ADDR.	FUNCTIONAL DESCRIPTION								R/W	Symbol	RESET	Access Mode
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0			7 0	
40h	ROUT & TIMER OUTPUT SYNC. CONTROL REG.								R/W	RCR	0000_0000	bit/byte
	TCKWDTRC	SYNCST	TOC	CRON	PR1	PR0	PRON	REM				
41h	TIMER0 MODE REG 0.								R/W	T0MR0	0000_0000	bit/byte
	T0CS	T0CN	T0EG	T0CPE1	T0CPE0	T0CK2	T0CK1	T0CK0				
42h	TIMER0 MODE REG 1.								R/W	T0MR1	0000_0000	bit/byte
	T0LTOS1	T0LTOS0	TOS0	WRAM0	CMOD0	INTS0	OUTC0	CKC0				
43h	TIMER0 DATA0 REG LOW.								W	T0D0L	undefined	byte
	T0D0L7	T0D0L6	T0D0L5	T0D0L4	T0D0L3	T0D0L2	T0D0L1	T0D0L0				
	TIMER0 COUNT REG LOW.								R	T0CRL	undefined	byte
	T0CRL7	T0CRL6	T0CRL5	T0CRL4	T0CRL3	T0CRL2	T0CRL1	T0CRL0				
44h	TIMER0 DATA1 REG LOW.								W	T0D1L	undefined	byte
	T0D1L7	T0D1L6	T0D1L5	T0D1L4	T0D1L3	T0D1L2	T0D1L1	T0D1L0				
45h	TIMER0 DATA0 REG HIGH.								W	T0D0H	undefined	byte
	T0D0H7	T0D0H6	T0D0H5	T0D0H4	T0D0H3	T0D0H2	T0D0H1	T0D0H0				
	TIMER0 COUNT REG HIGH.								R	T0CRH	undefined	byte
	T0CRH7	T0CRH6	T0CRH5	T0CRH4	T0CRH3	T0CRH2	T0CRH1	T0CRH0				
46h	TIMER0 DATA1 REG HIGH.								W	T0D1H	undefined	byte
	T0D1H7	T0D1H6	T0D1H5	T0D1H4	T0D1H3	T0D1H2	T0D1H1	T0D1H0				
47h	-								-	-	-	-
48h	-								-	-	-	-
49h	TIMER1 MODE REG 0.								R/W	T1MR0	0000_0000	bit/byte
	T1CS	T1CN	T1EG	T1CPE1	T1CPE0	T1CK2	T1CK1	T1CK0				
4Ah	TIMER1 MODE REG 1.								R/W	T1MR1	0000_0000	bit/byte
	T1LTOS1	T1LTOS0	TOS1	WRAM1	CMOD1	INTS1	OUTC1	CKC1				
4Bh	TIMER1 DATA0 REG LOW.								W	T1D0L	undefined	byte
	T1D0L7	T1D0L6	T1D0L5	T1D0L4	T1D0L3	T1D0L2	T1D0L1	T1D0L0				
	TIMER1 COUNT REG LOW.								R	T1CRL	undefined	byte
	T1CRL7	T1CRL6	T1CRL5	T1CRL4	T1CRL3	T1CRL2	T1CRL1	T1CRL0				
4Ch	TIMER1 DATA1 REG LOW.								W	T1D1L	undefined	byte
	T1D1L7	T1D1L6	T1D1L5	T1D1L4	T1D1L3	T1D1L2	T1D1L1	T1D1L0				
4Dh	TIMER1 DATA0 REG HIGH.								W	T1D0H	undefined	byte
	T1D0H7	T1D0H6	T1D0H5	T1D0H4	T1D0H3	T1D0H2	T1D0H1	T1D0H0				
	TIMER1 COUNT REG HIGH.								R	T1CRH	undefined	byte
	T1CRH7	T1CRH6	T1CRH5	T1CRH4	T1CRH3	T1CRH2	T1CRH1	T1CRH0				
4Eh	TIMER1 DATA1 REG HIGH.								W	T1D1H	undefined	byte
	T1D1H7	T1D1H6	T1D1H5	T1D1H4	T1D1H3	T1D1H2	T1D1H1	T1D1H0				
4Fh	-								-	-	-	-

Caution :
Before operating pheriperals, Must be initialize undefined registers.

2.7. Peripheral Registers

ADDR.	FUNCTIONAL DESCRIPTION								R/W	Symbol	RESET	Access Mode
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0			7 0	
60h	-								-	-	-	-
61h	-								-	-	-	-
62h	-								-	-	-	-
63h	-								-	-	-	-
64h	-								-	-	-	-
65h	-								-	-	-	-
66h	-								-	-	-	-
67h	-								-	-	-	-
68h	-								-	-	-	-
69h	-								-	-	-	-
6Ah	-								-	-	-	-
6Bh	-								-	-	-	-
6Ch	-								-	-	-	-
6Dh	PAGE BUFFER REG.								W	PBUF	0000_0000	byte
6Eh	ERASE PROGRAM ADDRESS LOW REG.								W	EPAL	0000_0000	byte
6Fh	ERASE PROGRAM ADDRESS HIGH REG.								W	EPAH	0000_0000	byte

Caution :
Before operating pheriperals, Must be initialize undefined registers.

2.7. Peripheral Registers

ADDR.	FUNCTIONAL DESCRIPTION								R/W	Symbol	RESET	Access Mode
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0			7 0	
70h	SYSTEM CONTROL REG.								W	SCR	0000_0000	byte
	LVDOFF	RSTNF	OSCNF1	OSCNF0	PSS	OCS	DRS1	DRS0				
71h	-								-	-	-	-
72h	WATCH DOG TIMER CONTROL REG.								R/W	WDTR	0000_0000	bit/byte
	TKS1	TKS0	KSEN	RCWDTEN	WDTRST	RCWDTDIS	WAKEUP1	WAKEUP0				
73h	LRN REG.								R/W	LRN	0000_0000	bit/byte
	RIOL1	RIOL0	YMG	T1WRAM	LRNEN	NTRENB	LNF1	LNF0				
74h	PROHIBIT								W	MTM0	-	-
75h	PROHIBIT								W	MTM1	-	-
76h	PROHIBIT								W	MTM2	-	-
77h	PROHIBIT								W	MTM3	-	-
78h	Y REG.								R/W	Y	0000_0000	byte
	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0				
	INTY REG.								R	INTY	0000_0000	byte
	0	0	0	0	0	0	0	YF				
79h	Program Page Reg. (PG[1:0], ADDR[14:13])								R	PG	0000_0000	byte
	-	-	PG1	PG0	-	-	PC14	PC13				
7Ah	STATUS FLAG REG.								R	SFR	0000_0000	byte
	-	-	-	MG1	MG0	S	I	Cy				
7Bh	PROHIBIT								R	MLAA	-	-
7CH	PROHIBIT								R	MRDL	-	-
7Dh	PROHIBIT								R	MRDH	-	-
7Eh	VTG. DETECTION INDICATOR ENABLE REG.								W	WDIER	0000_0000	byte
	SNST	VDIRST	VDIER5	VDIER4	VDIER3	VDIER2	VDIER1	VDIER0				
	VTG. DETECTION INDICATOR DATA REG.								R	VDIDR	0000_0000	byte
	-	-	VDIDR5	VDIDR4	VDIDR3	VDIDR2	VDIDR1	VDIDR0				
7Fh	VTG. DETECTION INDICATOR FLAG REG.								R	VDIFR	0000_0000	byte
		-	VDIFR5	VDIFR4	VDIFR3	VDIFR2	VDIFR1	VDIFR0				

Caution :
Before operating pheriperals, Must be initialize undefined registers.

3. I/O Ports

The ADAM85F has 13 I/O ports which are R0(6 I/O), R1(7 I/O) and One Output port which is ROUT.
R0 and R1 Port have Function Selection Register.
Pull-up resistor of R0 and R1 ports can be selectable by program.
R0 and R1 ports contains data direction register which controls I/O and data register which stores port data.
R0 and R1 Ports have Open Drain selection register.

I/O Ports Registers

Port	Data Reg.	Pull-up Reg.	Open-Drain Reg.	Direction Reg.	Function Reg.	IOH Reg.	IOL Reg.
port R0	R0	R0PU	R0OD	R0DD	R0FN	R0IOH	R0IOL
port R1	R1	R1PU	R1OD	R1DD	R1FN	R1IOH	R1IOL

R/W	R/W	W	W	R/W	R/W	W	W
Initial value	'1'	'1'	0000_0000	0000_0000	0000_0000	0000_0000	0000_0000
default	'1'	disable	enable	input	disable	x1	x1

✓ Port R0

• R0 Data Register (R0)

	7	6	5	4	3	2	1	0	
R0	-	-	R05	R04	R03	R02	R01	R00	00h
initial value	0	0	1	1	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R0 data register (R0) is 6-bit register to store data of port R0.
When set as the output state by R0DD, and data is written in R0, data is outputted into R0 pin.
When read at the input state, pin is read.
When read at the output state, data register is read.
bit is read-modified operation. (SETR1/CLRR1 instruction)
The initial value of R0 is "3Fh" in reset state.

• R0 Pull-up Selection Register (R0PU)

	7	6	5	4	3	2	1	0	
R0PU	-	-	R0PU5	R0PU4	R0PU3	R0PU2	R0PU1	R0PU0	01h
initial value	0	0	1	1	1	1	1	1	
R/W	W	W	W	W	W	W	W	W	

R0 pull-up resistor control register (R0PU) is 6-bit register and can control pull-up on or off each bit, if corresponding port is selected as input.
If R0PU is selected as "0", pull-up is enabled and if selected as "1", it is disabled.
R0PU is write-only register and initialized as "3Fh" in reset state.
The pull-up is automatically disabled, if corresponding port is selected as output.

• R0 Open Drain Selection Register (R0OD)

	7	6	5	4	3	2	1	0	
R0OD	-	-	R0OD5	R0OD4	R0OD3	R0OD2	R0OD1	R0OD0	02h
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

R0 Open Drain Selection Register (R0OD) is 6-bit register, and can assign R0 port as open drain output port each bit If R0OD is selected as "0", port R0 is open drain output, and if selected as "1", it is push-pull output. R0OD is write-only register and initialized as "00h" in reset state.

• **R0 I/O Data Direction Register (R0DD)**

	7	6	5	4	3	2	1	0	
R0DD	-	-	R0DD5	R0DD4	R0DD3	R0DD2	R0DD1	R0DD0	03h
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

R0 I/O Data Direction Register (R0DD) is 6-bit register, and can assign input state or output state to each bit. If R0DD is "0", port R0 is in the input state, and if "1", it is in the output state. R0DD is write-only register. Since R0DD is initialized as "00h" in reset state, the whole port R0 becomes input state.

• **R0 Function Selection Register (R0FN)**

	7	6	5	4	3	2	1	0	
R0FN	-	-	R0FN5	R0FN4	R0FN3	R0FN2	R0FN1	R0FN0	04h
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

R0 Function Selection Register (R0FN) is 6-bit register, and can assign Key Scan pin or not.
If R0FN is selected as "1", Key Scan function is enabled and if selected as "0", it is disabled. R0FN is write-only register and initialized as "00h" in reset state.

Selection Mode of R0FN

Bit Name	Selection Mode		Remarks
-	0	-	
	1	-	
-	0	-	
	1	-	
R0FN5	0	R05	
	1	KS5	
R0FN4	0	R04	
	1	KS4	
R0FN3	0	R03	
	1	KS3	
R0FN2	0	R02	
	1	KS2	
R0FN1	0	R01	
	1	KS1	
R0FN0	0	R00	*RESETB
	1	KS0	

• **R0 IOH/IOL Control Register Low (R0IL)**

	7	6	5	4	3	2	1	0	
R0IL	R03IL		R02IL		R01IL		R00IL		06h
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

• **R0 IOH/IOL Control Register High (R0IH)**

	7	6	5	4	3	2	1	0	
R0IH	-		-		R05IH		R04IH		07h
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

Selection Mode of R0IL

Bit Name	Selection Mode		Remarks
R03IL	00	x1.0/x1.0	
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	
R02IL	00	x1.0/x1.0	
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	
R01IL	00	x1.0/x1.0	
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	
R00IL	00	x1.0/x1.0	
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	

Selection Mode of R0IH

Bit Name	Selection Mode		Remarks
-	00	-	
	01	-	
	10	-	
	11	-	
-	00	-	
	01	-	
	10	-	
	11	-	
R05IH	00	x1.0/x1.0	
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	
R04IH	00	x1.0/x1.0	
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	

✓ Port R1

• R1 Data Register (R1)

	7	6	5	4	3	2	1	0	
R1	-	R16	R15	R14	R13	R12	R11	R10	08h
initial value	0	1	1	1	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R1 data register (R1) is 7-bit register to store data of port R1.
When set as the output state by R1DD, and data is written in R1, data is outputted into R1 pin.
When read at the input state, pin is read.
When read at the output state, data register is read.
bit is read-modified operation. (SETR1/CLRR1 instruction)
The initial value of R1 is "7Fh" in reset state.

• R1 Pull-up Selection Register (R1PU)

	7	6	5	4	3	2	1	0	
R1PU	-	R1PU6	R1PU5	R1PU4	R1PU3	R1PU2	R1PU1	R1PU0	09h
initial value	0	1	1	1	1	1	1	1	
R/W	W	W	W	W	W	W	W	W	

R1 pull-up resistor control register (R1PU) is 7-bit register and can control pull-up on or off each bit, if corresponding port is selected as input.
If R1PU is selected as "0", pull-up is enabled and if selected as "1", it is disabled.
R1PU is write-only register and initialized as "7Fh" in reset state.
The pull-up is automatically disabled, if corresponding port is selected as output.

• R1 Open Drain Selection Register (R1OD)

	7	6	5	4	3	2	1	0	
R1OD	-	R1OD6	R1OD5	R1OD4	R1OD3	R1OD2	R1OD1	R1OD0	0Ah
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

R1 Open Drain Selection Register (R1OD) is 7-bit register, and can assign R1 port as open drain output port each bit If R1OD is selected as "0", port R1 is open drain output, and if selected as "1", it is push-pull output. R1OD is write-only register and initialized as "00h" in reset state.

• **R1 I/O Data Direction Register (R1DD)**

	7	6	5	4	3	2	1	0	
R1DD	-	R1DD6	R1DD5	R1DD4	R1DD3	R1DD2	R1DD1	R1DD0	0Bh
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

R1 I/O Data Direction Register (R1DD) is 7-bit register, and can assign input state or output state to each bit. If R1DD is "0", port R1 is in the input state, and if "1", it is in the output state. R1DD is write-only register. Since R1DD is initialized as "00h" in reset state, the whole port R1 becomes input state.

• **R1 Function Selection Register Low (R1FL)**

	7	6	5	4	3	2	1	0	
R1FL	R13FL		R12FL		R11FL		R10FL		0Ch
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

R1 Function Selection Register Low (R1FL) is 8-bit register, and can assign Key Scan pin or not. If R1FN is selected as "1", Key Scan function is enabled and if selected as "0", it is disabled. R1FN is write-only register and initialized as "00h" in reset state.

• **R1 Function Selection Register High (R1FH)**

	7	6	5	4	3	2	1	0	
R1FH	-		R16FH		R15FH		R14FH		0Dh
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

R1 Function Selection Register High (R1FH) is 6-bit register, and can assign Key Scan pin or not. If R1FN is selected as "1", Key Scan function is enabled and if selected as "0", it is disabled. R1FN is write-only register and initialized as "00h" in reset state.

Selection Mode of R1FL

Bit Name	Selection Mode		Remarks
R13FL	00	R13	
	01	KS11	
	10	T0	
	11	-	
R12FL	00	R12	
	01	KS10	
	10	INT1(EC1)	
	11	-	
R11FL	00	R11	
	01	KS9	
	10	INT0(EC0)	
	11	-	
R10FL	00	R10	
	01	KS8	
	10	-	
	11	-	

Selection Mode of R1FH

Bit Name	Selection Mode		Remarks
-	00	-	
	01	-	
	10	-	
	11	-	
R16FH	00	R16	*OSC2
	01	KS14	
	10	-	
	11	-	
R15FH	00	R15	*OSC1
	01	KS13	
	10	-	
	11	-	
R14FH	00	R14	
	01	KS12	
	10	T1	
	11	-	

• **R1 IOH/IOL Control Register Low (R1IL)**

	7	6	5	4	3	2	1	0	
R1IL	R13IL		R12IL		R11IL		R10IL		0Eh
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

• **R1 IOH/IOL Control Register High (R1IH)**

	7	6	5	4	3	2	1	0	
R1IH	-		R16IH		R15IH		R14IH		0Fh
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

Selection Mode of R1IL

Bit Name	Selection Mode		Remarks
		IOH/IOL	
R13IL	00	x1.0/x1.0	R13
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	
R12IL	00	x1.0/x1.0	R12
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	
R11IL	00	x1.0/x1.0	R11
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	
R10IL	00	x1.0/x1.0	R10
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	

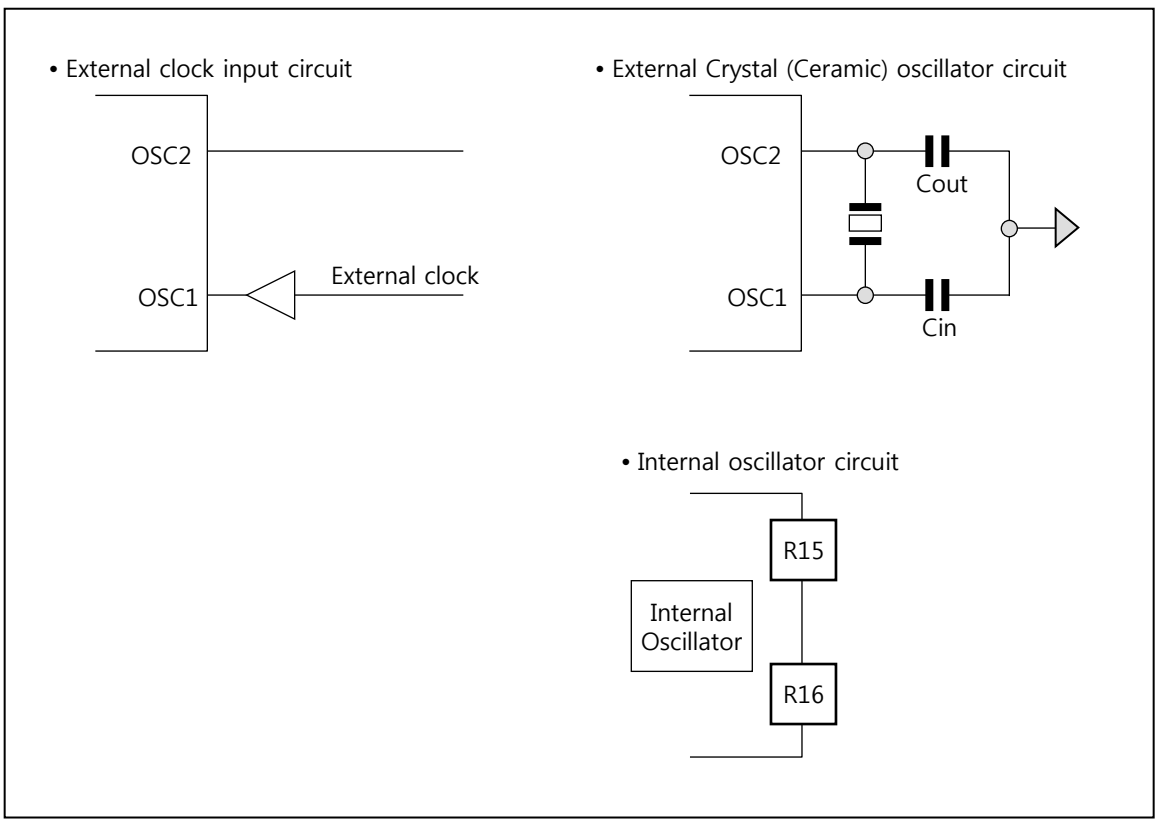
Selection Mode of R1IH

Bit Name	Selection Mode		Remarks
		IOH/IOL	
-	-	-	-
	-	-	
	-	-	
	-	-	
R16IH	00	x1.0/x1.0	R16
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	
R15IH	00	x1.0/x1.0	R15
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	
R14IH	00	x1.0/x1.0	R14
	01	x0.5/x0.5	
	10	x1.5/x1.5	
	11	x0.5/x1.5	

4.1. Oscillation Circuit

Oscillation circuit is designed to be used either with a ceramic resonator or crystal oscillator.
fig. shows circuit diagrams using a crystal (or ceramic) oscillator and external clock.
Clock from oscillation circuit makes CPU clock via clock pulse generator, and then provide peripheral hardware clock.
Alternately, the oscillator may be driven from an external source as shown is fig.
In the STOP mode, oscillation stop, OSC2 state goes to "High", OSC1 state goes to "Low", and built-in feed back resistor is disabled.

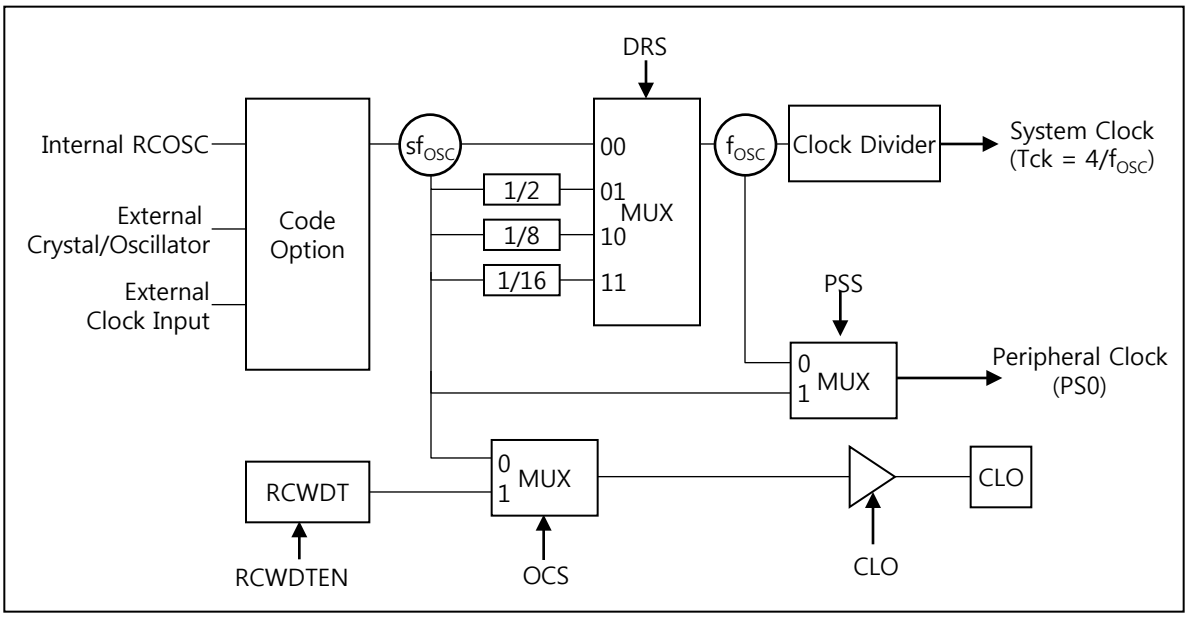
fig. Oscillator configuration



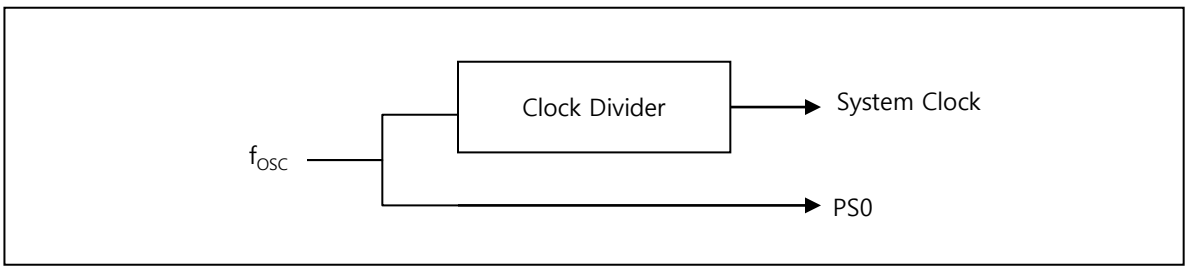
• Code Option (Oscillator Selection)

Name	Oscillator Type Selection	Option Value	R15 Assign	R16 Assign
XTS[2:0]	Internal RC 4MHz	111	R15	R16
	Internal RC 8MHz	110	R15	R16
	External Clock Input	101	OSC1	R16
	XT High Oscillator	100	OSC1	OSC2
	XT Low Oscillator	011	OSC1	OSC2
		010		
		001		
	Internal RC 16MHz	000	R15	R16

4.2. System Clock & Peripheral Clock Generator Block Diagram



4.3. System Clock Generator



• **System Control Register**

	7	6	5	4	3	2	1	0	
SCR	LVDOFF	RSTNF	OSCNF[1:0]		PSS	OCS	DRS1	DRS0	70h
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

Selection Mode of SCR

Bit Name		Selection Mode		Remarks
LVDOFF	LVD Disable	0	LVD Enable	
		1	LVD Disable	
RSTNF	RESETB Noise Filter Enable	0	Disable	
		1	Enable	
OSCNF[1:0]	OSC. Noise Filter Enable	00	x1	
		01	x2	
		10	x3	
		11	x4	
PSS	Peripheral Clock Selection	0	f_{OSC} to PS0	
		1	sf_{OSC} to PS0	
OCS	Output Clock Selection	0	sf_{OSC} Output	
		1	RCWDT Output	
DRS[1:0]	Divide Ratio Selection	00	sf_{OSC}	f_{OSC}
		01	$sf_{OSC}/2$	
		10	$sf_{OSC}/8$	
		11	$sf_{OSC}/16$	

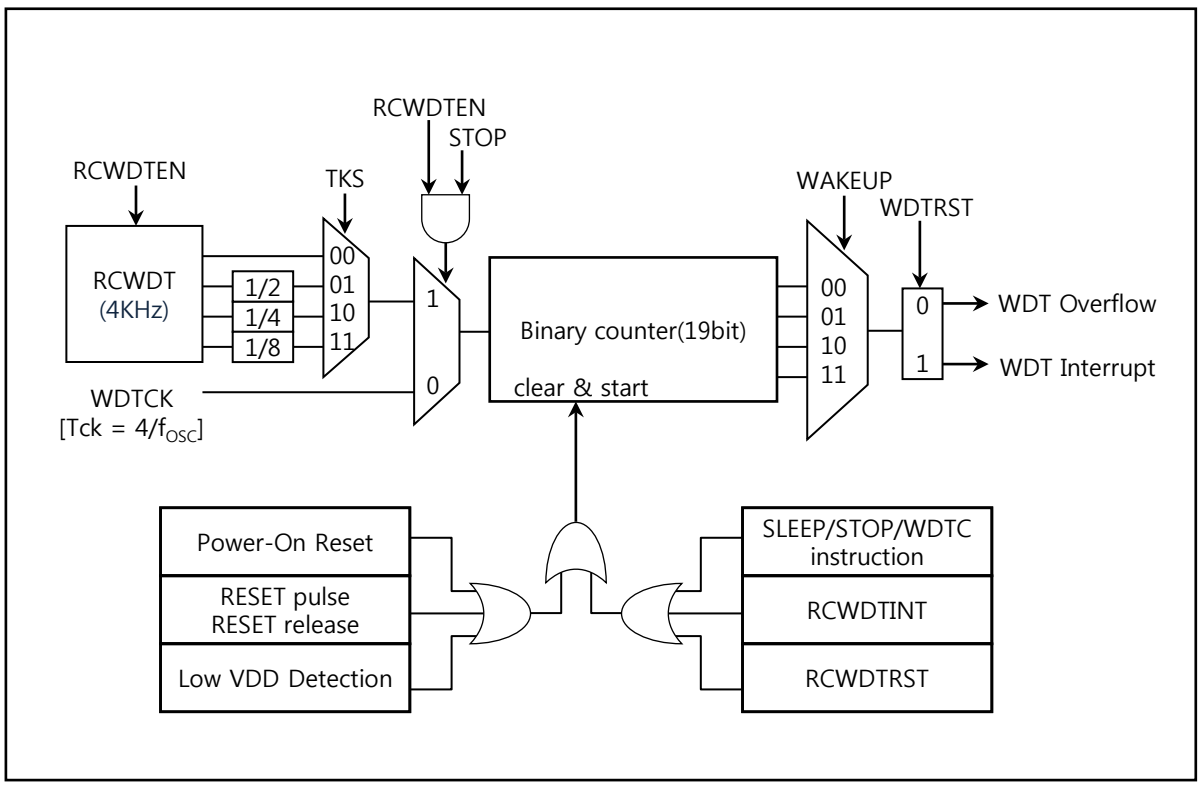
5.1. Watch Dog Timer (WDT)

Watch dog timer is organized binary of 19 steps. The signal of Tck cycle comes in the first step of WDT after WDT reset.
If this counter was overflowed, reset signal automatically come out so that internal circuit is initialized. The overflow time is 2^{19} × (Tck/2) (262.144ms at f_{OSC} = 4MHz) Normally, the binary counter must be reset before the overflow by using reset instruction (WDTC), Power-on reset pulse or Low VDD detection pulse.

* Tck = $4/f_{OSC}$

* It is constantly reset in STOP mode.
  When STOP is released by any stop release source, counting is restarted.
  After oscillation stabilization time 2^{15} × (Tck/2) [16.384ms at f_{OSC} = 4MHz],
  STOP is released.

Fig. Block Diagram of Watch-dog Timer



• Watch Dog Timer overflow priod is

2^{19} x (Tck/2)

where, Tck = $4/f_{OSC}$

• **WDT Control Register**

	7	6	5	4	3	2	1	0	
WDTR	TKS1	TKS0	KSEN	RCWDTEN	WDTRST	RCWDTDIS	WAKEUP1	WAKEUP0	72h
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of WDTR

Bit Name		Selection Mode			Remarks
		00	1us		(@4MHz)
TKS[1:0]	All Key Scan Time & WDT Clock Selection	00	Key Scan 16ms (*)	RCWDT 4KHz	at STOP mode
		01	8ms	8KHz	
		10	32ms	2KHz	
		11	64ms	1KHz	
KSEN	Key Scan Control at STOP mode	0	Disable		
		1	Enable		at STOP mode
RCWDTEN	RCWDT Mode Contol	0	WDT mode		
		1	RCWDT mode		at STOP mode
WDTRST	WDT Reset or Interrupt Control	0	WDT Reset		
		1	WDT Interrupt		
RCWDTDIS	RCWDT Oscillation Stop at LVD	0	free RUN		
		1	STOP RCWDT Osc.		at LVD mode
WAKEUP[1:0]	Reset or Interrupt Wakeup Time	00	(Tck/2) * 2^{19}		
		01	(Tck/2) * 2^{18}		
		10	(Tck/2) * 2^{17}		
		11	(Tck/2) * 2^{16}		

Reset or Interrupt Wakeup Time (f_{OSC})

(Tck = $4/f_{OSC}$ @4MHz)

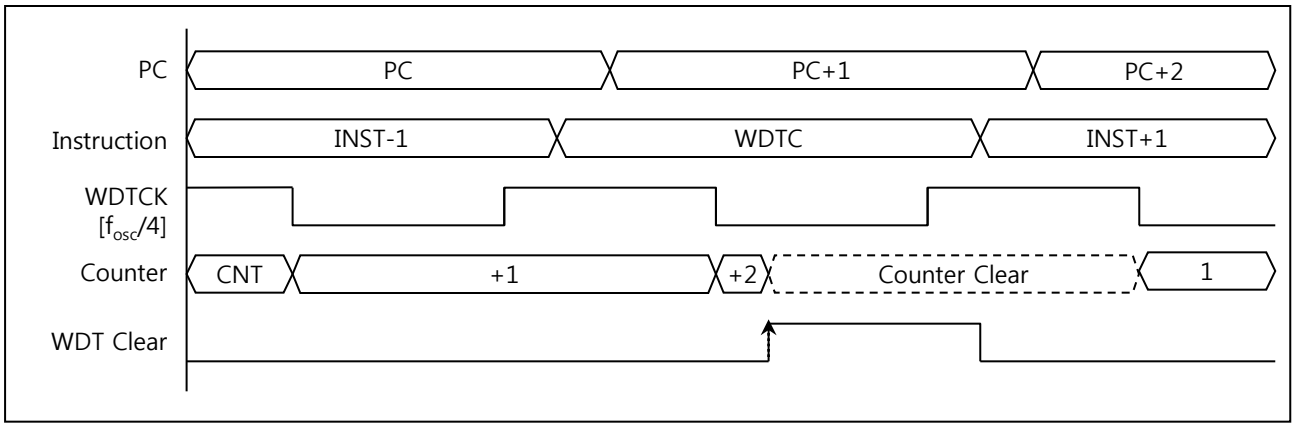
	(Tck/2) * 2^{19}	(Tck/2) * 2^{18}	(Tck/2) * 2^{17}	(Tck/2) * 2^{16}	Unit
Tck = 1us	262.144	131.072	65.536	32.768	ms

Reset or Interrupt Wakeup Time (f_{RCWDT})

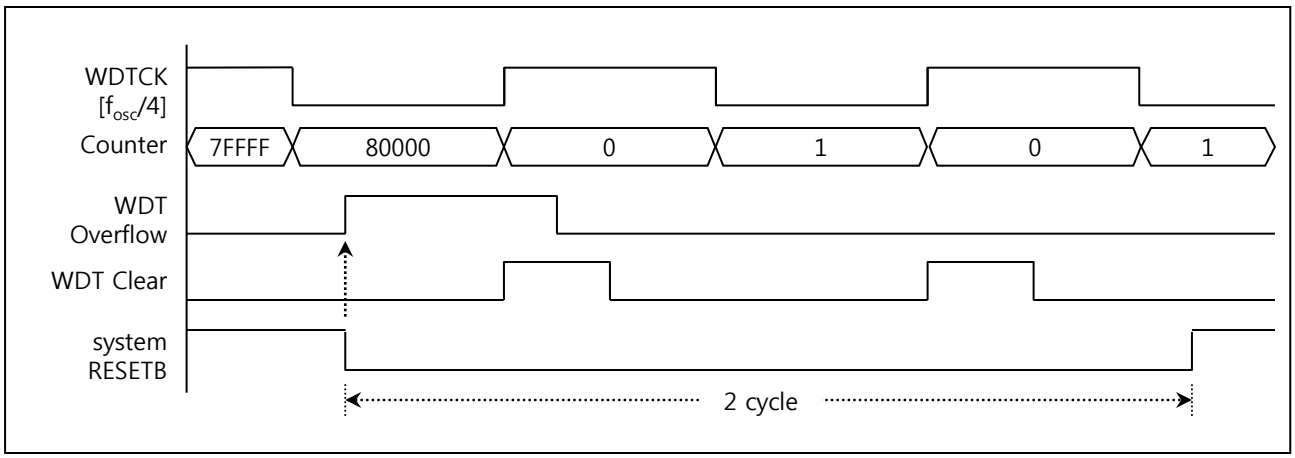
(T_{RCWDT})

	(T_{RCWDT}/2) * 2^{19}	(T_{RCWDT}/2) * 2^{18}	(T_{RCWDT}/2) * 2^{17}	(T_{RCWDT}/2) * 2^{16}	Unit
T_{RCWDT} ≒ 250us	≒ 64	≒ 32	≒ 16	≒ 8	s

* WDTC Timing Diagram



* Watch dog timer overflow RESET Timing Diagram



6.1. Timer

6.1.1. Timer operation mode

Timer is basically made of Timer Data/Counter Register, Timer Mode Register and control circuit.
The types of Timer are 16bit Timer/Counter (Timer0, Timer1).

Timer0	-. 16-bit Interval Timer -. 16-bit Event Counter -. 16-bit Capture Timer -. 16-bit rectangular-wave output -. 16-bit PWM output -. Buzzer output
Timer1	-. 16-bit Interval Timer -. 16-bit Event Counter -. 16-bit Capture Timer -. 16-bit rectangular-wave output -. 16-bit PWM output -. Buzzer output **-. 16-bit Carry Generator**

• **ROUT & Timer Output Sync. Control Register (RCR)**

	7	6	5	4	3	2	1	0	
RCR	TCKWDTRC	SYNCST	TOC	CRON	PR1	PR0	PRON	REM	40h
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

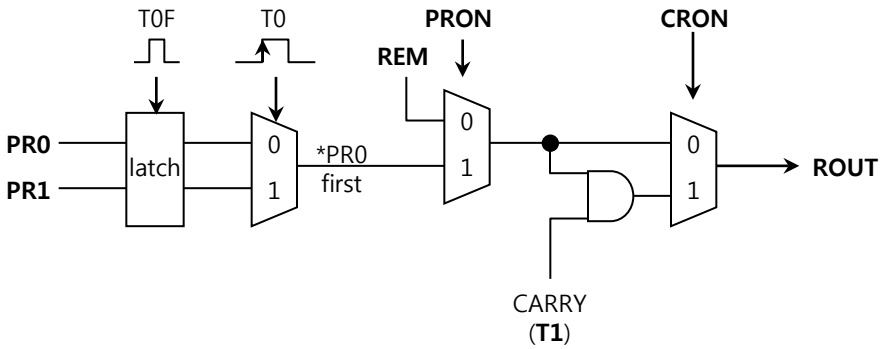
Selection Mode of RCR

Bit Name		Selection Mode		Remarks
TCKWDTRC	Timer Source Clock to WDTRC	0	Disable	
		1	Enable	
SYNCS	Sync. Timer Start Disable	0	Disable	
	Sync. Timer Start Enable	1	Depend on TOC	
TOC	Timer Output Control Disable	0	Normal Timer Mode (T0/T1) T0O ← T0 output T1O ← T1 output	
	Timer Output Control Enable by Timer0	1	Timer0 Mode (T0) T0O ← T0 output T1O ← T0 output inversion	
CRON	Carry Output Control	0	Output of ROUT without Timer 1 Pulse	
		1	Output of ROUT with Timer 1 Pulse	
PR1	Preset of ROUT Bit Control(When PRON=1)	0	ROUT 'L' on counting Timer0 DATA1	
		1	ROUT 'H' on counting Timer0 DATA1	
PR0	Preset of ROUT Bit Control(When PRON=1)	0	ROUT 'L' on counting Timer0 DATA0	
		1	ROUT 'H' on counting Timer0 DATA0	
PRON	PR0 / PR1 Function Control	0	PR0 / PR1 Function Disable ('REM' bit active)	
		1	PR0 / PR1 Function enable ('REM' bit inactive)	
REM	Output of Rout Bit Control (When PRON=0)	0	ROUT output low	Hi-Z (@N-Tr)
		1	ROUT output high	Low (@N-Tr)

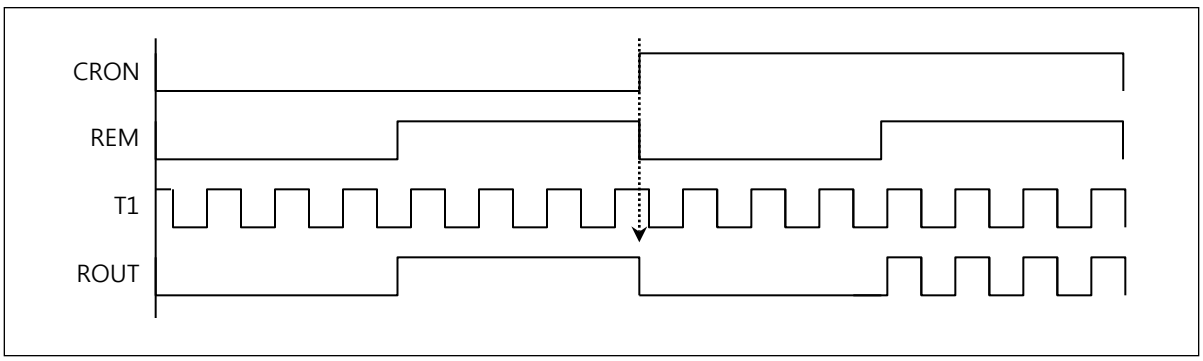
• **ROUT Output Control**

RCR

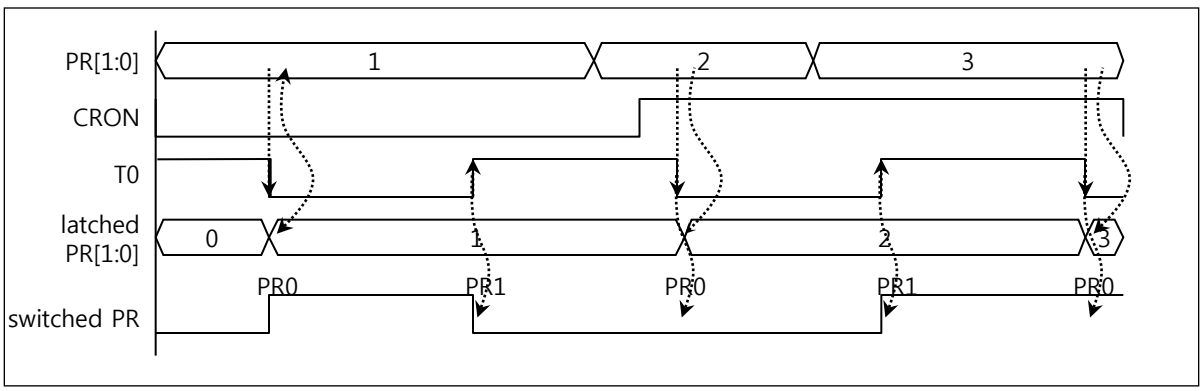
TCKWDTRC	CSYNCST	TOC	**CRON**	**PR1**	**PR0**	**PRON**	**REM**



• **REM mode Timing Diagram (at PRON = 0)**

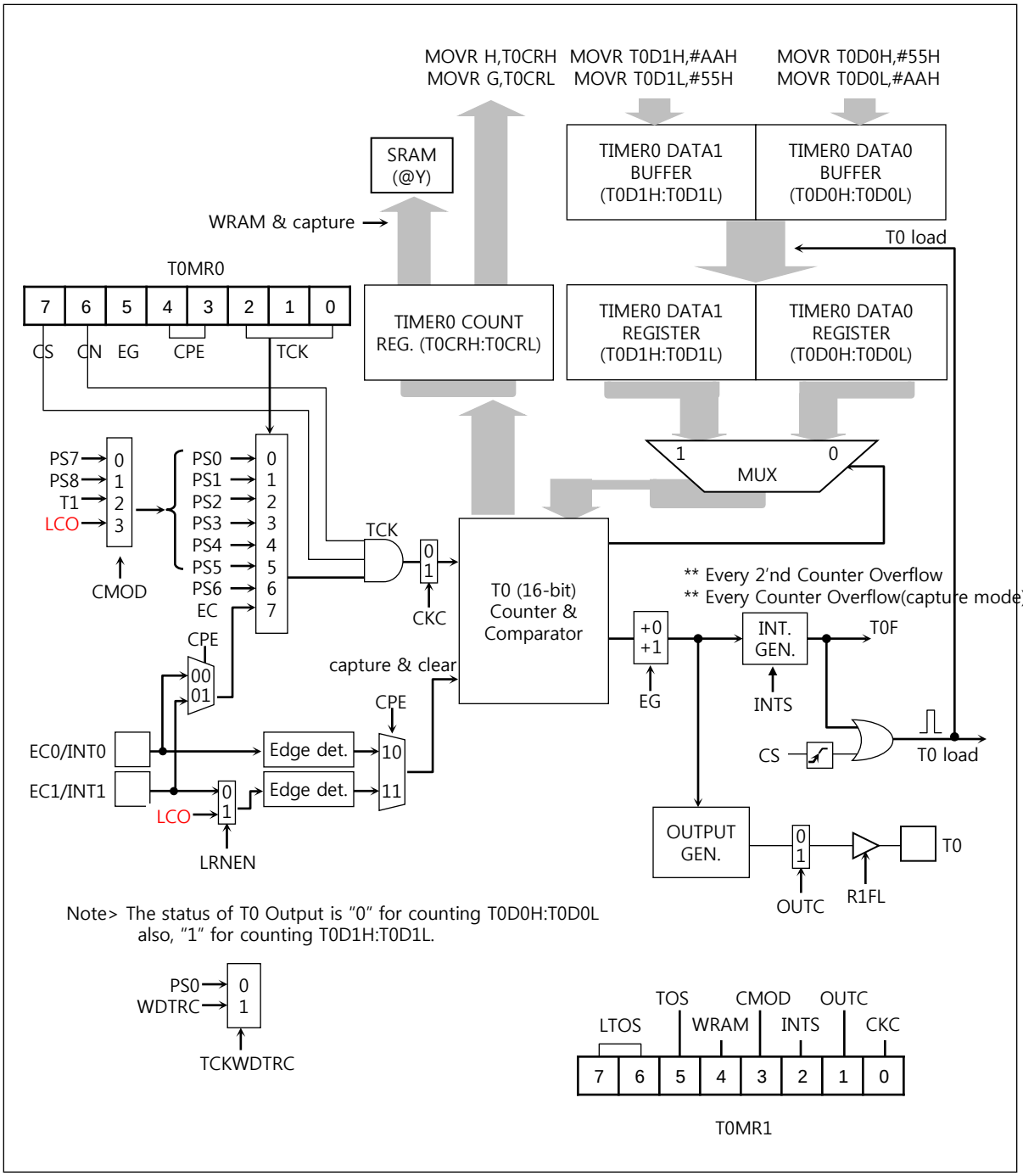


• **PR mode Timing Diagram (at PRON = 1)**



6.2. Timer0

6.2.1. Timer0(T0) Block Diagram



• **Timer0 Mode Register 0 (T0MR0)**

	7	6	5	4	3	2	1	0	
T0MR0	T0CS	T0CN	T0EG	T0CPE1	T0CPE0	T0CK2	T0CK1	T0CK0	41h
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of T0MR0

(f_{OSC} = 4MHz)

Bit Name			Selection Mode		Remarks
T0CS	Timer0 Clear / start Control	0	Timer0 Stop		
		1	Timer0 Clear and Start		
T0CN	Timer0 Pause / Continue Control	0	Timer0 Pause		
		1	Timer0 continue		
T0EG	Timer0 Count Control	0	Timer0 Count		
		1	Timer0 Count + 1		
T0CPE1 T0CPE0	Input capture & Event Count selection	00	EC0		
		01	EC1		
		10	Capture 0 (INT0)		
		11	Capture 1 (INT1)		
T0CK2 T0CK1 T0CK0	Input clock selection	000	PS0 (0.25us)	*PS7 (32us)	*CMOD
		001	PS1 (0.5us)	*PS8 (64us)	
		010	PS2 (1us)	*T1	
		011	PS3 (2us)	*LCO	
		100	PS4 (4us)		
		101	PS5 (8us)		
		110	PS6 (16us)		
		111	EC (EC0 or EC1)		

• **Timer0 Mode Register 1 (T0MR1)**

	7	6	5	4	3	2	1	0	
T0MR1	T0LTOS1	T0LTOS0	TOS0	WRAM0	CMOD0	INTS0	OUTC0	CKC0	42h
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of T0MR1

Bit Name			Selection Mode	Remarks
T0LTOS1 T0LTOS0	Logical Timer Output Selection	00	Logical 'AND' of Timer0 output and Timer1 output	
		01	Logical 'OR' of Timer0 output and Timer1 output	
		10	Logical 'NAND' of Timer0 output and Timer1 output	
		11	Logical 'NOR' of Timer0 output and Timer1 output	
TOS0	Timer/Logical-Timer Output Selection	0	Timer0 Output	
		1	Logical Timer Output	
WRAM0	Automatically Save Captured data to RAM	0	Disable	
		1	Timer0 Automatically Save Capture data to RAM	
CMOD0	Clock Source Change	0	Timer0 Normal Mode	
		1	Timer0 Clock Source Change	
INTS0	Timer0 Interrupt Overflow Control	0	Timer0 Interrupt Every 2nd Overflow	
		1	Timer0 Interrupt Every Overflow	
OUTC0	Timer0 Output Control	0	Timer0 Output Normal	
		1	Timer0 Output Reverse	
CKC0	Timer0 Input Clock Control	0	Timer0 Input Clock Normal	
		1	Timer0 Input Clock Reverse	

Note: Save 2bytes capture data to RAM (2cycle) - addressed by @Y++., T0CRL saved first.

SRAM(@Y)	0	1	2	3	4	5	6	7
	T0CRL	T0CRH	T0CRL	T0CRH	T0CRL	T0CRH	T0CRL	T0CRH
	1'st Captured Data		2'nd Captured Data		3'rd Captured Data		4'th Captured Data	

• **Timer0 Data0 Register Low (T0D0L)**

	7	6	5	4	3	2	1	0	
T0D0L	T0D0L7	T0D0L6	T0D0L5	T0D0L4	T0D0L3	T0D0L2	T0D0L1	T0D0L0	43h
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• **Timer0 Count Register Low (T0CRL)**

	7	6	5	4	3	2	1	0	
T0CRL	T0CRL7	T0CRL6	T0CRL5	T0CRL4	T0CRL3	T0CRL2	T0CRL1	T0CRL0	43h
initial value	-	-	-	-	-	-	-	-	
R/W	R	R	R	R	R	R	R	R	

Note: At 16bit counter value read(T0CRH:T0CRL), Must be read T0CRL.

• **Timer0 Data1 Register Low (T0D1L)**

	7	6	5	4	3	2	1	0	
T0D1L	T0D1L7	T0D1L6	T0D1L5	T0D1L4	T0D1L3	T0D1L2	T0D1L1	T0D1L0	44h
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• **Timer0 Data0 Register High (T0D0H)**

	7	6	5	4	3	2	1	0	
T0D0H	T0D0H7	T0D0H6	T0D0H5	T0D0H4	T0D0H3	T0D0H2	T0D0H1	T0D0H0	45h
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• **Timer0 Count Register High (T0CRH)**

	7	6	5	4	3	2	1	0	
T0CRH	T0CRH7	T0CRH6	T0CRH5	T0CRH4	T0CRH3	T0CRH2	T0CRH1	T0CRH0	45h
initial value	-	-	-	-	-	-	-	-	
R/W	R	R	R	R	R	R	R	R	

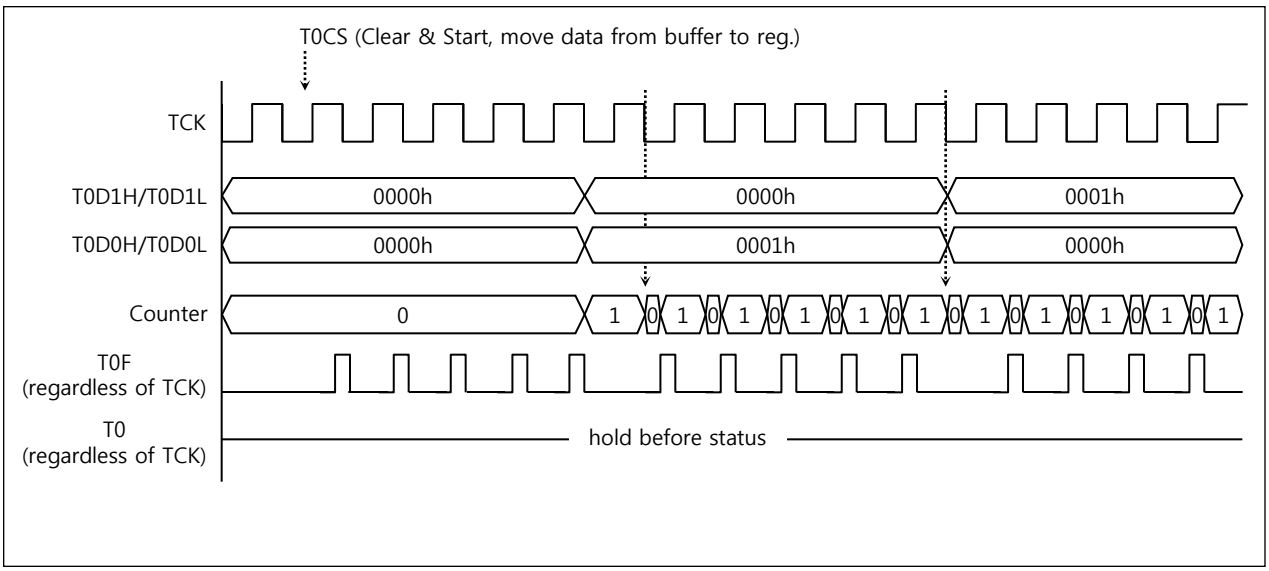
Note: At 16bit counter value read(T0CRH:T0CRL), Must be read T0CRL.

• **Timer0 Data1 Register High (T0D1H)**

	7	6	5	4	3	2	1	0	
T0D1H	T0D1H7	T0D1H6	T0D1H5	T0D1H4	T0D1H3	T0D1H2	T0D1H1	T0D1H0	46h
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

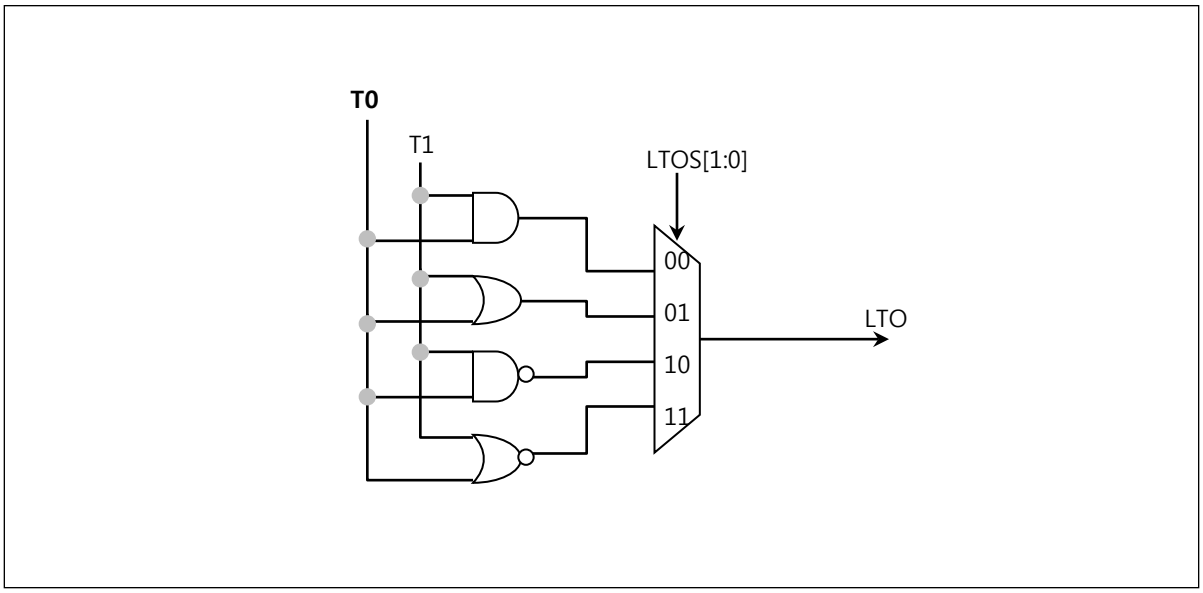
6.2.2. Timer0 Caution

• Caution : In the case of T0EG is "0",

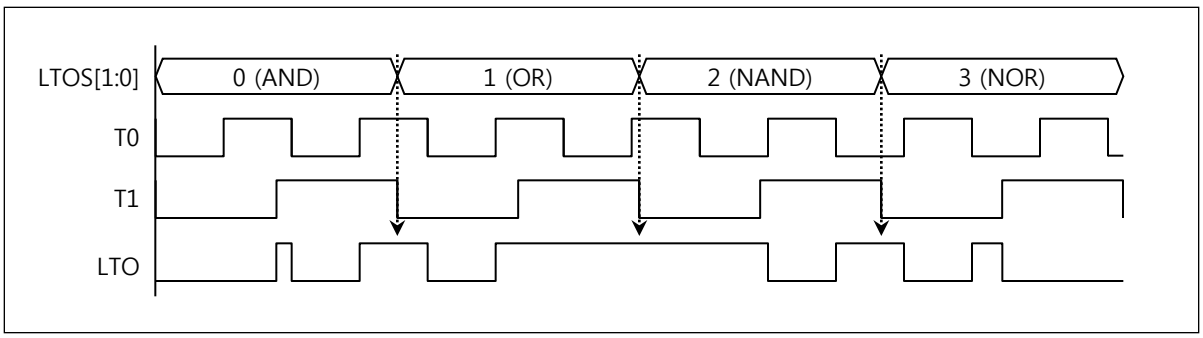


Want to count "0", set T0EG=1

* Logical Timer Output Control

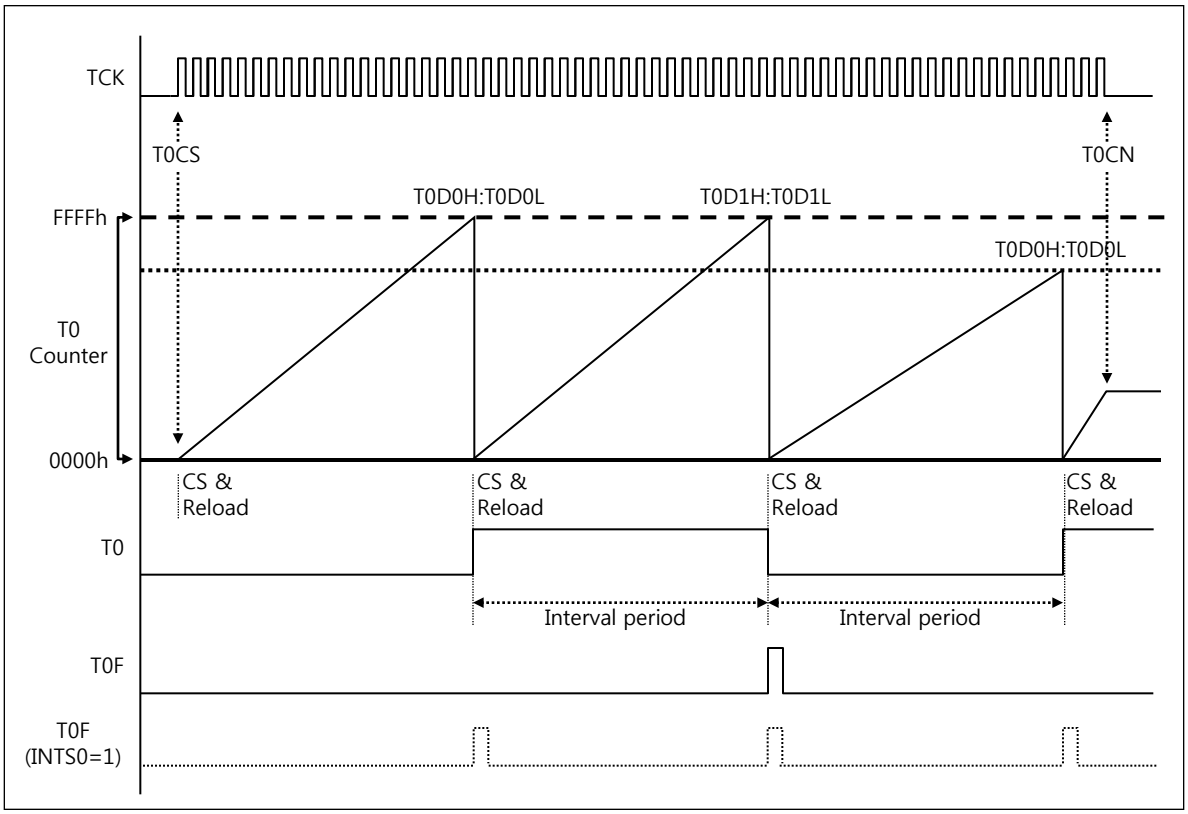


* Logical Timer Output mode Timing Diagram



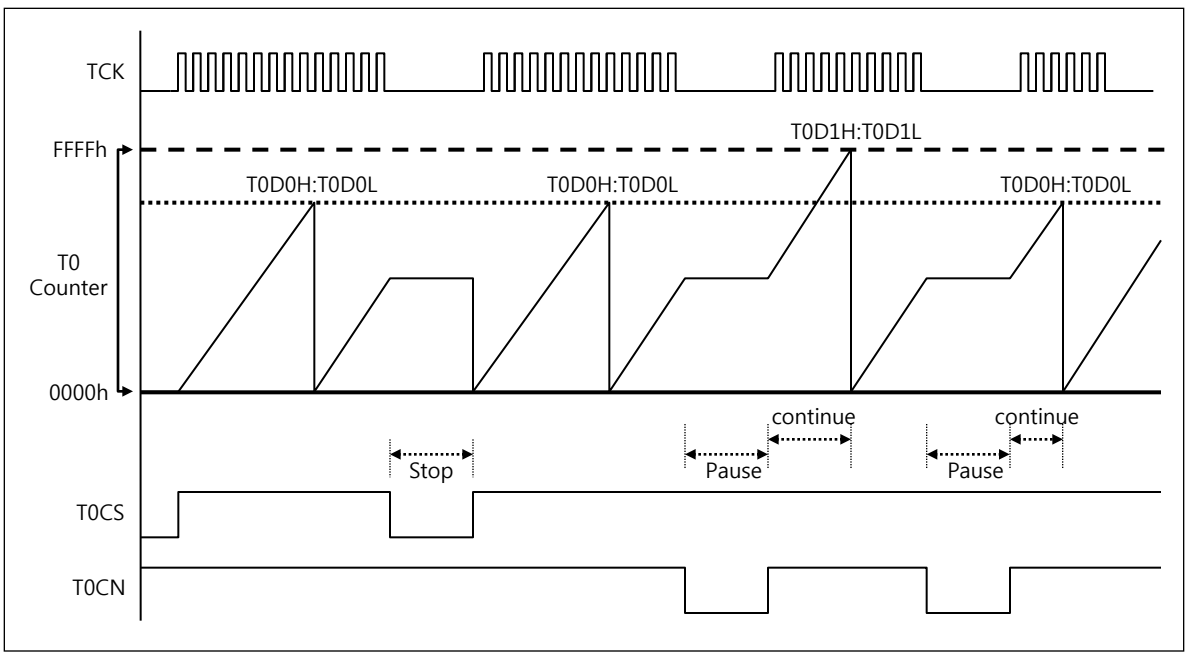
6.2.3. Timer0 Timing Diagram

* 16-bit Timer/Counter mode Timing Diagram

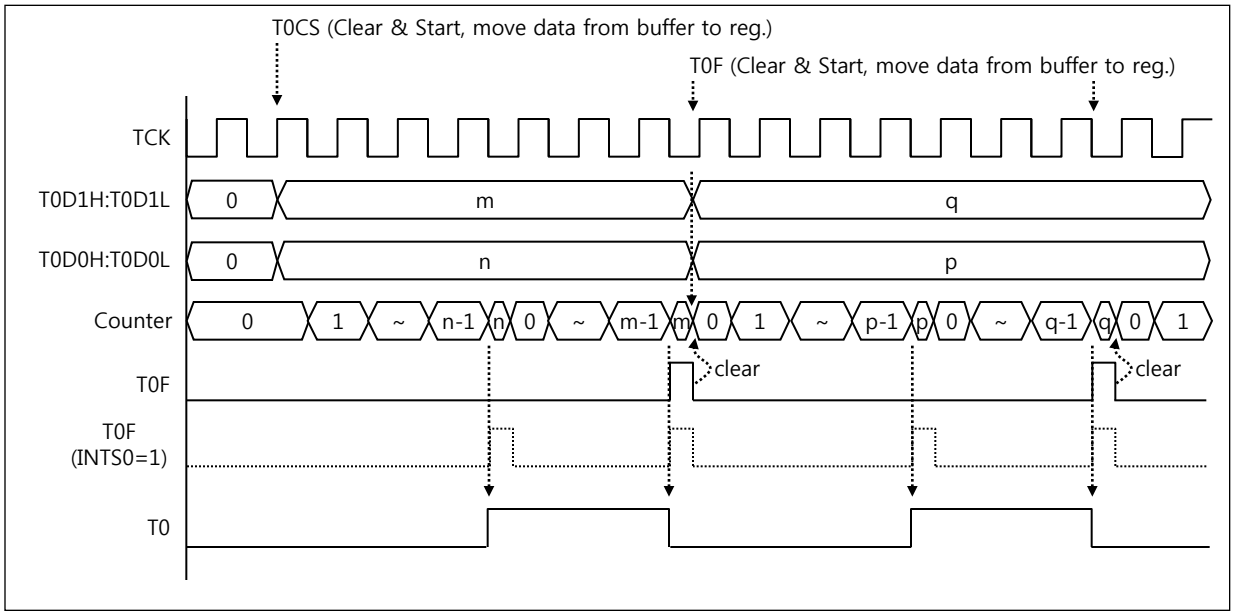


Note > CS : Timer0 Counter Clear & Start.
Reload : Timer0 Data move from Data buffer to Data register.

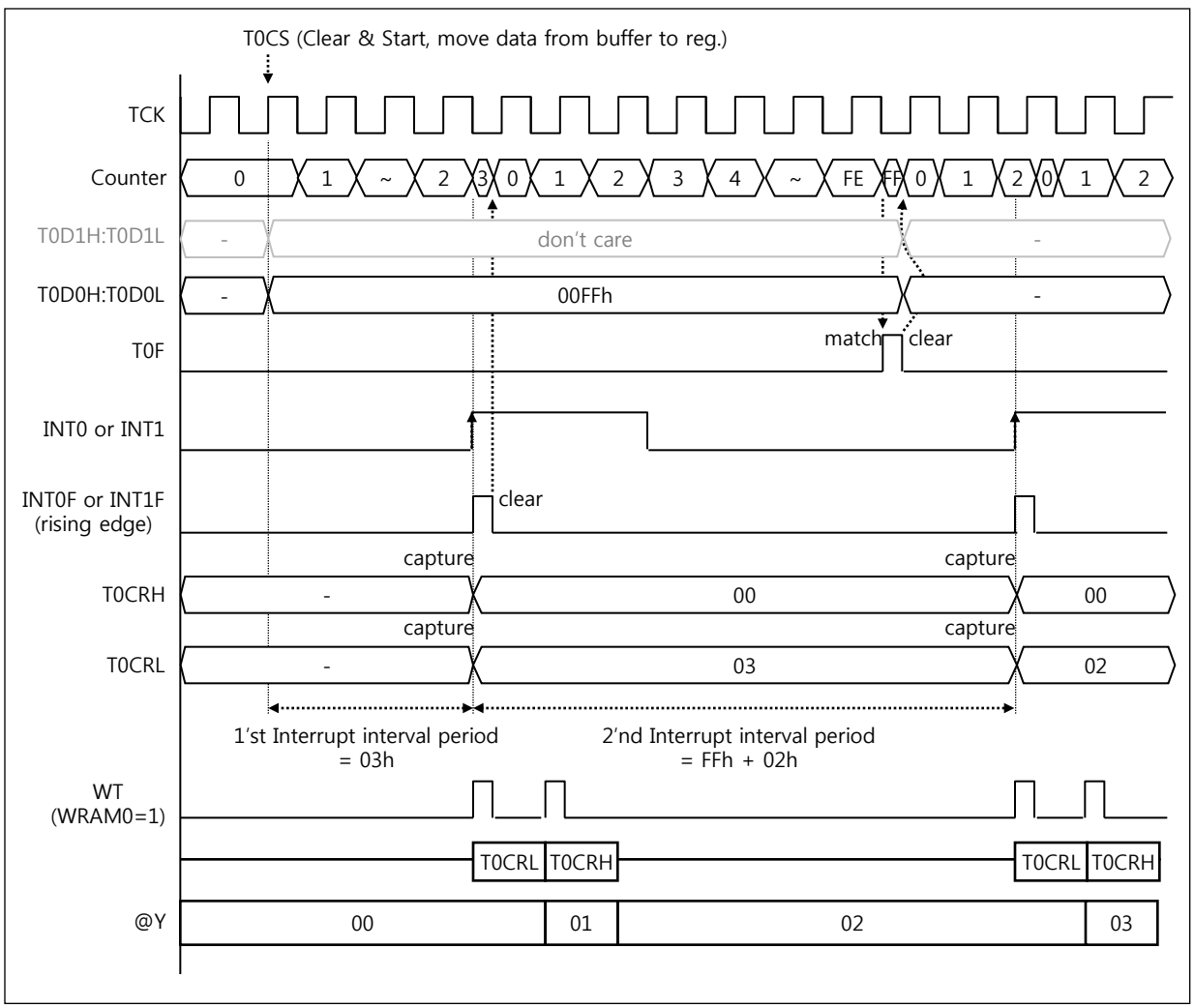
* Start / Stop operation



* 16-bit Timer/Counter mode Timing Diagram

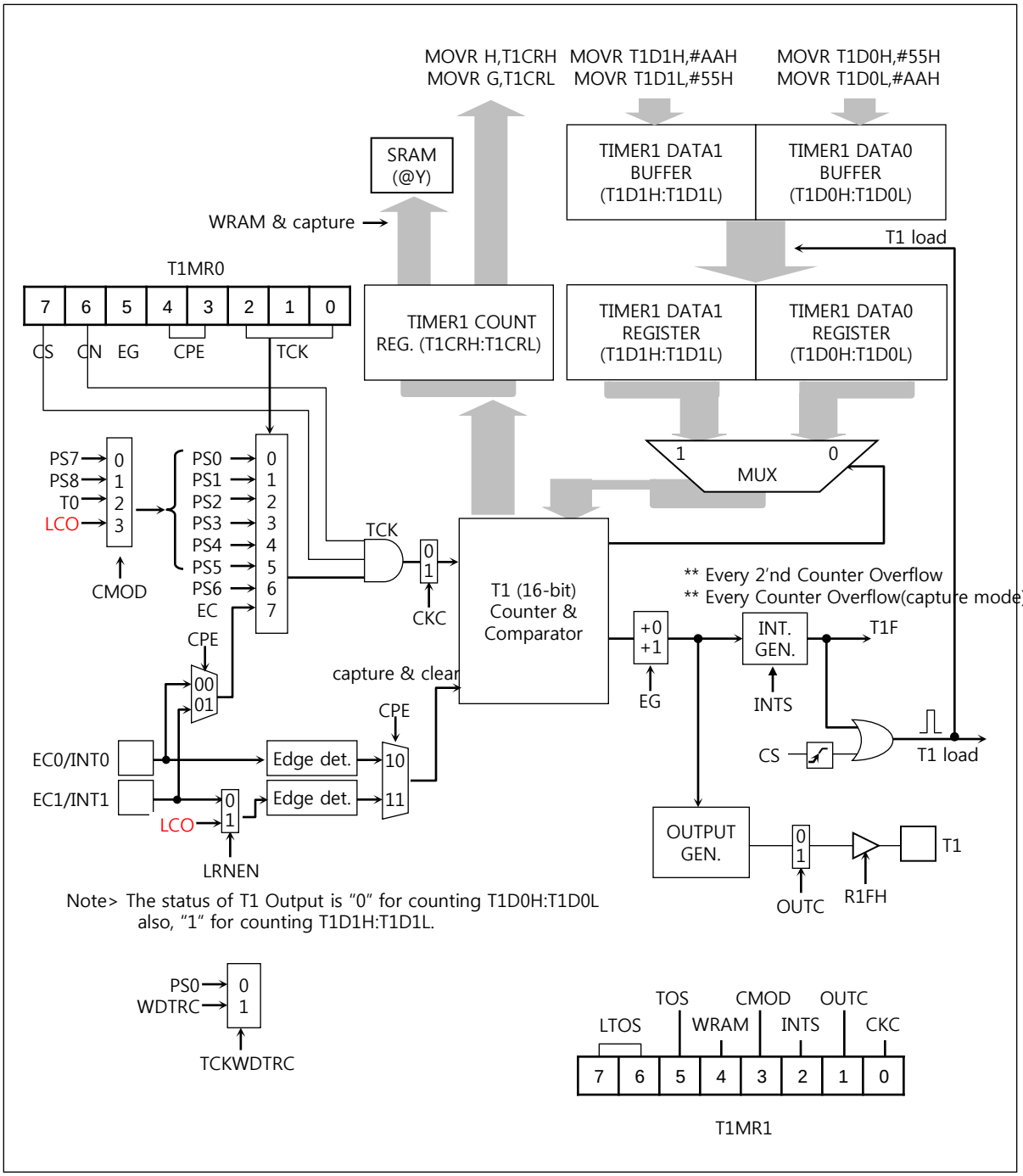


* 16-bit Capture mode Timing Diagram



6.2. Timer1

6.2.1. Timer1(T1) Block Diagram



• **Timer1 Mode Register 0 (T1MR0)**

	7	6	5	4	3	2	1	0	
T1MR0	T1CS	T1CN	T1EG	T1CPE1	T1CPE0	T1CK2	T1CK1	T1CK0	49h
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of T1MR0

(f_{OSC} = 4MHz)

Bit Name			Selection Mode		Remarks
T1CS	Timer1 Clear / start Control	0	Timer1 Stop		
		1	Timer1 Clear and Start		
T1CN	Timer1 Pause / Continue Control	0	Timer1 Pause		
		1	Timer1 continue		
T1EG	Timer1 Count Control	0	Timer1 Count		
		1	Timer1 Count + 1		
T1CPE1 T1CPE0	Input capture & Event Count selection	00	EC0		
		01	EC1		
		10	Capture 0 (INT0)		
		11	Capture 1 (INT1)		*Learning Circuit
T1CK2 T1CK1 T1CK0	Input clock selection	000	PS0 (0.25us)	*PS7 (32us)	*CMOD
		001	PS1 (0.5us)	*PS8 (64us)	
		010	PS2 (1us)	*T0	
		011	PS3 (2us)	*LCO	
		100	PS4 (4us)		
		101	PS5 (8us)		
		110	PS6 (16us)		
		111	EC (EC0 or EC1)		

• **Timer1 Mode Register 1 (T1MR1)**

	7	6	5	4	3	2	1	0	
T1MR1	T1LTOS1	T1LTOS0	TOS1	WRAM1	CMOD1	INTS1	OUTC1	CKC1	4Ah
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of T1MR1

Bit Name			Selection Mode	Remarks
T1LTOS1 T1LTOS0	Logical Timer Output Selection	00	Logical 'AND' of Timer1 output and Timer1 output	
		01	Logical 'OR' of Timer1 output and Timer1 output	
		10	Logical 'NAND' of Timer1 output and Timer1 output	
		11	Logical 'NOR' of Timer1 output and Timer1 output	
TOS1	Timer/Logical-Timer Output Selection	0	Timer1 Output	
		1	Logical Timer Output	
WRAM1	Automatically Save Captured data to RAM	0	Disable	
		1	Timer1 Automatically Save Capture data to RAM	
CMOD1	Clock Source Change	0	Timer1 Normal Mode	
		1	Timer1 Clock Source Change	
INTS1	Timer1 Interrupt Overflow Control	0	Timer1 Interrupt Every 2nd Overflow	
		1	Timer1 Interrupt Every Overflow	
OUTC1	Timer1 Output Control	0	Timer1 Output Normal	
		1	Timer1 Output Reverse	
CKC1	Timer1 Input Clock Control	0	Timer1 Input Clock Normal	
		1	Timer1 Input Clock Reverse	

Note: Save 2bytes capture data to RAM (2cycle) - addressed by @Y++., T1CRL saved first.

SRAM(@Y)	0	1	2	3	4	5	6	7
	T1CRL	T1CRH	T1CRL	T1CRH	T1CRL	T1CRH	T1CRL	T1CRH
	1'st Captured Data		2'nd Captured Data		3'rd Captured Data		4'th Captured Data	

• **Timer1 Data0 Register Low (T1D0L)**

	7	6	5	4	3	2	1	0	
T1D0L	T1D0L7	T1D0L6	T1D0L5	T1D0L4	T1D0L3	T1D0L2	T1D0L1	T1D0L0	4Bh
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• **Timer1 Count Register Low (T1CRL)**

	7	6	5	4	3	2	1	0	
T1CRL	T1CRL7	T1CRL6	T1CRL5	T1CRL4	T1CRL3	T1CRL2	T1CRL1	T1CRL0	4Bh
initial value	-	-	-	-	-	-	-	-	
R/W	R	R	R	R	R	R	R	R	

Note: At 16bit counter value read(T1CRH:T1CRL), Must be read T1CRL.

• **Timer1 Data1 Register Low (T1D1L)**

	7	6	5	4	3	2	1	0	
T1D1L	T1D1L7	T1D1L6	T1D1L5	T1D1L4	T1D1L3	T1D1L2	T1D1L1	T1D1L0	4Ch
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• **Timer1 Data0 Register High (T1D0H)**

	7	6	5	4	3	2	1	0	
T1D0H	T1D0H7	T1D0H6	T1D0H5	T1D0H4	T1D0H3	T1D0H2	T1D0H1	T1D0H0	4Dh
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

• **Timer1 Count Register High (T1CRH)**

	7	6	5	4	3	2	1	0	
T1CRH	T1CRH7	T1CRH6	T1CRH5	T1CRH4	T1CRH3	T1CRH2	T1CRH1	T1CRH0	4Dh
initial value	-	-	-	-	-	-	-	-	
R/W	R	R	R	R	R	R	R	R	

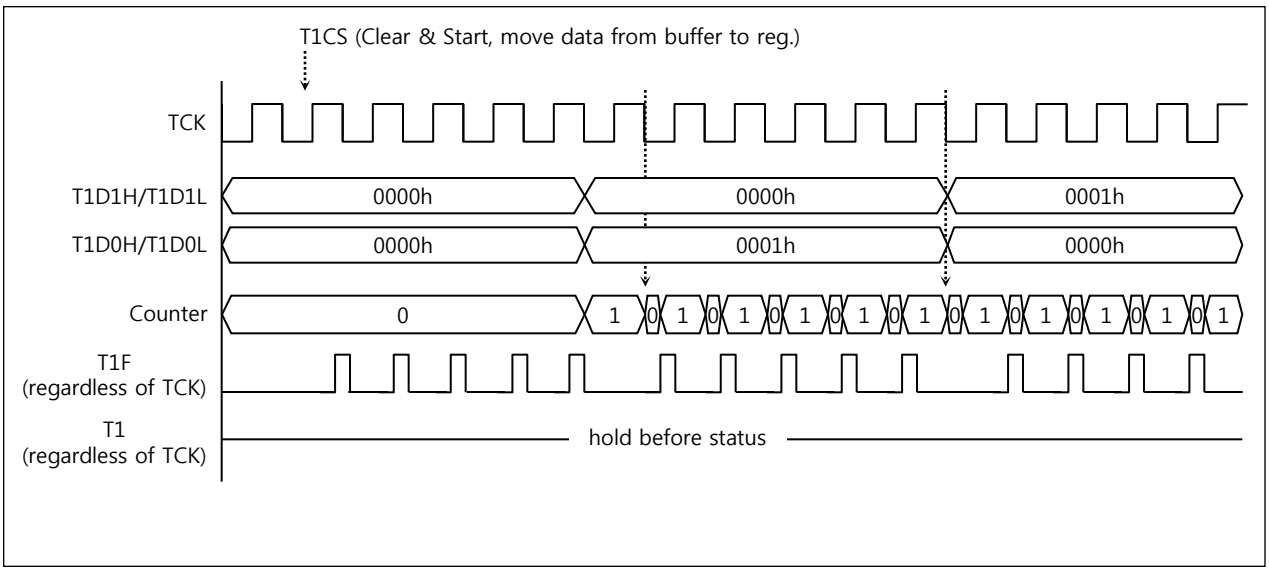
Note: At 16bit counter value read(T1CRH:T1CRL), Must be read T1CRL.

• **Timer1 Data1 Register High (T1D1H)**

	7	6	5	4	3	2	1	0	
T1D1H	T1D1H7	T1D1H6	T1D1H5	T1D1H4	T1D1H3	T1D1H2	T1D1H1	T1D1H0	4Eh
initial value	-	-	-	-	-	-	-	-	
R/W	W	W	W	W	W	W	W	W	

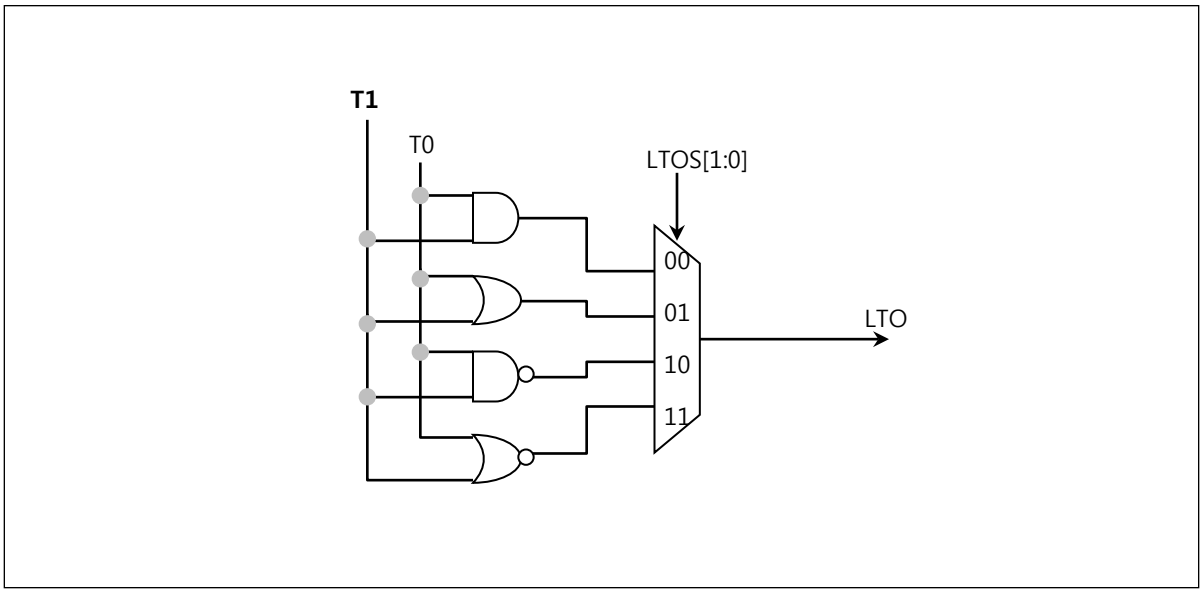
6.2.2. Timer1 Caution

• Caution : In the case of T1EG is "0",

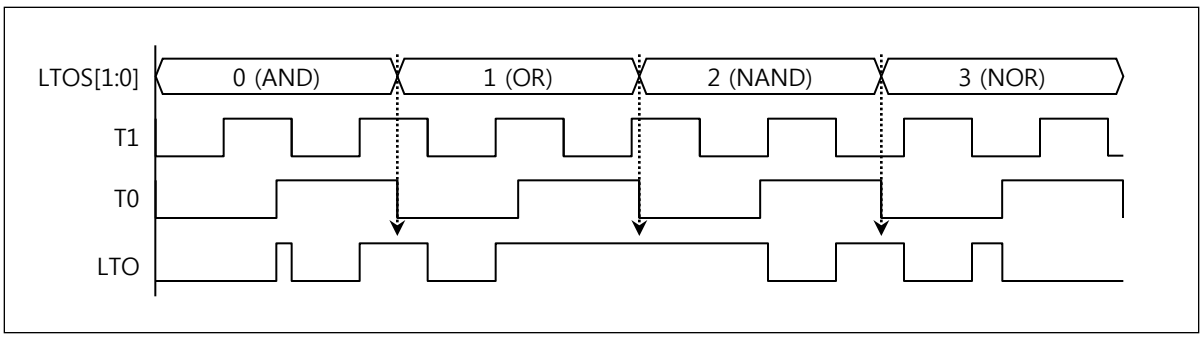


Want to count "0", set T1EG=1

* Logical Timer Output Control

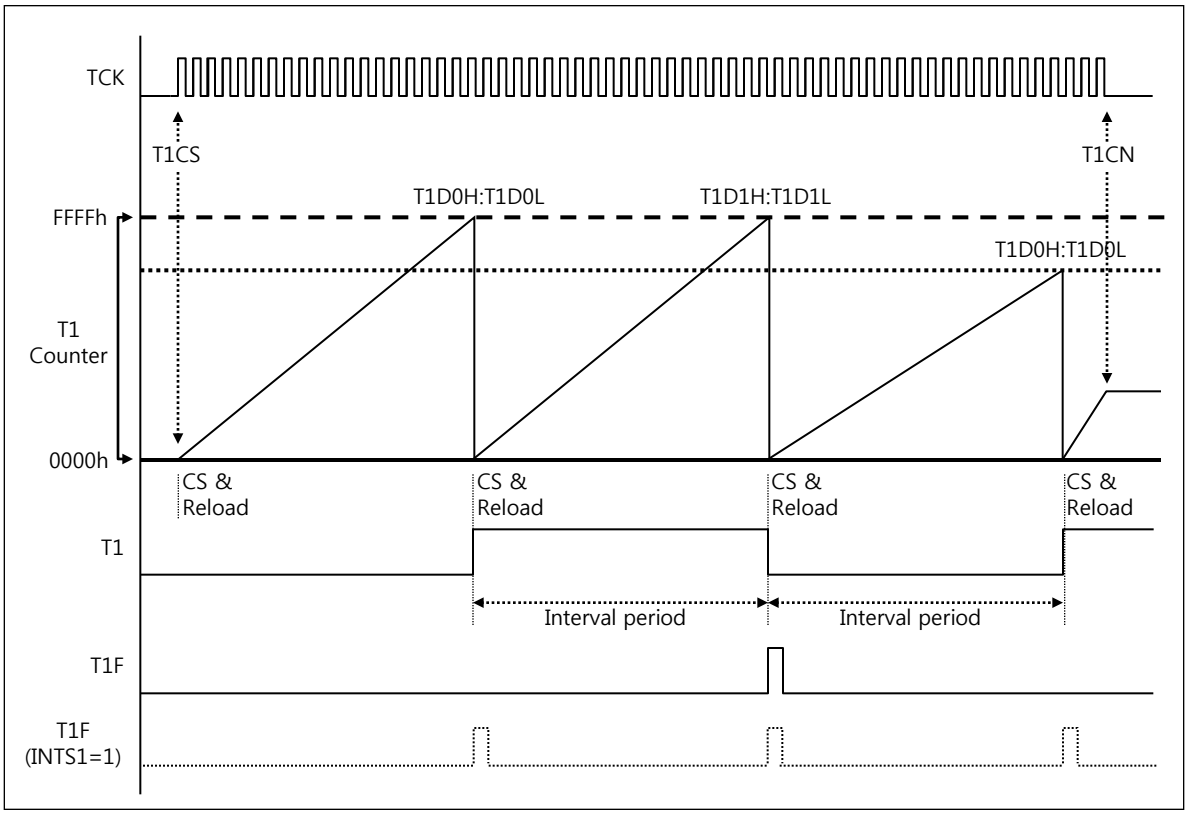


* Logical Timer Output mode Timing Diagram



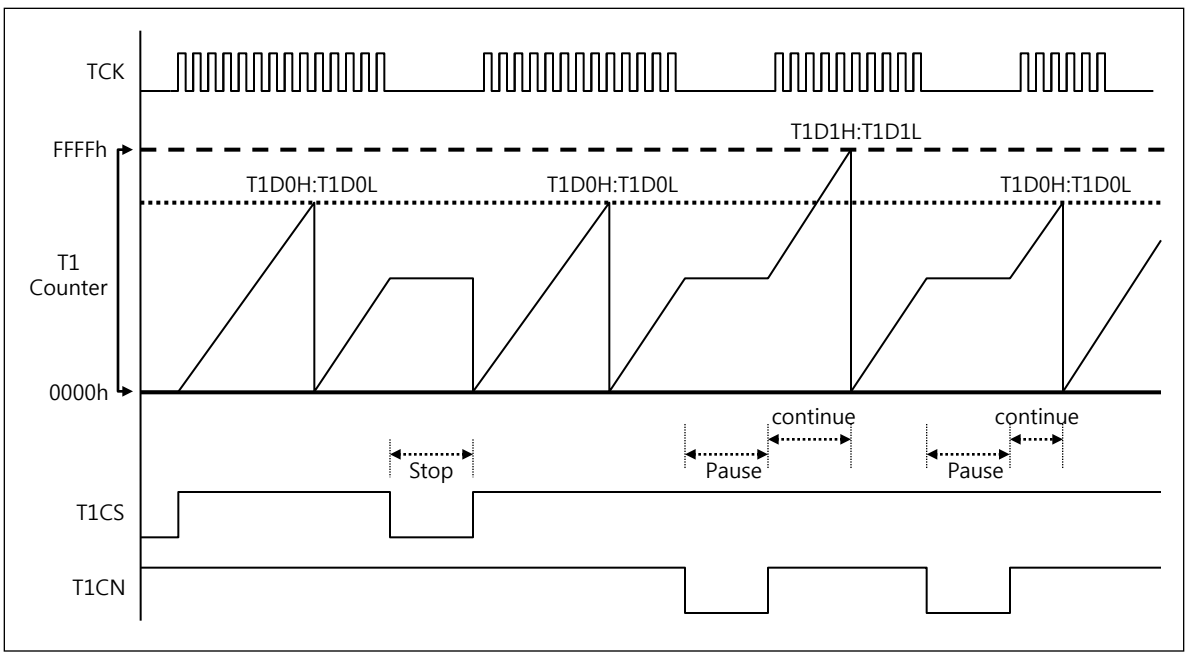
6.2.3. Timer1 Timing Diagram

* 16-bit Timer/Counter mode Timing Diagram

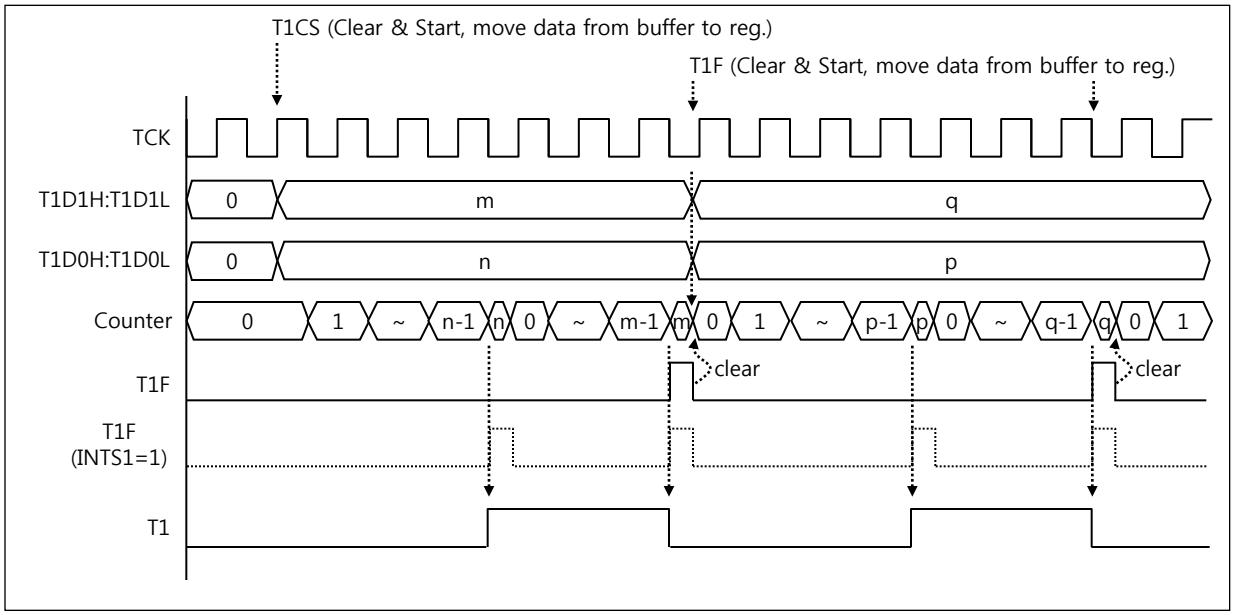


Note > CS : Timer1 Counter Clear & Start.
Reload : Timer1 Data move from Data buffer to Data register.

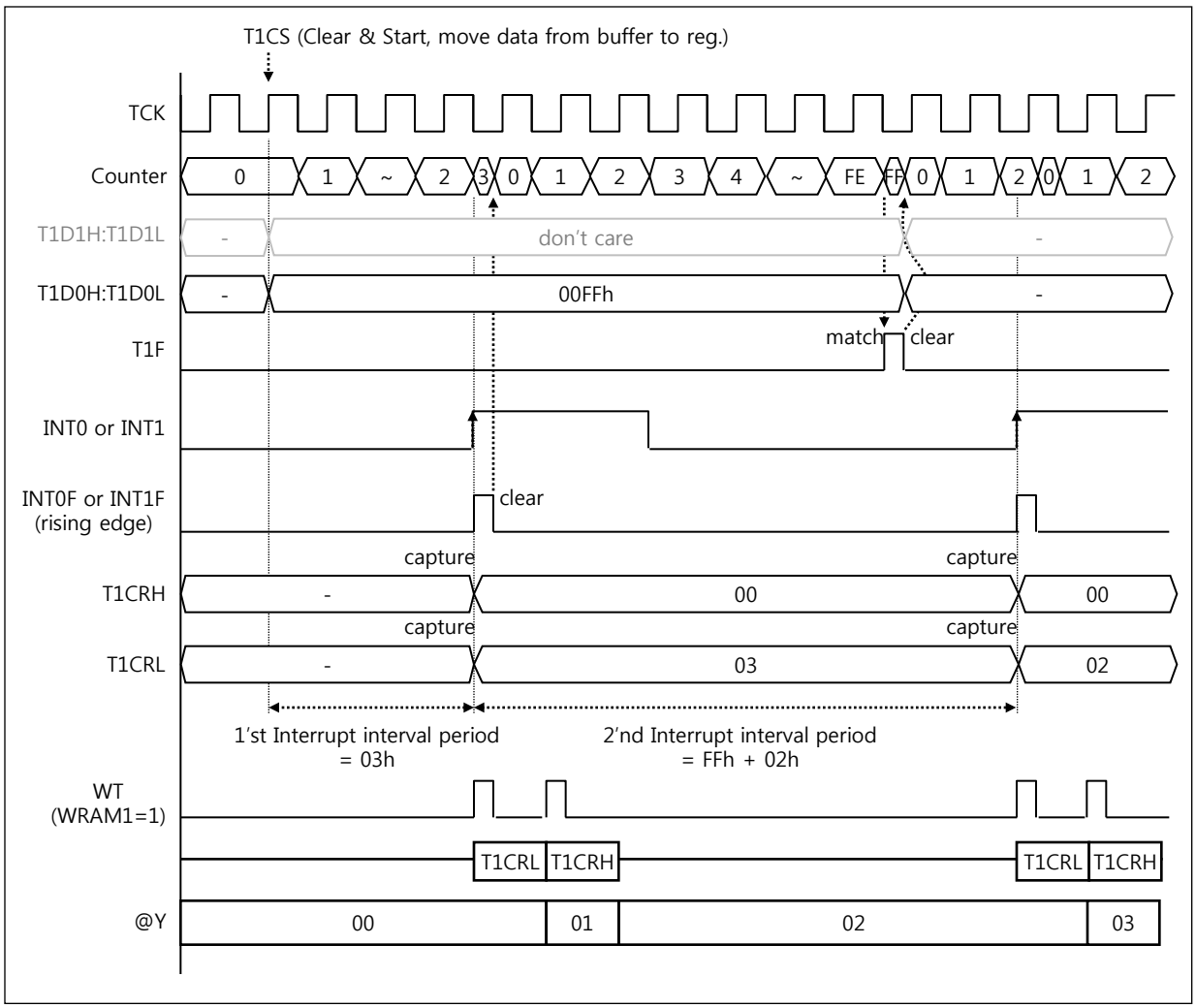
* Start / Stop operation



* 16-bit Timer/Counter mode Timing Diagram

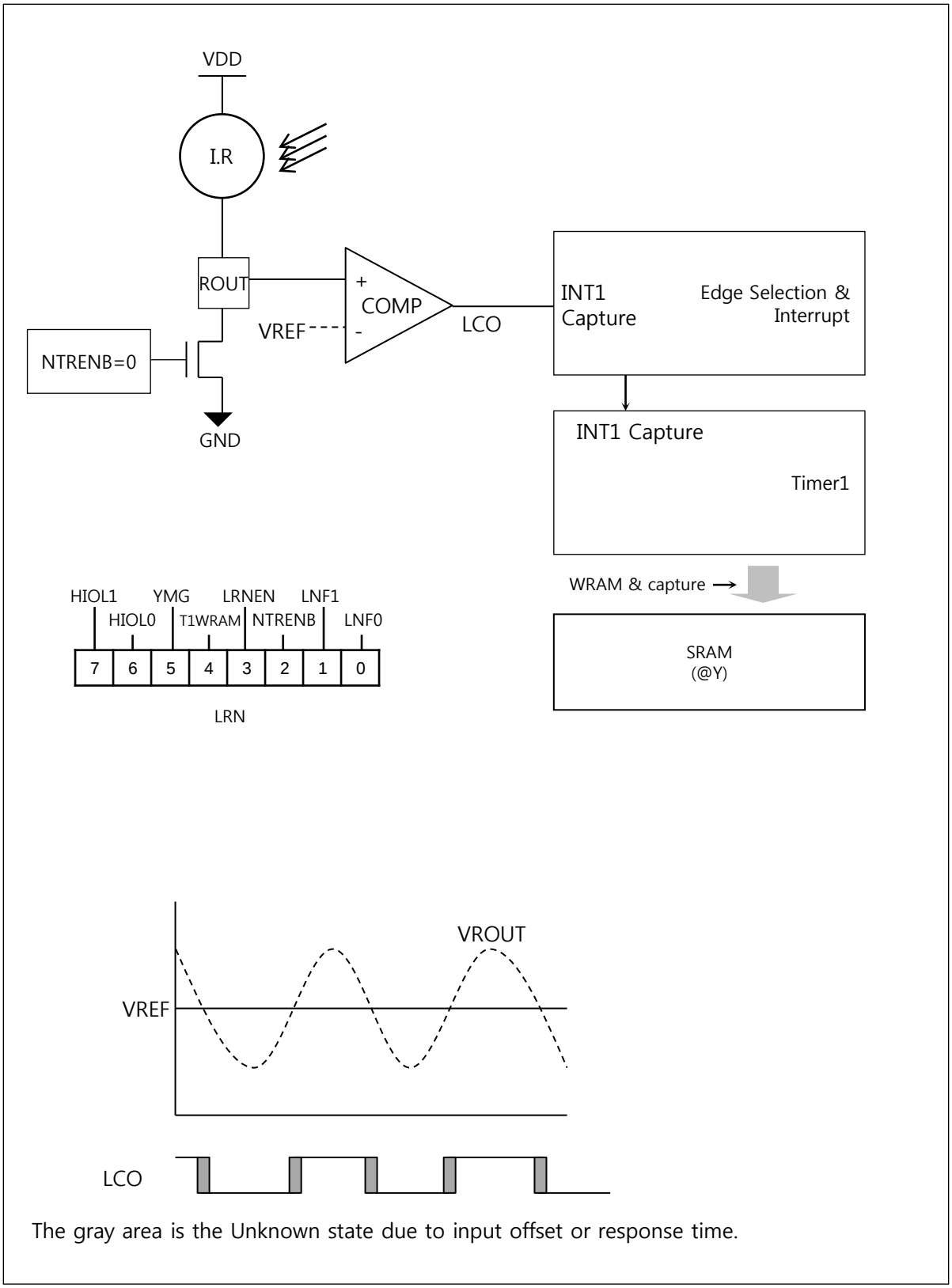


* 16-bit Capture mode Timing Diagram



8.1. Block Diagram

8.1.1. Block Diagram



The gray area is the Unknown state due to input offset or response time.

• **Learning Mode Register (LRN)**

	7	6	5	4	3	2	1	0	
LRN	RIOL1	RIOL0	YMG	T1WRAM	LRNEN	NTRENB	LNF1	LNF0	73h
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of LRN

Bit Name			Selection Mode	Remarks
RIOL1 RIOL0	ROUT IOL Control	00	x3	
		01	x2.5	
		10	x2	
		11	x1.5	
YMG	SRAM Page YMG Enable	0	Disable (reset YMG)	
		1	Enable	
T1WRAM	Automatically Save Captured data to RAM	0	2byte Capture Data	Only Timer1
		1	1byte Capture Data	
LRNEN	Learning Circuit Enable	0	Disable	
		1	Enable	
NTRENB	ROUT Driver TR. Selection	0	N-MOS Open Drain	
		1	Push-Pull	
LNF1 LNF0	Learning Detector noise canceller Selectionn.	00	200ns	
		01	100ns	
		10	40ns	
		11	10ns	

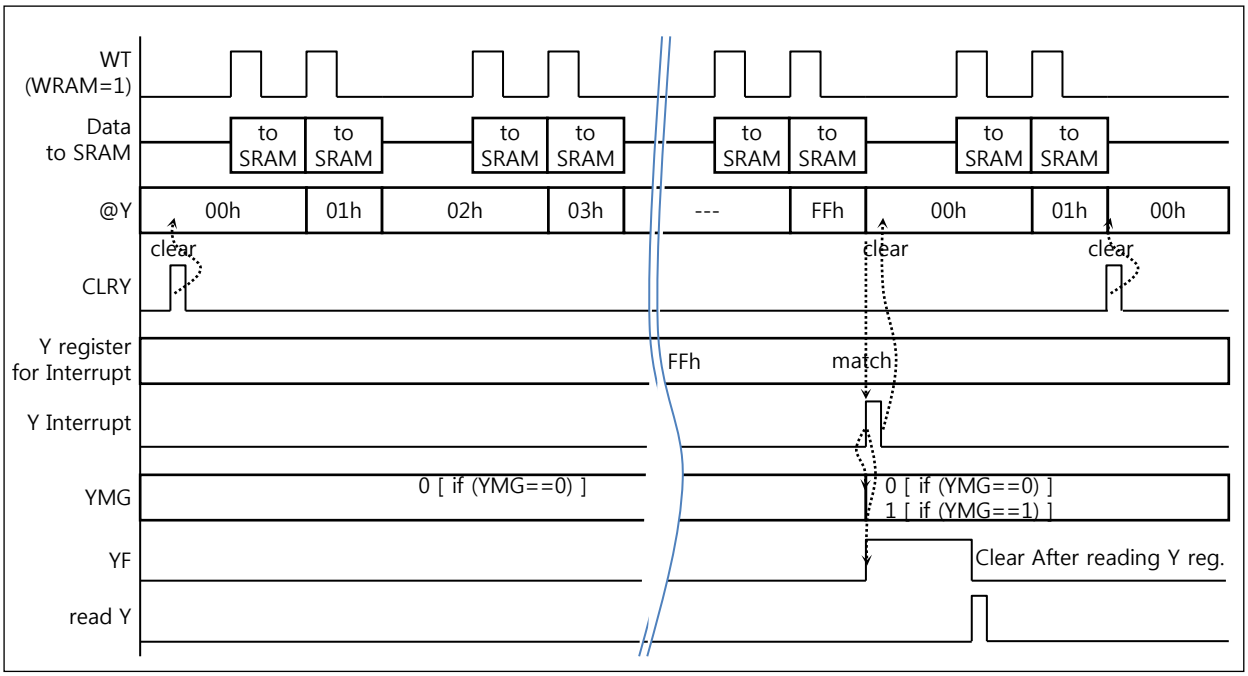
Note: Save 2bytes capture data to RAM (2cycle) - addressed by @Y++., T1CRL saved first.

SRAM(@Y)	0	1	2	3	4	5	6	7
	T1CRL	T1CRH	T1CRL	T1CRH	T1CRL	T1CRH	T1CRL	T1CRH
	1'st Captured Data		2'nd Captured Data		3'rd Captured Data		4'th Captured Data	

Note: Save 1bytes data to SRAM (1cycle) - addressed by @Y++.

SRAM(@Y)	0	1	2	3	4	5	6	→
	T1CRL	T1CRL	T1CRL	T1CRL	T1CRL	T1CRL	T1CRL	T1CRL

• **Y Interrupt Timing Diagram**



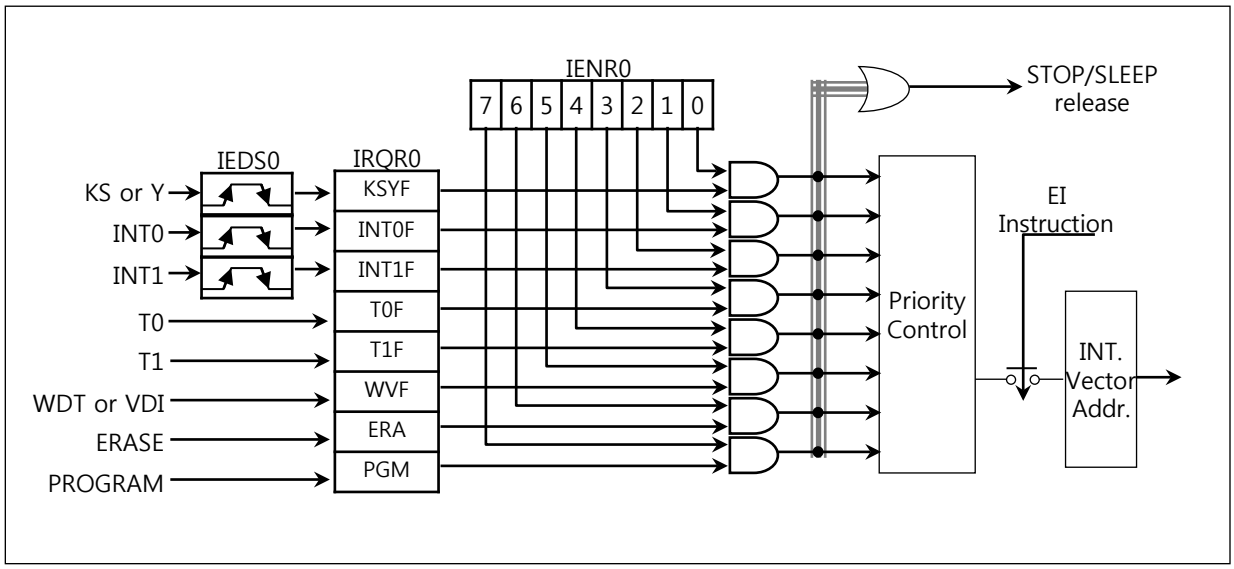
9. Interrupt

The ADAM85F contains 11 interrupt sources; 3 externals and 8 internals.
Nested interrupt services with priority control is also possible.

- 8 interrupt source (KS, INT0, INT1, T0, T1, Y, WDT, VDI)
- 6 interrupt vector
- 8 level nested interrupt control is possible.
- Read of interrupt request flag are possible.
- In interrupt accept, request flag is automatically cleared.

Interrupt Enable Register (IENR0), Interrupt Request Register (IRQR0) and priority circuit.
Interrupt function block diagram is shown in fig.

fig. Interrupt Source



9.1. Interrupt Source

Each interrupt vector is independent and has its own priority.

After internal reset is released, RESET vector Address is 0000h thus program start point should be defined as follows (also interrupt):

Table. Interrupt Source

	Mask	Priority	Interrupt Source	INT Vector Addr.
Hardware Interrupt	Non-maskable	0	RESET	0000h
	maskable	1	KS (Key Scan Interrupt) Y (Y register Overflow Interrupt)	0002h
		2	INT0 (External 0 Interrupt)	0004h
		3	INT1 (External 1 Interrupt)	0006h
		4	T0 (Timer0 Interrupt)	0008h
		5	T1 (Timer1 Interrupt)	000Ah
		6	WDT (Watch-Dog Timer) or VDI (Voltage Detection Indicator)	000Ch
		7	ERA (Erase Interrupt)	000Eh
		8	PGM (Program Interrupt)	0010h
		9	-	-
		10	-	-
		11	-	-
		12	-	-
		13	-	-
		14	-	-
		15	-	-
		16	-	-

Example :

```
                ;ORG        0000h
vRESET:         MOVPG       #0H
                BR          !PGM_START
vKS_Y:          MOVPG       #0H
                BR          !INT_KS_Y
vINT0:          MOVPG       #0H
                BR          !INT_INT0
vINT1:          MOVPG       #0H
                BR          !INT_INT1
vT0:            MOVPG       #0H
                BR          !INT_T0
vT1:            MOVPG       #0H
                BR          !INT_T1
vWDT_VDI:       MOVPG       #0H
                BR          !INT_WDT_VDI
vERA:           MOVPG       #0H
                BR          !INT_ERA
vPGM:           MOVPG       #0H
                BR          !INT_PGM
```

```
;ORG             INT_ADDR
INT_KS_Y:        JOB_TO_WORK
                 RETI
INT_INT0:        JOB_TO_WORK
                 RETI
INT_INT1:        JOB_TO_WORK
                 RETI
INT_T0:          JOB_TO_WORK
                 RETI
INT_T1:          JOB_TO_WORK
                 RETI
INT_WDT_VDI:     JOB_TO_WORK
                 RETI
INT_ERA:         JOB_TO_WORK
                 RETI
INT_PGM:         JOB_TO_WORK
                 RETI
```

9.2. Interrupt Control Register

I flag of SFR is a interrupt mask enable flag.
When I flag = "0", all interrupts become disable.
When I flag = "1", interrupts can be selectively enabled and disabled by contents of corresponding Interrupt Enable Register(IENR0).
When interrupt is occurred, interrupt request flag is set,and Interrupt request is detected at the edge of interrupt signal. The accepted interrupt request flag is automatically cleared during interrupt cycle process.
The interrupt request flag maintains "1" until the interrupt is accepted or is cleared in program. In reset state, interrupt request flag register (IRQR0) is cleared to "0".
It is possible to read the state of interrupt register and to manipulate the contents of register.

• **External Interrupt Edge selection Register 0 (IEDS0)**

	7	6	5	4	3	2	1	0	
IEDS0	-	-	IEDI1		IEDI0		IEDK		30h
initial value	0	0	0	0	0	0	0	0	
R/W	-	-	W	W	W	W	W	W	

Selection Mode of IEDS0

Bit Name	Selection Mode		Remarks
-	0	-	
-	0	-	
IEDI1	00	Disable	INT1
	01	Falling Edge Selection	
	10	Rising Edge Selection	
	11	Both Edge Selection	
IEDI0	00	Disable	INT0
	01	Falling Edge Selection	
	10	Rising Edge Selection	
	11	Both Edge Selection	
IEDK	00	Disable	KS
	01	Falling Edge Selection	
	10	Rising Edge Selection	
	11	Both Edge Selection	

• **Interrupt Enable Register 0 (IENR0)**

	7	6	5	4	3	2	1	0	
IENR0	PGME	ERAE	WVE	T1E	T0E	INT1E	INT0E	KSYE	32h
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of IENR0

Bit Name	Selection Mode		Remarks
PGME	1	Program Interrupt enable	
ERAE	1	Erase Interrupt enable	
WVE	1	WDT or VDI Interrupt enable	*In interrupt service routine → check VDIR flag
T1E	1	Timer 1 Interrupt enable	
T0E	1	Timer 0 Interrupt enable	
INT1E	1	External Interrupt 1 enable	
INT0E	1	External Interrupt 0 enable	
KSYE	1	Key Scan or Y register Overflow Interrupt enable	*In interrupt service routine → check INTY flag → After CLRY instruction

• **Interrupt Request Flag Register 0 (IRQR0)**

	7	6	5	4	3	2	1	0	
IRQR0	PGMF	ERAF	WVF	T1F	T0F	INT1F	INT0F	KSYF	33h
initial value	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Selection Mode of IRQR0

Bit Name	Selection Mode		Remarks
PGMF	1	Program Interrupt Request enable	
ERAF	1	Erase Interrupt Request enable	
WVF	1	WDT or VDI Interrupt Request enable	
T1F	1	Timer 1 Interrupt Request enable	
T0F	1	Timer 0 Interrupt Request enable	
INT1F	1	External Interrupt 1 Request enable	
INT0F	1	External Interrupt 0 Request enable	
KSYF	1	Key Scan or Y register Overflow Interrupt Request enable	

9.3. Interrupt Timing

Interrupt Request Sampling Time :
-. Maximum 2 machine cycle (2 machine cycle Instructions)

Interrupt preprocess step is 1 machine cycle

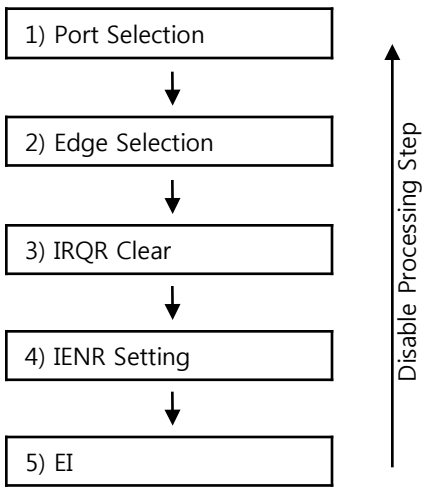
9.4. The valid timing after executing Interrupt control instructions

I flag is valid just after executing of EI/DI on the contrary.

9.5. Multiple Interrupt

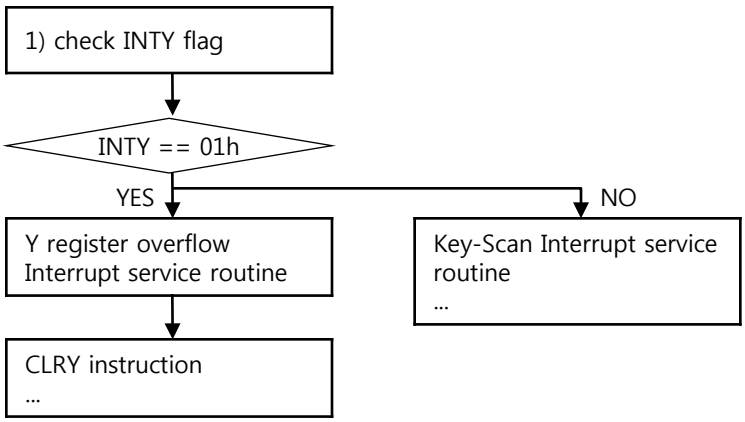
If there is an interrupt, Interrupt Mask Enable Flag is automatically cleared before entering the Interrupt Service Routine. After then, no interrupt is accepted. If EI instruction is executed, interrupt mask enable bit becomes "1", and each enable bit can accept interrupt request.
When two or more interrupts are generated simultaneously, the highest priority interrupt is accepted.

9.6. Key-Scan or External Interrupt Enable Processing Step

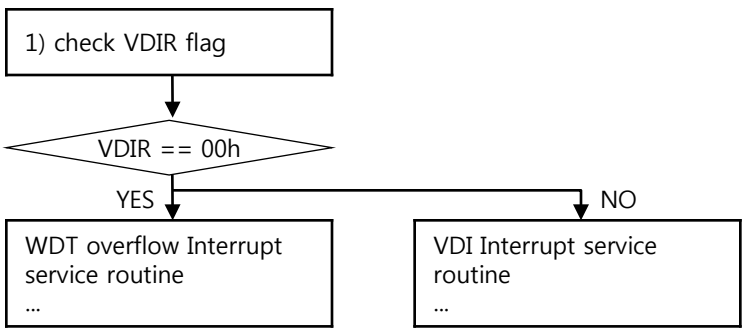


9.7. Interrupts for checking flag

Key-Scan or INTY Interrupt Processing Step



WDT or VDI Interrupt Processing Step



9.8. Interrupt Processing Sequence

When an interrupt is accepted, the on-going process is stopped and the interrupt service routine is executed. After the interrupt service routine is completed it is necessary to restore everything to the state before the interrupt occurred.
As soon as an interrupt is accepted, the content of the program counter is saved in the stack register which is 16 level stack area, and the contents of status flag register (SFR) is saved on the interrupt stack register (INTSK) which is 8 level stack area.
At the same time, the content of the vector address corresponding to the accepted interrupt, which is in the interrupt vector table, enters into the program counter and interrupt service is executed. In order to execute the interrupt service routine, it is necessary to write the jump addresses in the vector table corresponding to each interrupt.

Interrupt Processing Step

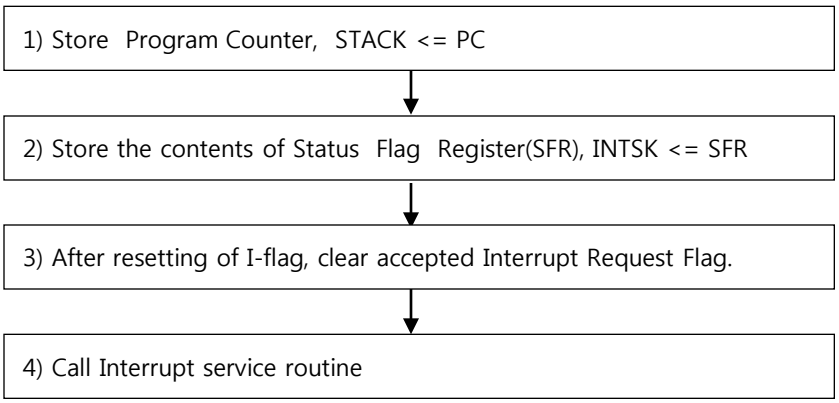
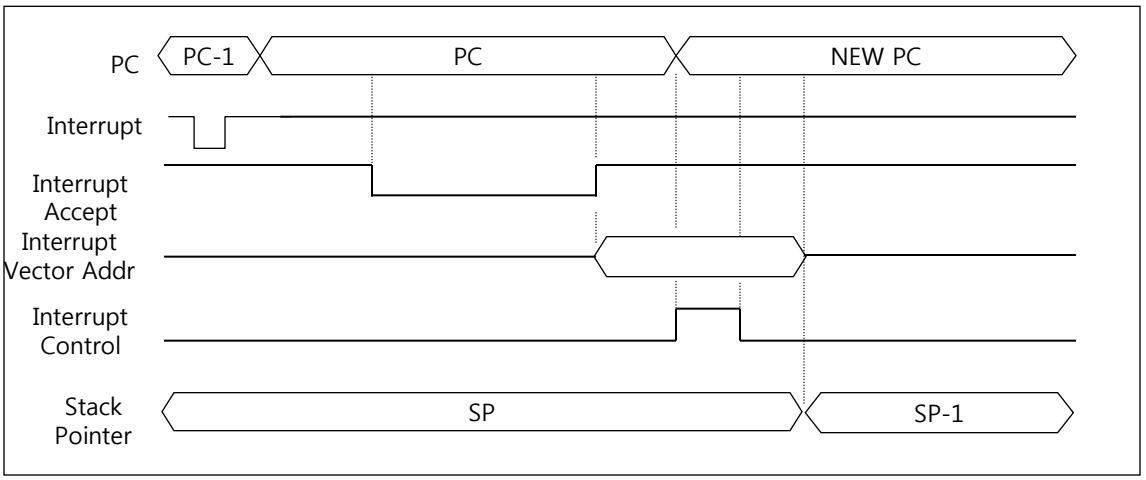


Fig. Interrupt Processing Step Timing



10. STOP/SLEEP FUNCTION

10.1. Stop Mode

STOP mode can be entered by STOP instruction during program.
In STOP mode, oscillator is stopped to make all clocks stop, which leads to less power consumption. All registers and RAM data are preserved.
"NOP" instruction should be follows STOP instruction for pre-charge time of Data Bus line.

```
ex)     STOP        ;STOP instruction execution
        NOP         ;NOP instruction
```

Table. Operation State in Stop Mode

Internal circuit	STOP mode	REMARKS
Oscillator	Stop	
Internal CPU clock	Stop	
Register	Retained	
RAM	Retained	
I/O port , OUTPUT port	Retained (except ROUT)	ROUT = "Hi-Z"
Timer	Stop	
Watch dog Timer	Reset and restart at stop release	
Address Bus, Data Bus	Retained	

10.2. Stop Mode Release

Release of STOP mode is executed by Power on reset , Key input Port(one of R0 , R1) which is selected by R0FN and R1FN register for stop release is both edge , external interrupt and Low voltage detection (LVD) mode release .
When there is a release signal of STOP mode, the instruction execution starts after stabilization oscillation time($2^{14} \times 4/f_{OSC}$ = 16.384ms at f_{OSC} = 4MHz)

Table. Stop Mode Release

Release Factor	Release Method	REMARKS
Power on reset	By Power on reset, Stop mode is release and system is initialized	
R0,R1 Port (key input)	Stop mode is released by low input of selected pin by R0FN,R1FN register	
External interrupt	Stop mode is release external interrupt input	
Release from LVD detection	Stop mode is release when release from LVD detection.	

10.3. Sleep Mode

Sleep mode can be entered by SLEEP instruction during program.
In SLEEP mode, oscillator and Peripheral source clock is running but system clock is stopped, which leads to less power consumption. All registers and RAM data are preserved.
"NOP" instruction should be follows SLEEP instruction for pre-charge time of Data Bus line.

```
ex)     SLEEP          ;SLEEP instruction execution
        NOP            ;NOP instruction
```

Table. Operation State in Sleep Mode

Internal circuit	SLEEP mode	REMARKS
Oscillator	Running	
Internal CPU clock	Stop	
Register	Retained	
RAM	Retained	
I/O port , OUTPUT port	Retained (except ROUT)	ROUT = "Hi-Z"
Timer	Operation	
Watch dog Timer	Reset and restart at sleep release	
Address Bus, Data Bus	Retained	

10.4. Sleep Mode Release

Release of SLEEP mode is executed by Power on reset , Key input Port(one of R0 , R1) which is selected by R0FN and R1FN register for sleep release is both edge , external interrupt, timer interrupt and Low voltage detection (LVD) mode release .
When there is a release signal of SLEEP mode, the instruction execution starts after stabilization time($2^5 \times 4/f_{OSC}$ = 32us at f_{OSC} = 4MHz)

Table. Sleep Mode Release

Release Factor	Release Method	REMARKS
Power on reset	By Power on reset, Sleep mode is release and system is initialized	
R0,R1 Port (key input)	Sleep mode is released by low input of selected pin by R0FN,R1FN register	
External interrupt	Sleep mode is release external interrupt input	
Timer interrupt	Sleep mode is release Timer interrupt input	

11. RESET FUNCTION

11.1. Power On RESET

Power On Reset circuit automatically detects the rise of power voltage
(the rising time should be within 50ms). Until the power voltage reaches a certain voltage level, internal reset signal is maintained at "L" Level until oscillator is stable.
After power applies and starting of oscillation, this reset state is maintained for about oscillation cycle of fosc/4 $x2^{16}$ (about 65.536ms : at 4MHz).

fig. Block Diagram of Power On Reset Circuit

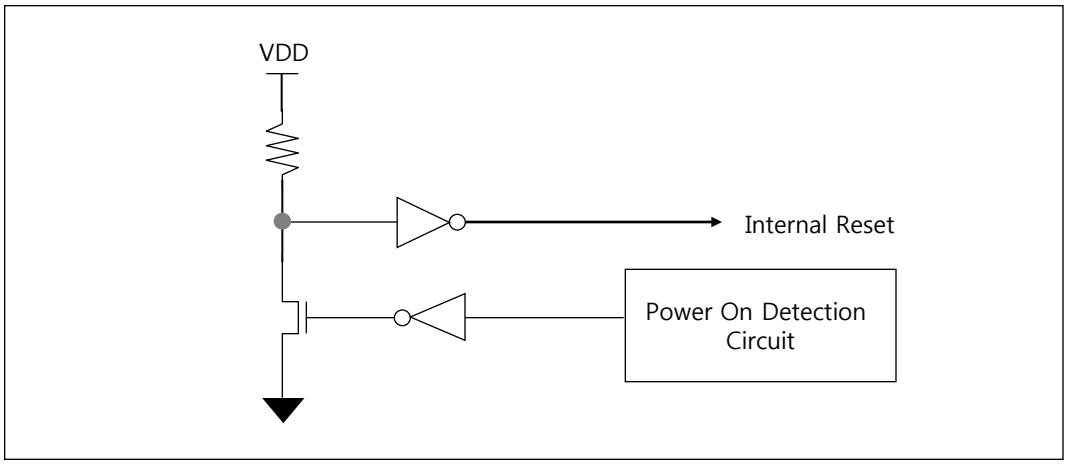
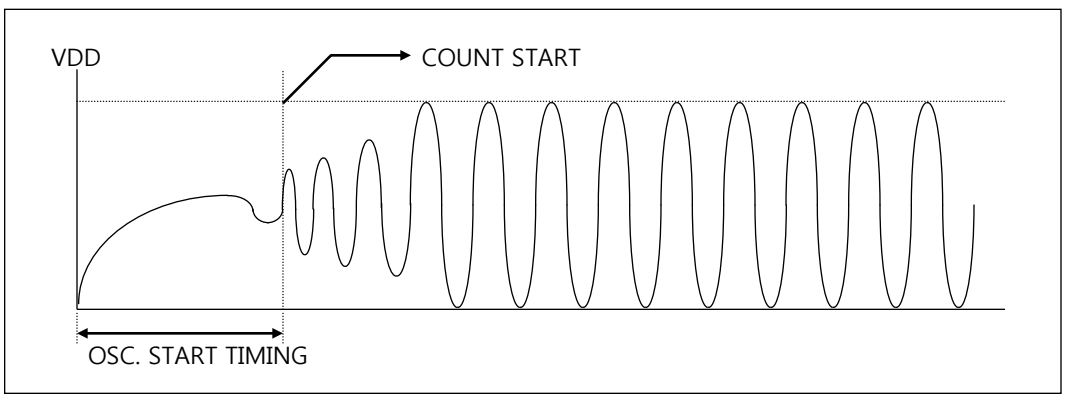


fig. Oscillator stabilization diagram



Notice. When Power On Reset, oscillator stabilization time doesn't include OSC. Start time.

12.1. Low Voltage Detection Condition

An on board voltage comparator checks that VDD is at the required level to ensure correct operation of the device.
If VDD is below a certain level, Low voltage detector forces the device into low voltage detection mode.

12.2. Low Voltage Detection Mode

There is no power consumption except stop current.
1. STOP mode release function is disabled.
2. I/O port is configured as input mode (with pull-up resistor).
3. Data memory is retained until voltage through external capacitor is worn out.
4. Interrupt disabled.
5. ROUT port is low level.
6. Oscillator is stop.

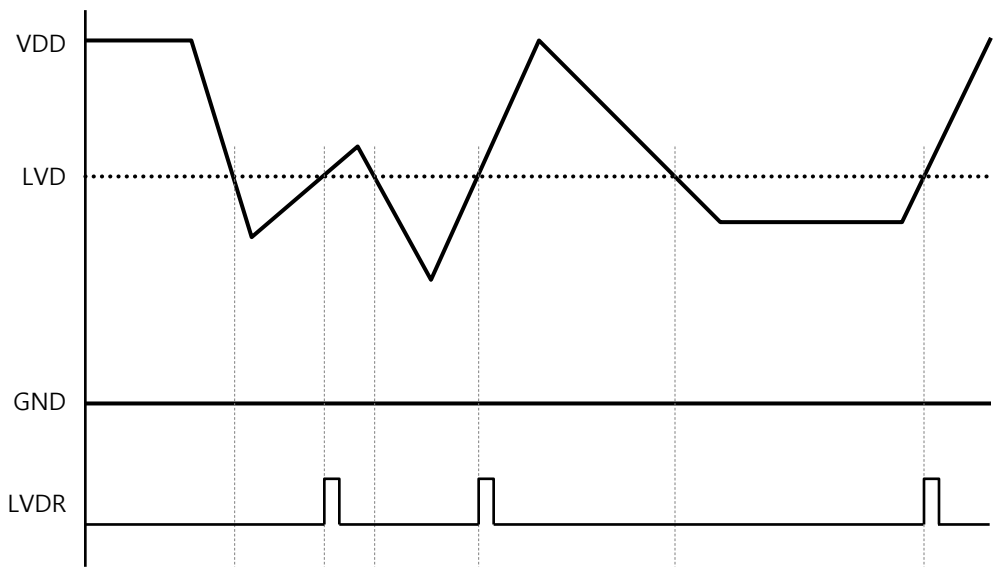
12.3. Release of Low Voltage Detection Mode

Reset signal result from new battery or any other power wakes the low voltage detection mode and come into normal reset state. It depends on user whether to execute RAM clear routine or not.

12.4. Low Voltage Detection voltage selection (Cell option)

User can select the voltage of Low Voltage detection voltage level.
One is high voltage version , another is low voltage version.

12.5. Timming Diagram (LVD RESET mode)



12.6. Voltage Detection Indicator Register

It is useful to display the consumption of Batteries.
If V_{DD} power level is below a low voltage level which is higher than low voltage detection level (refer to Fig .) , The bit of VDIR register could be set according to the V_{DD} level sequentially.
The V_{DD} detection levels for Indication are three , that is , VDIER[2:0] of VDIER Register.
The V_{DD} detection flag for Indication are three , that is , VDIR[6:4], VDIR[2:0] of VDIR Register.
If detection is occurred, flag is set. After READ VDIR, flag VDIR[6:4] is cleared automatically.
The detection voltage level is in the DC Characteristics.

(Notice) ENST must become SET necessarily if VDI is used in STOP Mode or RESET Mode.

- **Voltage Detection Indicator Enable Register (VDIER)**

	7	6	5	4	3	2	1	0	
VDIER	ENST	VDIRST	VDIER5	VDIER4	VDIER3	VDIER2	VDIER1	VDIER0	7Eh
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

Selection Mode of VDIER

Bit Name	Selection Mode		Remarks
ENST	0	Disable	
	1	Enable at STOP & RESET mode	
VDIRST	0	Interrupt enable	if(VDIER[4:0] == enable)
	1	RESET enable Must Set (ENST=1)	
VDIER5	0	Disable	-
	1	Enable	*Indicator voltage : 4.0V
VDIER4	0	Disable	-
	1	Enable	*Indicator voltage : 3.5V
VDIER3	0	Disable	-
	1	Enable	*Indicator voltage : 3.0V
VDIER2	0	Disable	-
	1	Enable	*Indicator voltage : 2.5V
VDIER1	0	Disable	-
	1	Enable	*Indicator voltage : 2.3V
VDIER0	0	Disable	-
	1	Enable	*Indicator voltage : 2.1V

• **Voltage Detection Indicator Data Register (VDIDR)**

	7	6	5	4	3	2	1	0	
VDIDR	-	-	VDIDR5	VDIDR4	VDIDR3	VDIDR2	VDIDR1	VDIDR0	7Eh
initial value	0	0	0	0	0	0	0	0	
R/W	R	R	R	R	R	R	R	R	

Selection Mode of VDIDR

Bit Name	Selection Mode		Remarks
-	0	-	-
-	0	-	-
VDIDR5	Set	*Indicator Status	always VDD ≤ 4.0V
VDIDR4	Set	*Indicator Status	always VDD ≤ 3.5V
VDIDR3	Set	*Indicator Status	always VDD ≤ 3.0V
VDIDR2	Set	*Indicator Status	always VDD ≤ 2.5V
VDIDR1	Set	*Indicator Status	always VDD ≤ 2.3V
VDIDR0	Set	*Indicator Status	always VDD ≤ 2.1V

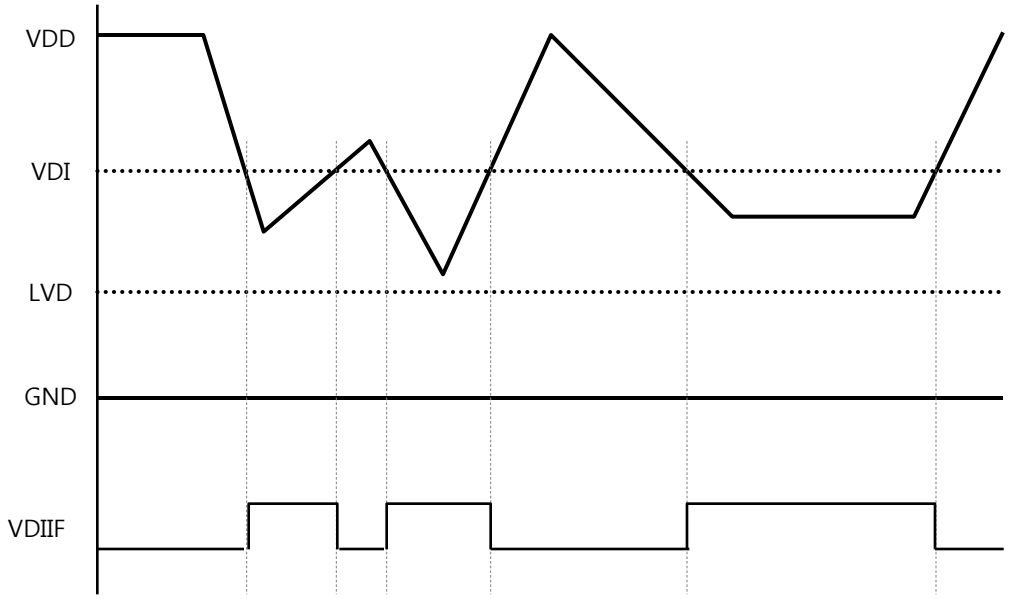
• **Voltage Detection Indicator Flag Register (VDIFR)**

	7	6	5	4	3	2	1	0	
VDIFR	-	-	VDIFR5	VDIFR4	VDIFR3	VDIFR2	VDIFR1	VDIFR0	7Fh
initial value	0	0	0	0	0	0	0	0	
R/W	R	R	R	R	R	R	R	R	

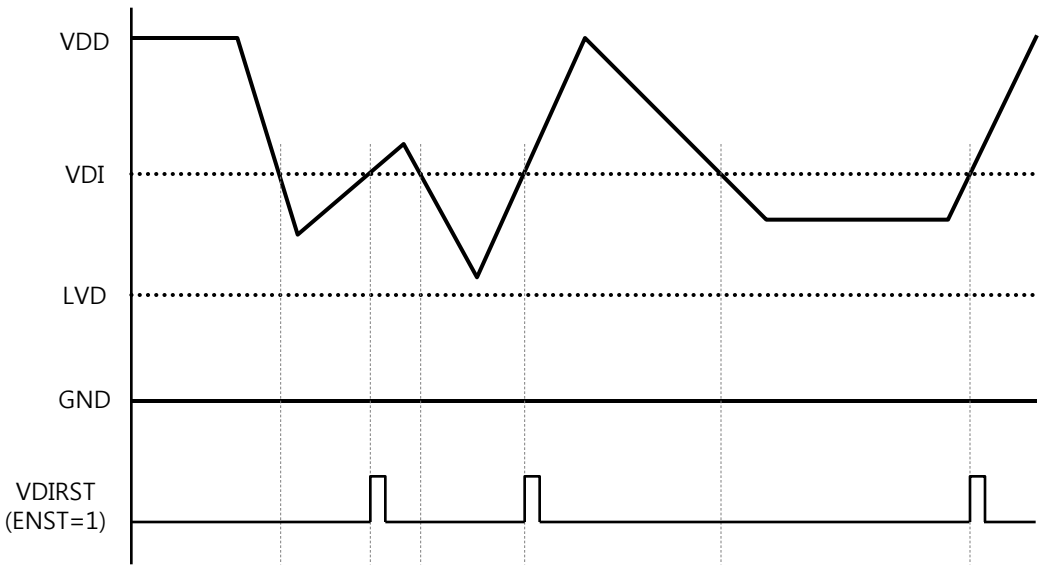
Selection Mode of VDIFR

Bit Name	Selection Mode		Remarks
-	0	-	
-	0	-	
VDIFR5	Set	if (VDIDR5 == 1), flag is set.	if (VDD > 4.0V), after read, automatically cleared.
VDIFR4	Set	if (VDIDR4 == 1), flag is set.	if (VDD > 3.5V), after read, automatically cleared.
VDIFR3	Set	if (VDIDR3 == 1), flag is set.	if (VDD > 3.0V), after read, automatically cleared.
VDIFR2	Set	if (VDIDR2 == 1), flag is set.	if (VDD > 2.5V), after read, automatically cleared.
VDIFR1	Set	if (VDIDR1 == 1), flag is set.	if (VDD > 2.3V), after read, automatically cleared.
VDIFR0	Set	if (VDIDR0 == 1), flag is set.	if (VDD > 2.1V), after read, automatically cleared.

12.7. Timming Diagram (VDI Interrupt mode)

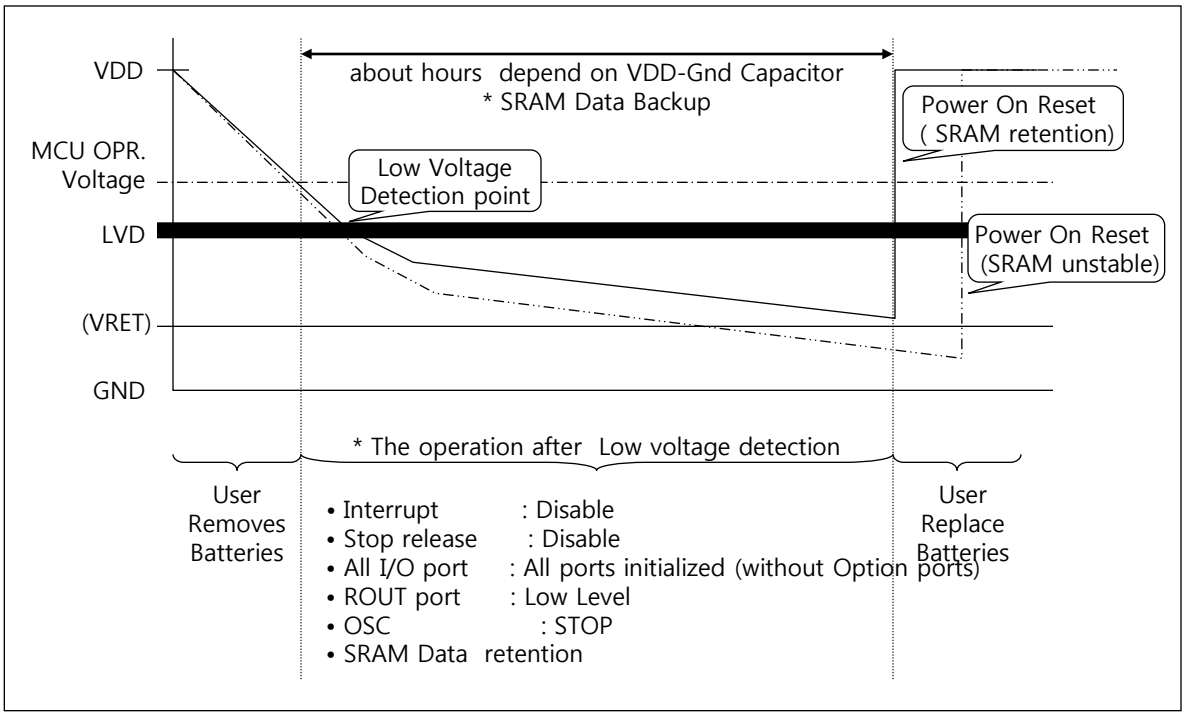


12.8. Timming Diagram (VDI RESET mode, Must set (ENST=1))



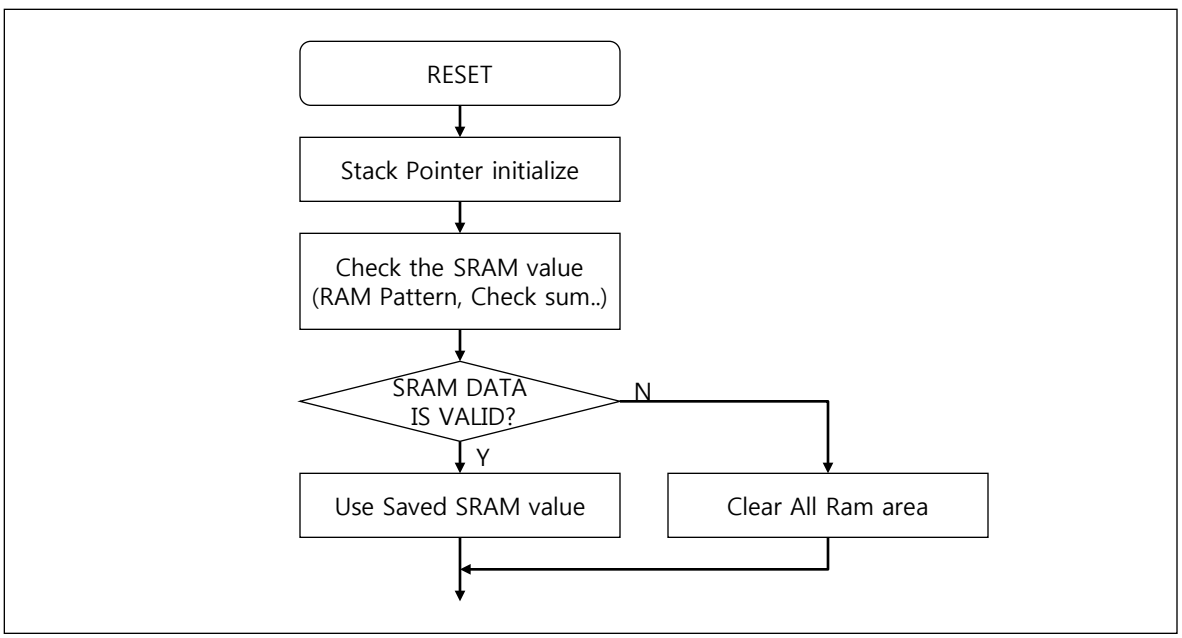
13.1 SRAM DATA BACK-UP after Low Voltage Detection

fig. Low Voltage Detection and Protection



13.2. S/W flow chart example after Reset using SRAM DATA Back-up

fig. S/W Flow Chart Example for SRAM Back-up



• **Page Buffer Register (PBUF)**

Program DATA Buffer, from SRAM to EEPROM

	7	6	5	4	3	2	1	0	
PBUF	PBUF7	PBUF6	PBUF5	PBUF4	PBUF3	PBUF2	PBUF1	PBUF0	6Dh
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

• **Erase Program Address Low Register (EPAL)**

Erase or Program Address Low

	7	6	5	4	3	2	1	0	
EPAL	EPAL7	EPAL6	EPAL5	EPAL4	EPAL3	EPAL2	EPAL1	EPAL0	6Eh
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

• **Erase Program Address High Register (EPAH)**

Erase or Program Address High

	7	6	5	4	3	2	1	0	
EPAH	EPAH7	EPAH6	EPAH5	EPAH4	EPAH3	EPAH2	EPAH1	EPAH0	6Fh
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

◈ EPM6 (EP Mode Register 6)

	7	6	5	4	3	2	1	0	
EPM6	ERA_MODE	PGM_MODE	-	-	-	-	-	-	39h
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

Selection Mode of EPM6

Bit Name		Selection Mode		Remarks
ERA_MODE	Erase/Program Mode Enable	00	Disable	
		01	Program Mode	
PGM_MODE		10	Erase Mode	
		11	-	
-	-	0	-	
-	-	0	-	
-	-	0	-	
-	-	0	-	
-	-	0	-	
-	-	0	-	

◈ EPM7 (EP Mode Register 7)

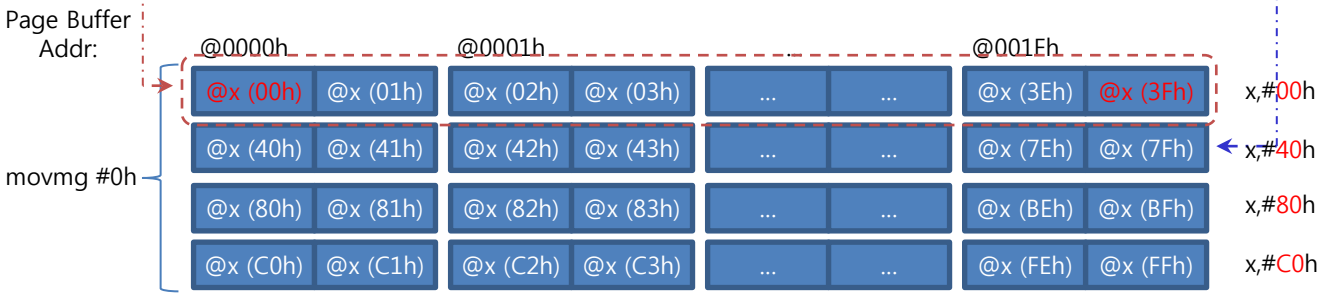
	7	6	5	4	3	2	1	0	
EPM7	-	-	-	SELFMODE	-	-	-	-	38h
initial value	0	0	0	0	0	0	0	0	
R/W	W	W	W	W	W	W	W	W	

Selection Mode of EPM7

Bit Name		Selection Mode		Remarks
-	-	0	-	
-	-	0	-	
-	-	0	-	
SELF_MODE	Self Erase/Program Mode Enable	0	Disable	
		1	Enable	
-	-	0	-	
-	-	0	-	
-	-	0	-	
-	-	0	-	

◈ Page Buffer(32-Word) Writing (from SRAM to Page-Buffer by @X)

```
                movmg       #0h              ;  or #1h or #2h
                mov         x,#00h
pbufwt00:       nop
                movr        pbuf,@x
                add         x,#01h
                cxne        x,#40h
                br          !pbufwt00
                nop
                movr        epah,#00h
                movr        epal,#00h    ; 'h0000 ~ 'h001f
                nop
Timer1:         Program/Erase time = 2.5ms/2.5ms
                wait timer = 50us
Command:        Program & Selfmode
                Erase & Selfmode
```



Self Program
step1 : Store SRAM Data by 64-byte unit.
step2 : Write SRAM Data(64-byte) to page buffer 32-word. @P0000(@R00:@R01), use @x .
step3 : Write Program Address(Word line=EPAH:EPAL) (@0000 ← @0000~@001F)
step4 : Set Program time (timer1 high width = 2.5ms)
step5 : Set Self Program Command (Program & Selfmode)

Self Erase
step1 : -
step2 : -
step3 : Write Erase Address(Word line=EPAH:EPAL) (@0000 ← @0000~@001F)
step4 : Set Erase time (timer1 high width = 2.5ms)
step5 : Set Self Erase Command (Erase & Selfmode)

*. Configuration Cell Options

◈ Configuration Bit Map

pgm/vfy Address : 8000h

reg write Address : 8800h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG0	LOCK	-	BYPSATLVDB	BYPSSEL	RSTS	XTS[2:0]			LVDSEL[1:0]		IRCFCAL[5:0]					
Initial	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Code Option Description	Option Write Value	remarks	
15	LOCK	LOCK enable	1	Disable	
			0	Enable	
14	-	-	1	Disable	
			0	-	
13	BYPSATLVDB	Bypass at LVD Mode	1	Disable	
			0	Enable	
12	BYPSSEL	Bypass Voltage Selection.	1	1.80V	
			0	1.65V	
11	RSTS	R00/RESETB Selection	1	R00	
			0	RESETB	
	Oscillator Type Selection			R15	R16
10 9 8	XTS[2:0]	Internal RC 4MHz	111	R15	R16
		Internal RC 8MHz	110	R15	R16
		External Clock Input	101	OSC1	R16
		XT Oscillator High Amp.	100	OSC1	OSC2
		XT Oscillator Low Amp.	011	OSC1	OSC2
			010		
			001		
		Internal RC 16MHz	000	R15	R16
7 6	LVDSEL[1:0]	LVD Selection Option	11	1.65V	
			10	1.8V	
			01	2.1V	
			00	2.3V	
5 4 3 2 1 0	IRCFCAL[5:0]	IRC16MHz Oscillator Center frequency calibration option	11_1111	16MHz	
			11_1110	0.5% Slow	
			~	~	
			10_0000	16% Slow	
			01_1111	0.5% Fast	
			~	~	
			00_0000	16% Fast	

*. Configuration Cell Options

◈ Configuration Bit Map

pgm/vfy Address : 8001h

reg write Address : 8801h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG1	LNNCAL[1:0]		LVDCAL[1:0]		R23	R22	R21	R20	R07	R06	R05	R04	R03	R02	R01	R00
Initial	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Code Option Description	Option Write Value	remarks
15 14	LNNCAL[1:0]	Sensitivity Control option (Leval3 is high. Leval0 is low.)	11	level1
			10	level0
			01	level2
			00	level3
13 12	LVDCAL[1:0]	LVD Cal. Option	11	1.65V
			10	Default + 0.05V
			01	Default + 0.10V
			00	Default - 0.05V
11	R15/R16	Port Pull-up enable at LVD mode	1	Disable
			0	Enable
10	R14	Port Pull-up enable at LVD mode	1	Disable
			0	Enable
9	R13	Port Pull-up enable at LVD mode	1	Disable
			0	Enable
8	R12	Port Pull-up enable at LVD mode	1	Disable
			0	Enable
7	R11	Port Pull-up enable at LVD mode	1	Disable
			0	Enable
6	R10	Port Pull-up enable at LVD mode	1	Disable
			0	Enable
5	R05	Port Pull-up enable at LVD mode	1	Disable
			0	Enable
4	R04	Port Pull-up enable at LVD mode	1	Disable
			0	Enable
3	R03	Port Pull-up enable at LVD mode	1	Disable
			0	Enable
2	R02	Port Pull-up enable at LVD mode	1	Disable
			0	Enable
1	R01	Port Pull-up enable at LVD mode	1	Disable
			0	Enable
0	R00	Port Pull-up enable at LVD mode	1	Disable
			0	Enable