COLOR LIGHT-TO-DIGITAL CONVERTER

Main features

- **PKG level trimming Support**
  - Multiple trimming by internal NVM
  - No need of complicated power control

- **RGB Color and Ambient Light Sensor Support**
  - Operation with five channels (R/G/B/C/IR)
  - Advanced color filter with high response
  - Operation condition : 0.0019lux to 5000lux @Green channel

- **Programmable Gain & Integration Time**
  - Very High Sensitivity

- **Low Dark Noise**
  - No dark count at fully dark condition

- **I2C Interface up to 400kbit/s**

- **I/O and Packages**
  - 4OPLGA: Optical Lend Grid Array, 4-pins
  - 2.95 x 1.50 x 1.50mm

- **Operating Conditions**
  - 2.7V to 3.6V Wide Voltage Range
  - -40°C to 70°C Temperature Range

- **Application**
  - Cell Phone
  - Digital TV, Tablet PC, Notebook PC
  - Navigation Systems
  - Other Display-equipped Portable Devices

AL8844

User's manual

V 1.41

Revision History

Version	Date	Revision list
1.00	2021.04.30	The First Edition.
1.10	2021.09.08	Fix Register Description
1.20	2021.11.11	Add I2C standard mode spec Update Optical Characteristics
1.30	2021.11.23	Update Optical Characteristics Fix operating temperature range
1.40	2022.01.10	Update Main features
1.41	2022.11.01	Revised the font of this document

Version 1.41

Published by AE team

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1 Overview

1.1. Description

The AL8844 is a high resolution color and IR(red, green, blue, clear and IR) light sensor which can transform illuminance (light intensity) to a digital signal output.

With the RGB color sensor, the brightness and color temperature of backlight can be adjusted based on ambient light source that makes the panel look more comfortable for human eyes. Additionally it can be used for detecting light source type as it reports the IR content of the light.

The wide dynamic range also allows for operation in short distance detection behind dark glass such as a cell phone. The operation voltage ranges from 2.7 to 3.6 volt.

Device Name	Interface	Temp. Range	Package
AL8844	I^2C	-40℃ to +70℃	4OPLGA

Table 1.1 Ordering Information of AL8844

1.2. Ordering Information

Part Number	Packing	Package	Pin No.	Quantity	Lead Free	Remark
AL8844PA	Tape & Reel	2.95 x 1.5 x 1.5mm	4	2500	Compliant	

Table 1.2 Ordering Information

1.3. Slave Address

The AL8844 can support 3 different I^2C slave addresses by factory trimming option.

TRIM Option	Slave Address
Default	1000_001x
TRIM Option 1	1000_010x
TRIM Option 2	1000_011x

Table 1.3 Slave Address by Trim Option

1.4. Features

- **RGB Color Sensor**
  - Convert incident light intensity to digital data
  - 16-bit ALS ADC resolution
  - Programmable exposure time for light sensing
  - Automatic light flickering cancellation supporting
  - Block off IR(Infrared) by coating visible light pass filter on R/G/B/C PD area
  - IR pass filter on IR PD area
  - Spectral response close to human eye
  - Linear ALS response for easy design
  - Low dark noise

- **Trimming**
  - Embedded NVM to support PKG or module level trimming
  - No need of high voltage input while trimming

- **Interface**
  - I^2C
  - Selectable I^2C slave address by factory trimming option

- **Operating Mode**
  - RUN mode (OSC active, ADC active)
  - IDLE/WAIT mode (OSC active, ADC inactive)
  - STOP mode (OSC inactive, ADC inactive)

- **Operating Voltage**
  - 2.7V~ 3.6V

- **Operating Temperature**
  - –40 ~ +70℃

- **Package Type**
  - 4OPLGA

2 Block diagram

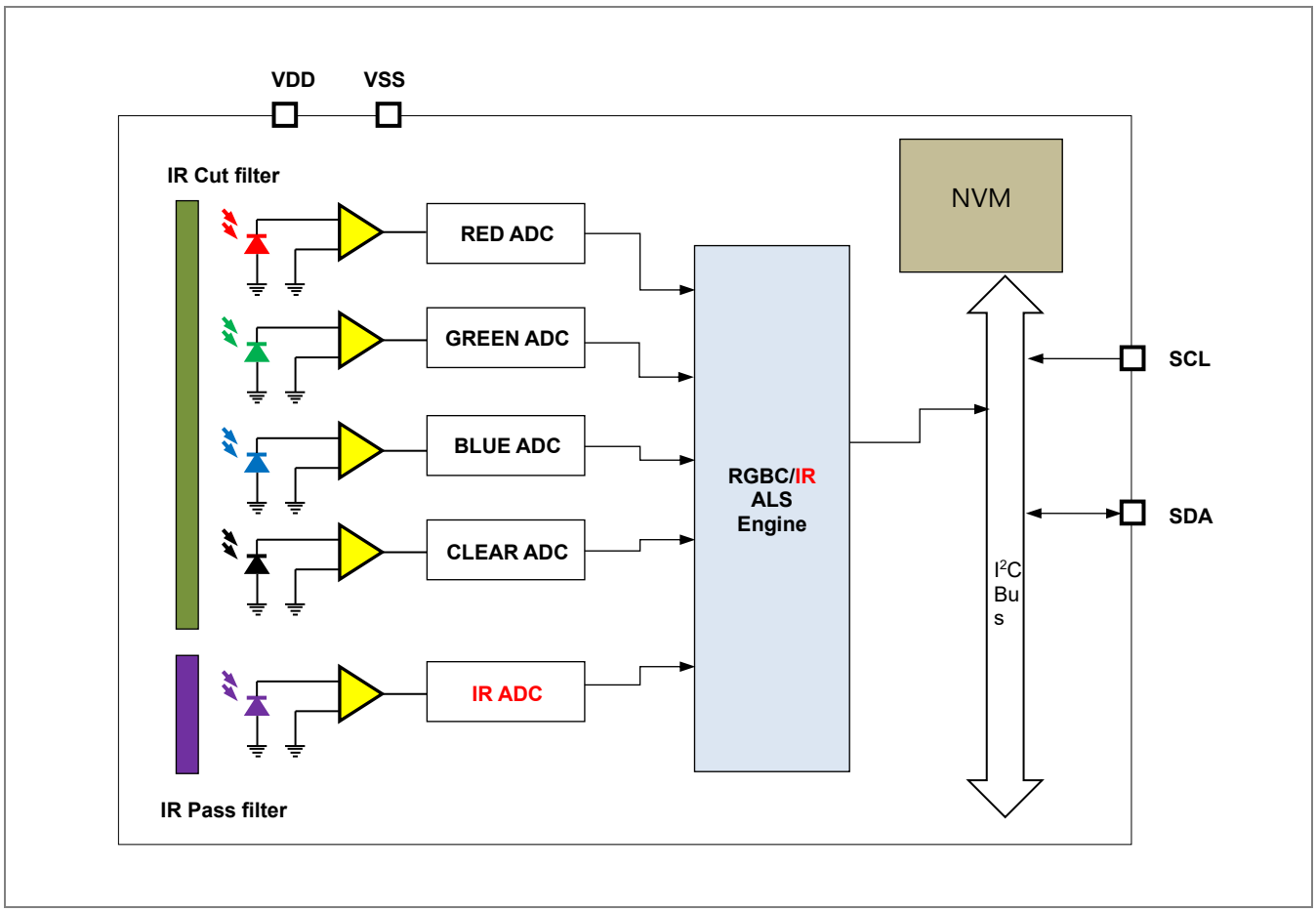

Figure 2.1 AL8844 Block Diagram

3 Package Diagram

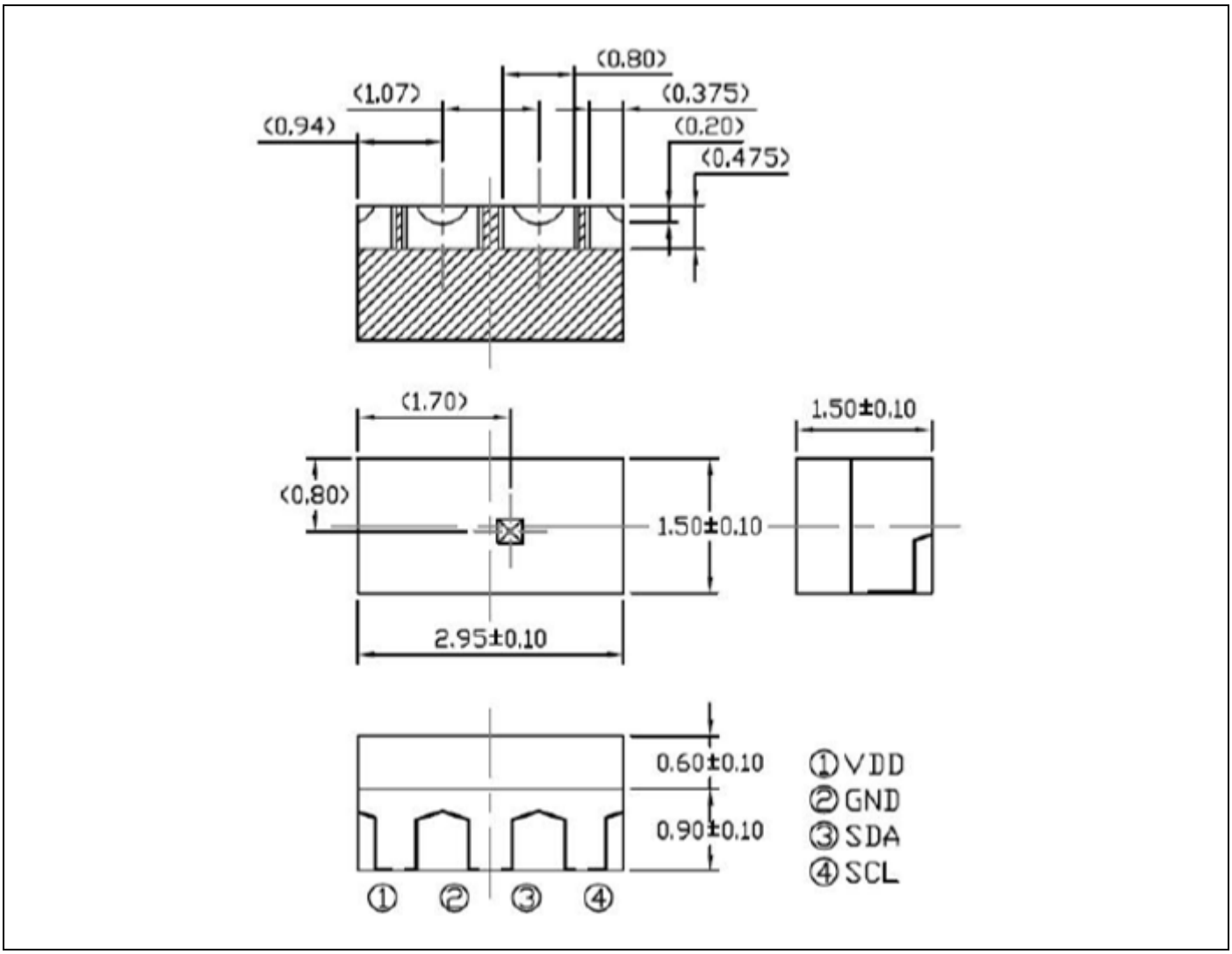

Figure 4.1 4OPLGA Package dimension

4 Pin Description

PIN Number	Pin Name	I/O	Function
1	VDD	Power	Power supply : 2.7 to 3.6V
2	GND	Ground	Ground
3	SDA	I/O(Open Drain)	I^2C Serial Clock Line
4	SCL	I(Open Drain)	I^2C Serial Data Line

Table 5.1 Pin Description

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	VDD		4.0	V	All voltages are with respect to VSS
Storage Temperature Range	T_{STG}	-40	85	°C	
Digital Output Voltage Range	VO	-0.5	4.0	V	
Digital Output Current	IO	-1	20	mA	
ESD Tolerance, human body model	VHBM		2,000	V	

Table 7.1 Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Voltage	VDD	2.7	3.0	3.6	V
Operating Free-air Temperature	T_A	-40		70	°C
Input Low Voltage	VIL			0.3VDD	V
Input High Voltage	VIH	0.7VDD			V

Table 7.2 Recommended Operating Conditions

5.3 DC Characteristics

(T_A= 25°C, VDD= 3.0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	SCL, SDA	0.7VDD			V
Input Low Voltage	V_{IL}	SCL, SDA			0.3VDD	V
Output Low Voltage	V_{OL}	VDD=3.0V, I_{OL}= 4mA; SCL, SDA			0.4	V
Input High Leakage Current	I_{IH}	SCL, SDA	–	–	1	uA
Input Low Leakage Current	I_{IL}	SCL, SDA	-1	–	–	uA
Internal Oscillator Frequency	f_{OSC}		3.7	4.0	4.3	MHz
Power Current	I_{STOP}	Stop mode (static)		1.0		uA
	I_{WAIT}	Idle/Wait mode (idle)		80	120	uA
	I_{DD}	Run mode (dynamic)		410	450	uA

Table 7.3 DC Characteristics

5.4 Optical Characteristics

(T_A= 25°C, VDD= 3.0V, IT=25ms, Gain=1X)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Peak Sensitivity Wavelength	λ_{PR}	Red ADC		610		nm
	λ_{PG}	Green ADC		525		nm
	λ_{PB}	Blue ADC		480		nm
	λ_{PC}	Clear ADC		525		nm
	λ_{PIR}	IR ADC		825		nm
ADC Count Value @200lux	A_R_{200L}	White LED, 3500K	5940	6600	7260	count
	A_G_{200L}		7605	8450	9295	count
	A_B_{200L}		3330	3700	4070	count
	A_C_{200L}		15210	16900	18590	count
	A_IR_{200L}	Ir LED, 940nm	TBD	TBD	TBD	count
Dark Count Value @0lux	A_R_{0L}	WLED, IrLED Off		0	1	count
	A_G_{0L}			0	1	count
	A_B_{0L}			0	1	count
	A_C_{0L}			0	1	count
	A_IR_{0L}			0	1	count

Table 7.4 Optical Characteristics

5.5 I²C Characteristics

(T_A=-40°C ~ +70°C, VDD=2.7V ~ 3.6V)

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN	MAX	MIN	MAX	
SCL Clock frequency	t_{SCL}	0	100	0	400	kHz
Hold time after (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	–	0.6	–	us
LOW period of SCL clock	t_{LOW}	4.7	–	1.3	–	us
HIGH period of SCL clock	t_{HIGH}	4.0	–	0.6	–	us
Setup time for a repeated START condition	$t_{SU:STA}$	4.7	–	0.6	–	us
Data hold time	$t_{HD:DAT}$	0	3.45	0	0.9	us
Data setup time	$t_{SU:DAT}$	250	–	100	–	ns
Clock/data fall time	t_F	–	300	0	300	ns
Clock/data rise time	t_R	–	1000	0	300	ns
Setup time for STOP condition	$t_{SU:STO}$	4.0	–	0.6	–	us
Bus free time between STOP and START condition	t_{BUF}	4.7	–	1.3	–	us

Table 7.5 I²C Characteristics

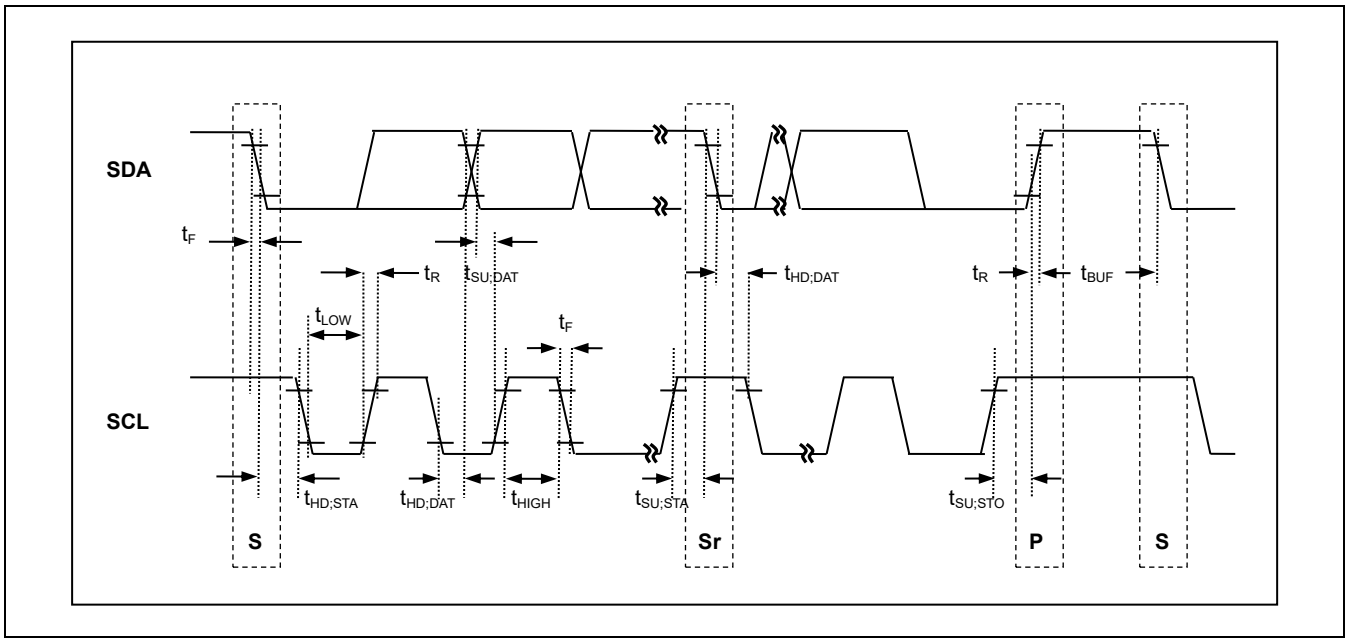

Figure 1.1 **I²C Timing**

5.6 Typical Characteristics

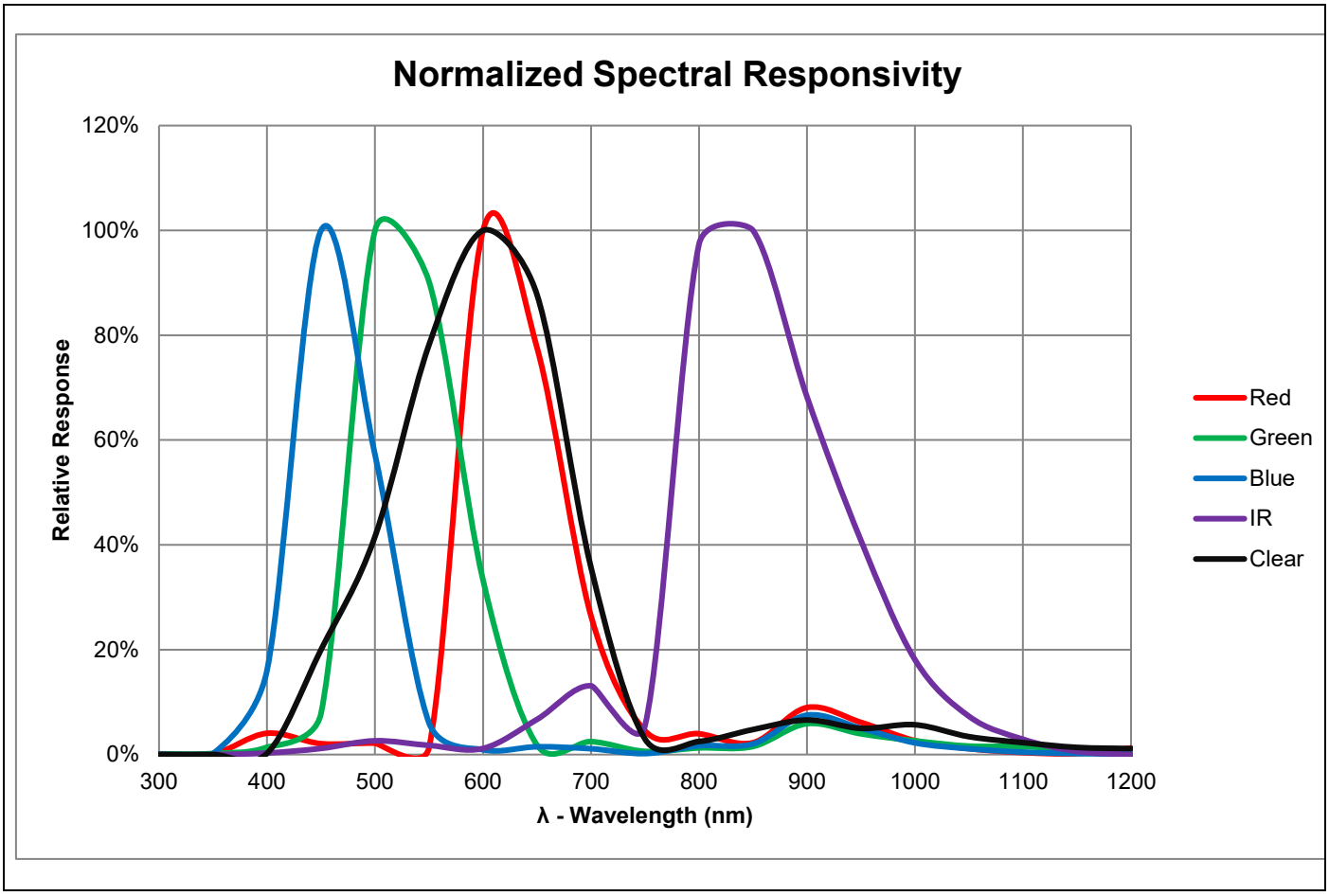

Figure 1.2 **Spectral Responsivity**

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

5.7 Recommended Circuit and Layout

5.7.1 Application Note

Place a 0.1uF decoupling capacitor close to VDD pin to reject power supply noise.

The pull up resistors of two line serial bus are recommended to be around 4.7kΩ.

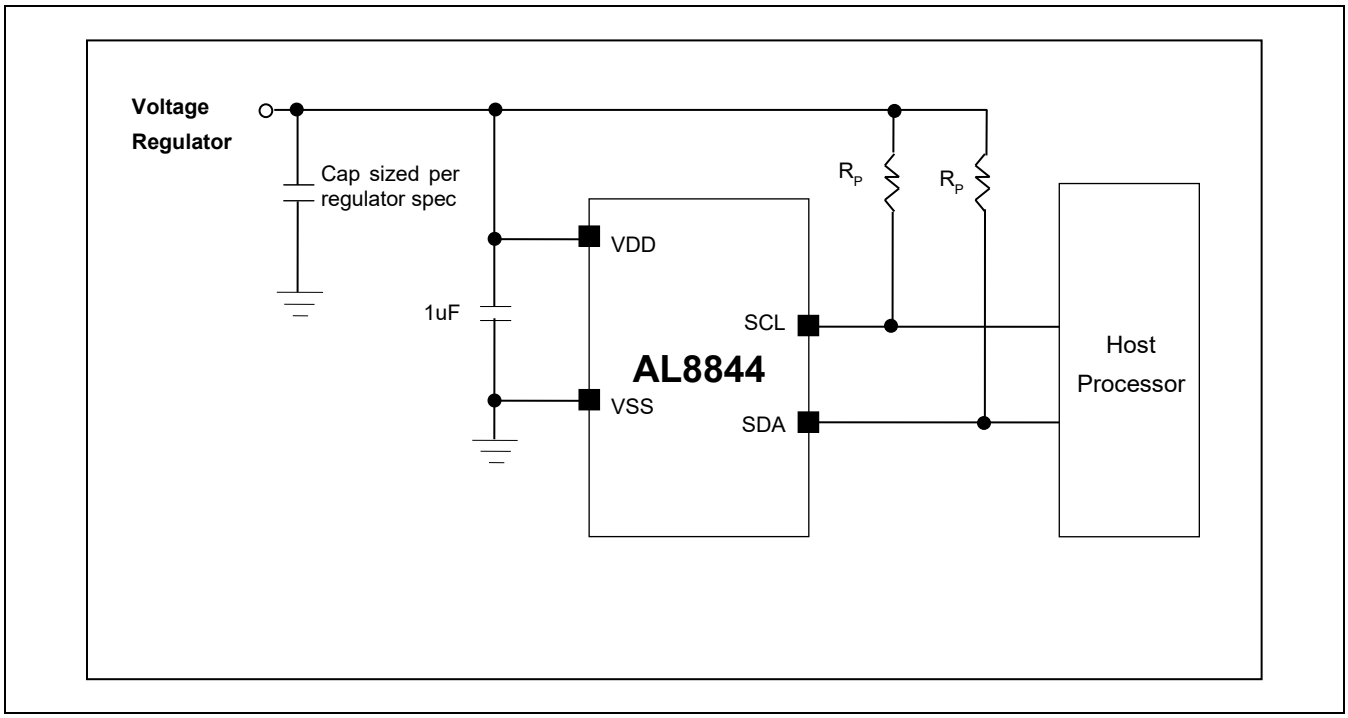

Figure 1.3 **Typical Appliation Circuit**

5.7.2 Application Information

The below sequences explain how to develop user program with AL8844 in case the I^2C slave address is set to default value.

1) Operating voltage 2.7 to 3.6V
2) Select I^2C speed, 100kHz ~ 400kHz
3) Set SLAVE address to $82_H(1000001_B)$.

   To communicate with AL8844, the I^2C master device should send 1^{st} byte of 82_H right after start condition for a write operation, or 83_H for a read operation.
4) Initiate communication with AL8844.

Write operation :

S(M)+S_ADDR_W(82_H,M)+A(S)+R_ADDR(XX_H,M)+ACK(S)+W_DATA_1+A(S)…+P(M).

(Example) How to load 33_H in CONTROL(80_H), 01_H in ITIME(81_H) register?

S+82_H+A+80_H+A+33_H+01_H+A+P

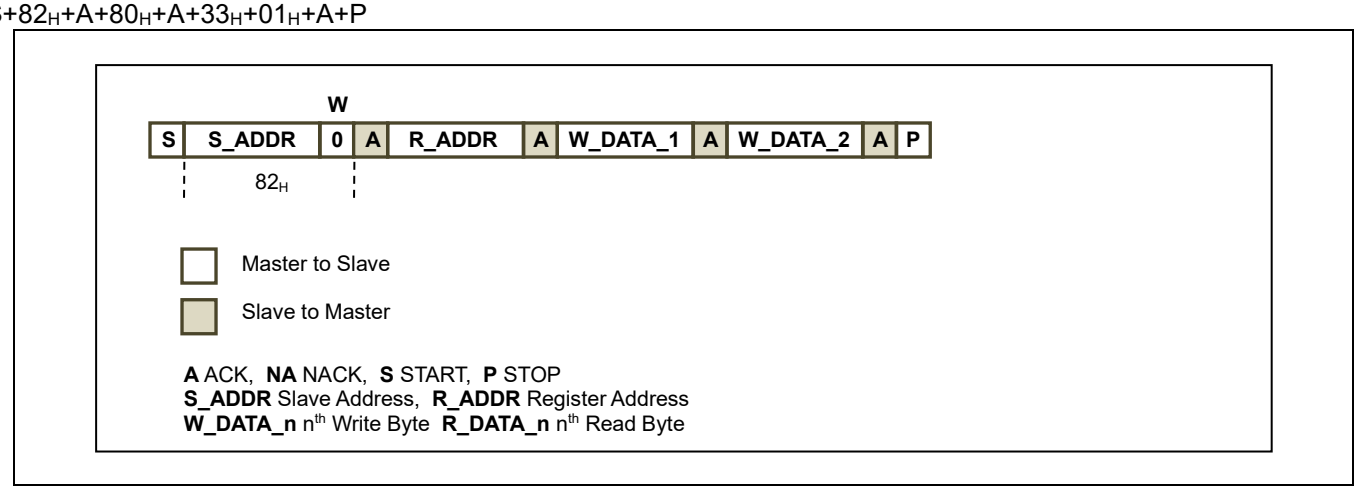

Figure 1.1 **I²C Write Example**

Read operation :

S(M)+S_ADDR_W($B6_H$,M)+A(S)+R_ADDR(XX_H,M)+A(S)+S+

S_ADDR_R(83_H,M)+A(S)+R_DATA_1(S)+A(M)…+NA+P(M)

(Example) How to read values from GDATAL(92_H) and GDATAH(93_H) registers?

S+82_H+A+92_H+A+S+83_H+A+RDATAL+ACK+RDATAH+NA+P

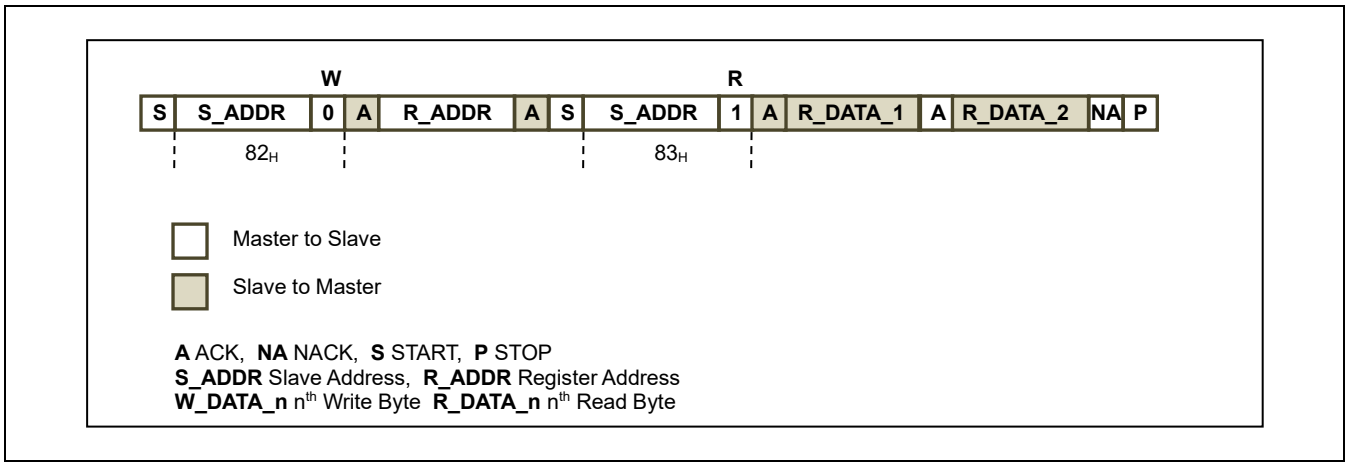

Figure 1.1 **I²C Read Example**

6 Operation

6.1 I²C

6.1.1 Overview

The I²C is one of industrial standard serial communication protocols, and which uses 2 bus lines Serial Data Line (SDA) and Serial Clock Line (SCL) to exchange data. Because both SDA and SCL lines are open-drain output, each line needs pull-up resistor. The features are as shown below.

- Compatible with 7bit addressing I²C interface
- Support up to 400kHz data transfer speed
- Slave operation only

6.1.2 I²C Bit Transfer

The data on the SDA line must be stable during HIGH period of the clock, SCL. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The exceptions are START(S), repeated START(Sr) and STOP(P) condition where data line changes when clock line is high

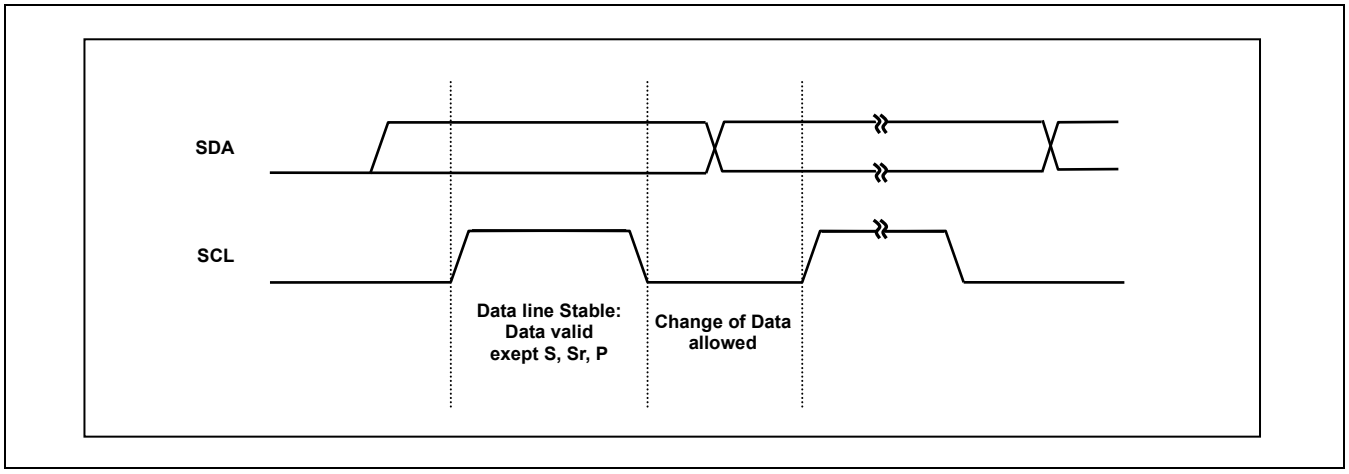

Figure 2.1 **Bit Transfer on the I²C Bus**

6.1.3 Start / Repeated Start / Stop

One master can issue a START (S) condition to notice other devices connected to the SCL, SDA lines that it will use the bus. A STOP (P) condition is generated by the master to release the bus lines so that other devices can use it.

- A high to low transition on the SDA line while SCL is high defines a START (S) condition.
- A low to high transition on the SDA line while SCL is high defines a STOP (P) condition.

Start and STOP conditions are always generated by a master. The bus is considered to be busy after START condition. The bus is considered to be free again after STOP condition, ie, the bus is busy between START and STOP condition. If a repeated START condition (Sr) is generated instead of STOP condition, the bus stays busy. So, the START and repeated START conditions are functionally identical

6.1.4 Data Transfer

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unlimited. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave can't receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

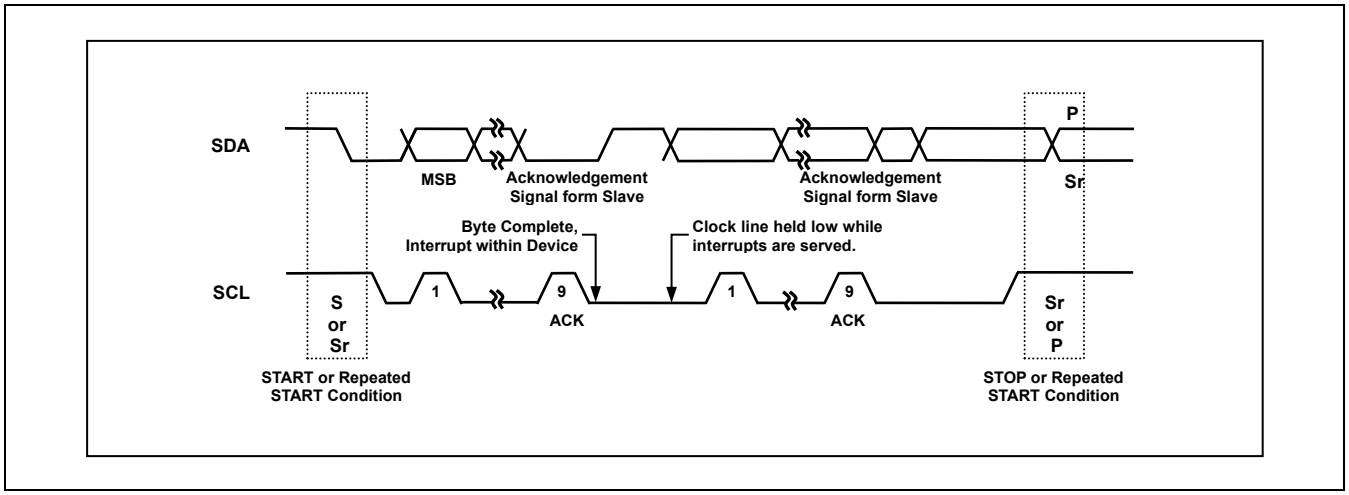

Figure 2.2 **Stop or Repeated Start condition**

6.1.5 Acknowledge

The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. When a slave is addressed by a master (Address Packet), and if it is unable to receive or transmit because it's performing some real time function, the data line must be left HIGH by the slave. And also, when a slave addressed by a master is unable to receive more data bits, the slave receiver must release the SDA line (Data Packet). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

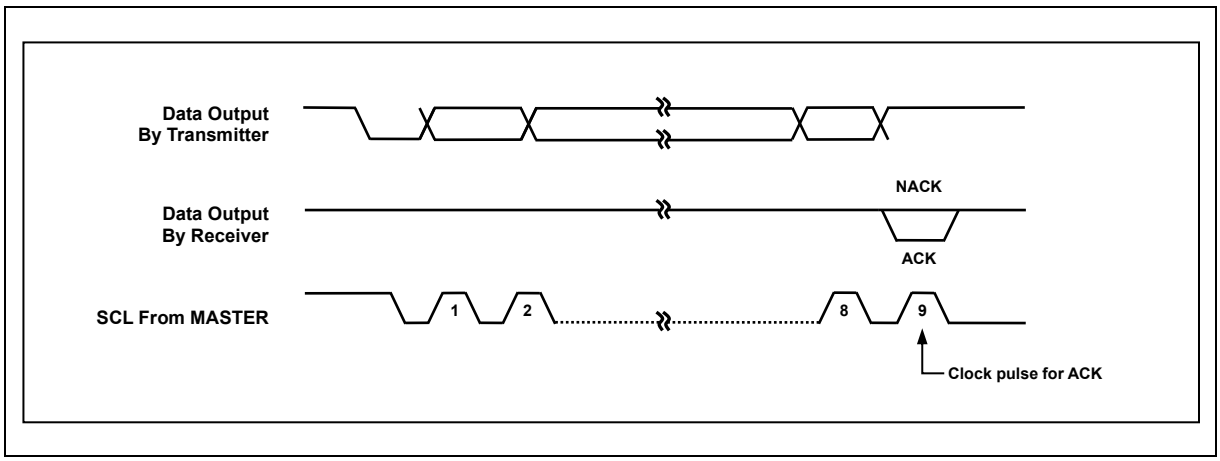

Figure 2.3 **Acknowledge on the I²C Bus**

6.1.6 Operation

The I²C is byte-oriented serial protocol and data transfer between master and this slave device is initiated by a start condition(S) from master. After start condition, the master sends 7-bit slave address and 1-bit read-write control bit. We call these 8-bit data address packet. The next bytes followed by address packet are all data packet unless another start condition is detected before a stop condition.

The 2nd byte sent from master after address packet with write direction is interpreted as base register or memory address byte. And this base address is incremented only when master transmits more than 2 bytes after start condition because the 2nd byte is register address field.

According to the FACTORY TRIMMING option, AL8844's I²C slave address can be configured as "1000001_B"(Default) , "1000010_B"(TRIM Option 1) or "1000011_B"(TRIM Option 2).

6.1.7 Write Protocol (Master Transmitter)

The master transmits a start condition(S), slave address and Write bit. If the high 7-bits of address packet equal to the device's slave address, the AL8844 acknowledges by pulling down the SDA line at the 9th SCL clock period. After address packet and acknowledge bit, the master transmits a data which is used for base address accessing internal memory or register of the device. The master transmits a number of data to be written and the slave always acknowledges for every data received. To finish transfer the master sends a stop condition regardless of the acknowledgement.

The destination address for incoming data byte increments automatically by one data packet. For example, if master transmits 5 data bytes including a base address(=register address in the following figure) byte and the base address is configured as 00_H, the internal address is defined as 00_H for 1st data byte, 01_H for 2nd data byte, 02_H for 3rd data byte and 03_H for 4th data byte. This applies to Read Protocol also.

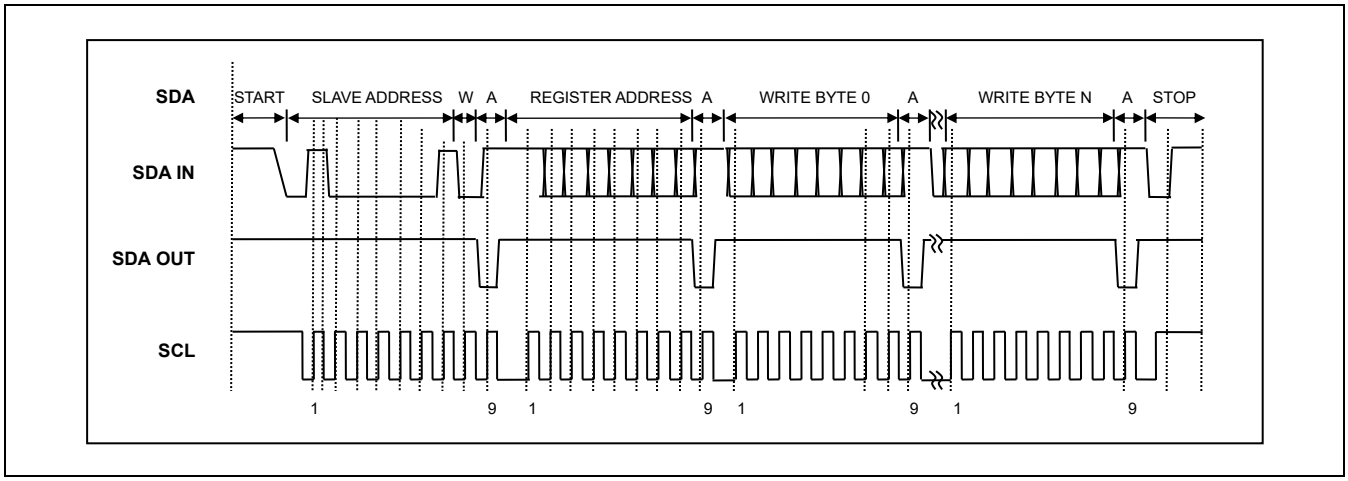

Figure 2.1 **I²C Write Protocol (Default Slave Address)**

6.1.8 Read Protocol (Master Receiver)

The master transmits a start condition(S), slave address and Write bit. If the high 7-bits of address packet equal to the device's slave address, the AL8844 acknowledges by pulling down the SDA line at the 9th SCL clock period. After address packet and acknowledge bit, the master transmits a data which is used for base address accessing internal memory or register of the device. To initiate read operations, the master sends repeated start condition and slave address with Read bit. After this address packet, the master reads data bytes until it does not acknowledges. Note that to send a stop condition after receiving last data byte, the master must generate a NACK(not acknowledging) on the last data byte received. Like Write Protocol, the read address increases by 1 after every read byte.

Note that the transfer direction changes in this protocol.

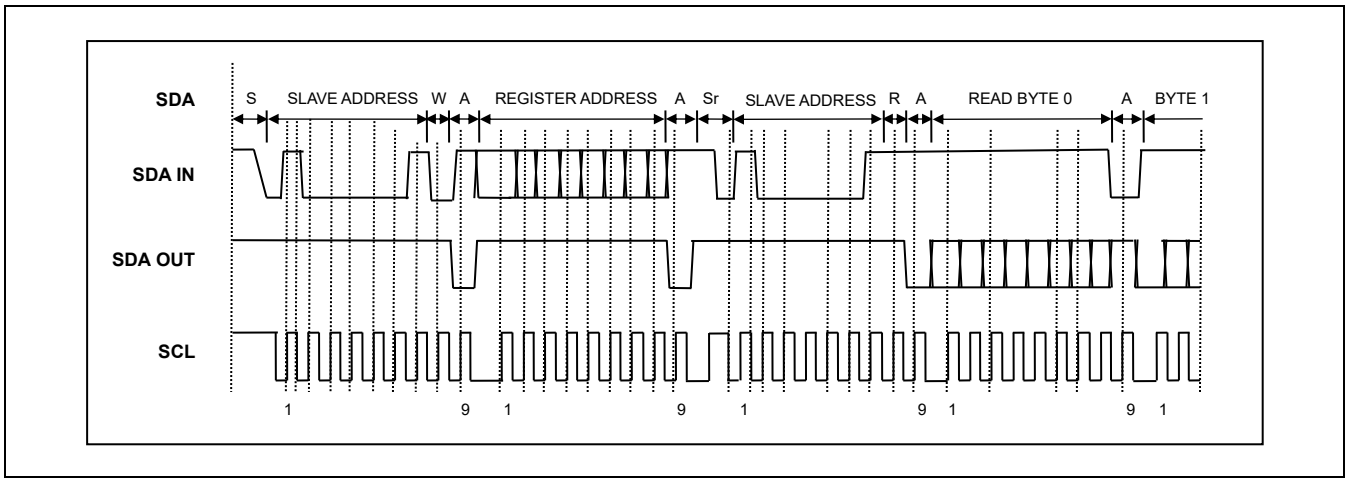

Figure 2.1 **I²C Read Protocol (Default Slave Address)**

6.2 Registers

6.2.1 Register Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
–	Address Set Register	ADDRSET	–	–	–	–	–	–	–	–	–
80H	Control Register	CONTROL	R/W	0	0	0	0	0	–	0	0
81H	ALS Integration Time Control Register	ITIME	R/W	0	0	0	0	0	0	0	0
82H	Wait Time Register	WTIME	R/W	0	1	1	1	1	1	1	1
86H	I2C Time Out Control Register	I2CTOC	R/W	0	–	–	–	–	–	0	0
87H	ADC Channel Enable Register	ADCCHEN	R/W	–	–	–	1	1	1	1	1
8FH	ID Register ***	ID	R	1	0	1	0	0	0	0	0
90H	Red ADC Low Data Register	RDATAL	R	0	0	0	0	0	0	0	0
91H	Red ADC High Data Register	RDATAH	R	0	0	0	0	0	0	0	0
92H	Green ADC Low Data Register	GDATAL	R	0	0	0	0	0	0	0	0
93H	Green ADC High Data Register	GDATAH	R	0	0	0	0	0	0	0	0
94H	Blue ADC Low Data Register	BDATAL	R	0	0	0	0	0	0	0	0
95H	Blue ADC High Data Register	BDATAH	R	0	0	0	0	0	0	0	0
96H	Clear ADC Low Data Register	CDATAL	R	0	0	0	0	0	0	0	0
97H	Clear ADC High Data Register	CDATAH	R	0	0	0	0	0	0	0	0
98H	IR ADC Low Data Register	IRDATAL	R	0	0	0	0	0	0	0	0
99H	IR ADC High Data Register	IRDATAH	R	0	0	0	0	0	0	0	0

Table 7.6 SFR Map

6.2.2 Register Description

ADDRSET (Address Set Register): --H

7	6	5	4	3	2	1	0
ADDR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

ADDR[7:0]	Base address for subsequent register access. When the I²C master initiates a write protocol with a start bit and slave address, the second byte is used to configure register address of AL8844.

CONTROL (Control Register): 80H

7	6	5	4	3	2	1	0
ONESHOT	Reserved		ATCON[2:0]			ALSEN	IRCEN
R/W	-	-	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

ONESHOT	Select operation mode.	
	0	IC goes stop mode after 1 integration cycle
	1	IC continues integrating until it is stopped by I²C command
RESERVED	Write only 00_B	
ATCON[2:0]	Select ALS integration time NOTE1	
	000	Test mode only
	001	25ms
	010	50ms
	011	100ms
	100	200ms
	101	Reserved
	110	400ms
	111	Reserved
ALSEN	Enable ALS operation	
	0	ALS disable
	1	ALS(R/G/B/C/IR) enable
IRCEN	Enable internal RC oscillator (typically 4.0MHz). Enabling oscillator turns on AL8844 automatically.	
	0	Turn off AL8844
	1	Turn on AL8844

NOTE)

1. The real ALSEN bit is updated after internal oscillator is enabled, typically 500us. It means reading CONTROL register before oscillator stabilization time will return "---- 0000_B" when writing '1' to these bits while IRCEN bit is disabled or enabling ALSEN and IRCEN bits simultaneously.

ITIME (ALS Integration Time Control Register): 81H

7	6	5	4	3	2	1	0
Reserved	Reserved	OFFSETC[5:0]					
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

RESERVED Write only '0' to this bit field

OFFSETC[5:0] Select dark offset rejection scheme

1A	No offset cancellation
25	Auto offset cancellation
others	Fixed offset cancellation (default)

NOTE)

1. Used for test purpose

WTIME (Wait Time Control Register): 82H

7	6	5	4	3	2	1	0
WEN	WTIME[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 7FH

WEN Wait time enable.
Wait time is controlled by WTIME register.

0	Wait time is disabled
1	Wait time is inserted between consecutive integrating cycles.

WTIME[6:0] Wait time. Specifies the wait time between continuous ALS operations in 20ms interval.
Wait time = (WTIME[6:0] + 1) x 20ms
The maximum wait time is 1,280ms (@FFH). NOTE1

The WTIME is used to reduce average power consumption, because the ADC stops integrating during wait time period.

When ALSEN=1_B, the internal operating mode is as follows : ALS—WAIT—ALS—WAIT—ALS—WAIT—ALS … (Refer to **7.3.2 Operation**)

NOTE)

1. Although setting a larger wait time contributes to reduce average consumption current, it makes update period and response time longer.

I2CTO (I2C Time Out Control Register): 86H

7	6	5	4	3	2	1	0
TOF	–	–	–	–	–	TOEN	TOVS
R/W	–	–	–	–	–	R/W	R/W

Initial value: 00H

TOF Timeout flag

Timeout event is occurred and AL8844 is initialized except for this flag.

0 No event

1 Timeout event occurred. Writing '0' clears this flag.

TOEN Timeout feature enable

The low period of SCL exceeds tTIMEOUT(25 or 35ms), AL8844 releases I2C bus(SCL, SDA) and initialized to reset state.

0 Disable timeout feature

1 Enable timeout feature

TOVS I2C time out target value select

TOVS	tTIMEOUT
0	25ms
1	35ms

ADCCHEN (ADC Channel Enable Register): 87H

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	ACH_EN[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 1FH

Reserved

ACH_EN[4:0] ADC channel control

ACH_EN	Operation
1XXXX	ADC IR channel enable.
X1XXX	ADC C channel enable.
XX1XX	ADC B channel enable.
XXX1X	ADC B channel enable.
XXXX1	ADC R channel enable.

NOTE)

1. For proper operation, enable or disable each channel before setting ALS_EN bit in CONTROL register.

ID (Device ID Register): 8FH

7	6	5	4	3	2	1	0
ID[7:0]							
R	R	R	R	R	R	R	R

Initial value: A0H

ID[7:0] Device ID

RDATAL (Red ADC Low Data Register): 90H
RDATAH (Red ADC High Data Register): 91H
GDATAL (Green ADC Low Data Register): 92H
GDATAH (Green ADC High Data Register): 93H
BDATAL (Blue ADC Low Data Register): 94H
BDATAH (Blue ADC High Data Register): 95H
CDATAL (Clear ADC Low Data Register): 96H
CDATAH (Clear ADC High Data Register): 97H
IRDATAL (IR ADC Low Data Register): 98H
IRDATAH (IR ADC High Data Register): 99H

7	6	5	4	3	2	1	0
RDATA[7:0]							
RDATA[15:8]							
GDATA[7:0]							
GDATA[15:8]							
BDATA[7:0]							
BDATA[15:8]							
CDATA[7:0]							
CDATA[15:8]							
IRDATA[7:0]							
IRDATA[15:8]							
R	R	R	R	R	R	R	R

Initial value: 00H

RDATA[15:0]	Red ADC data
GDATA[15:0]	Green ADC data
BDATA[15:0]	Blue ADC data
CDATA[15:0]	Clear ADC data
IRDATA[15:0]	IR ADC data

These registers hold the result of ADC. RDATA[15:0], GDATA[15:0], BDATA[15:0], CDATA[15:0] and IRDATA[15:0] hold the 16bit ADC data of red/green/blue/clear/ir channels.

The resolution and gain of ADC is controlled by CONTROL register.

6.3 Operation Description

6.3.1 Overview

After applying VDD, the device will initially be in the power down mode.
To start ALS sensing, set the PWR_ON bit in CONTROL register to 1, which enables internal 4MHz RC oscillator.

The CONTROL, ITIME or WTIME registers should be configured for the preferred operating conditions.
Finally the ALSEN bit in CONTROL register should be set to 1 to enable all ADC channel.

6.3.2 Operation

The internal state machine manages the operation of AL8844.

It controls the ALS functionality and power down modes. Average power consumption is managed by wait cycles.

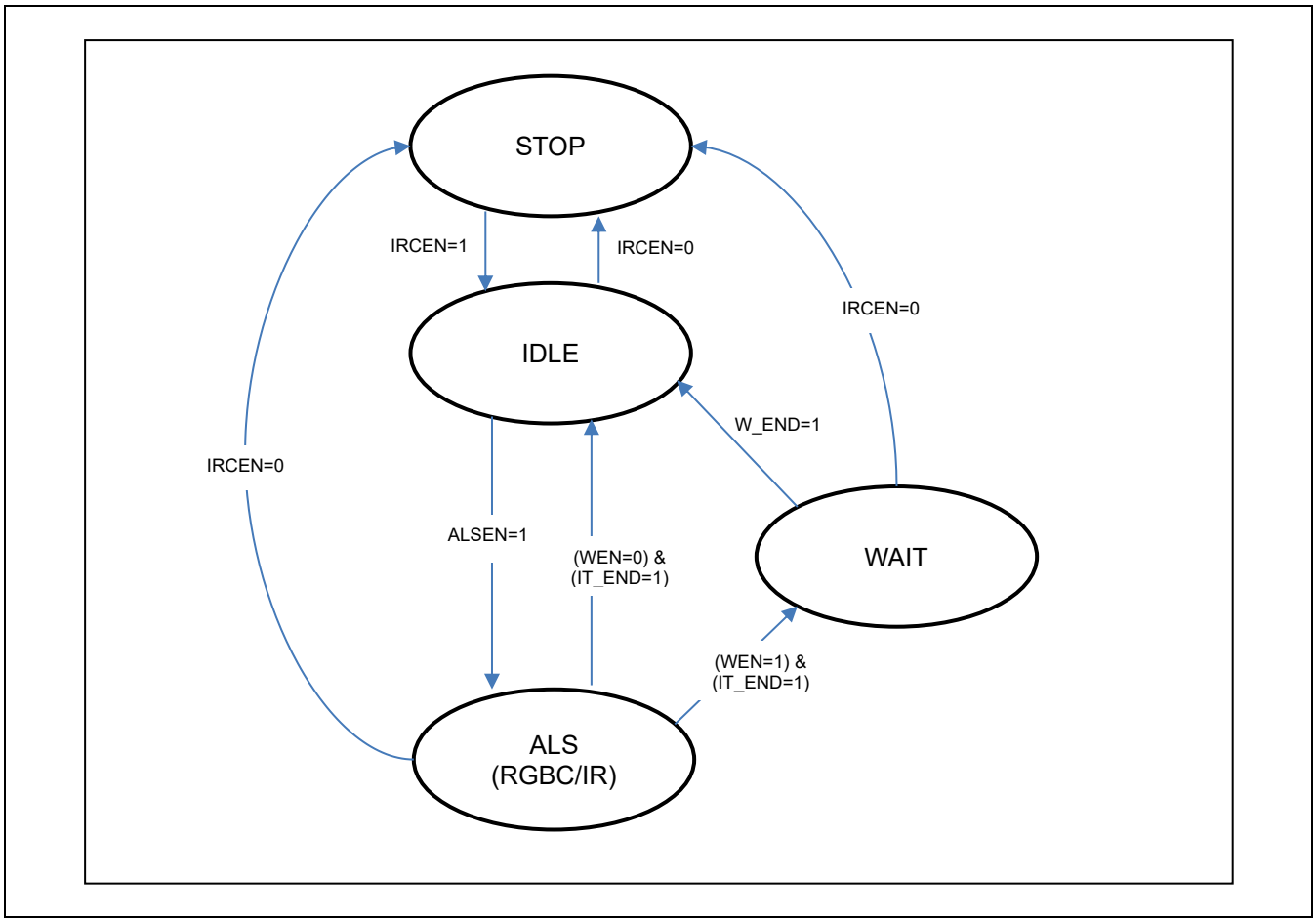

Figure 2.1 **Simplified ALS State Machine**

NOTE)

1. When WTIME=00_H, WEN is 0. When WTIME != 00_H, WEN is 1.
2. ALSEN is bit1 in COTROL register.
3. IT_END means 1 integration cycle is over.
4. W_END means wait cycle is over.

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